Single-Electron Pass-Transistor Logic with Multiple Tunnel Junctions and Its Hybrid Circuit with MOSFETs

Young-Kyun Cho and Yoon-Ha Jeong

ABSTRACT—To improve the operation error caused by the thermal fluctuation of electrons, we propose a novel single-electron pass-transistor logic circuit employing a multiple-tunnel junction (MTJ) scheme and modulate a parameters of an MTJ single-electron tunneling device (SETD) such as the number of tunnel junctions, tunnel resistance, and voltage gain. The operation of a 3-MTJ inverter circuit is simulated at 15 K with parameters C_g=C_T=C_{clk}=1 aF, R_T=5 MΩ, V_{clk}=40 mV, and V_{in}=20 mV. Using the SETD/MOSFET hybrid circuit, the charge state output of the proposed MTJ-SETD logic is successfully translated to the voltage state logic.

Keywords—Multiple-tunnel junction, single-electron transistor, pass-transistor logic, hybrid circuit.

I. Introduction

Correlated single-electron tunneling based on the Coulomb blockade effect in ultra small structures has attracted considerable interest in recent years [1]. Various logic design schemes [2]-[6] have been proposed using single-electron tunneling devices (SETDs). From the points of view of power consumption, switching speed, and CMOS-compatible operation, single-electron pass-transistor logic (SEPTL) [2], [5] is one of the most promising design schemes. SEPTL has a tree structure which is composed of unit devices with a two-way switching function. Each of the two-way switching devices receives an electron through an entry lead from the preceding device and then sends it on to the following device through the branch that doesn't need the large fan in/fan out.

Though the SEPTL has many advantages, the operation error cannot be avoided because only one electron drives the circuit. One way to improve the operation error of the circuit is to utilize multiple-tunnel junctions (MTJs) [7]. This leads to a decrease in the total capacitance of the island inside the MTJ circuit, to an increase in the charging energy of the island, and to an increase in the operation temperature.

The other significant problem of SEPTL is the charge state output which cannot cascade conventional circuitry. Therefore, to implement SEPTL into large scale integrated circuits, we have to transform the charge state output into the voltage state output. The SETD/MOSFET hybrid circuit [4] is the most attractive combination because the high input impedance of MOSFET can compensate for the inherent SETD disadvantage of the high output impedance of the SETD.

In this paper, we propose an MTJ-SEPTL circuit for the reduction of the operation error and confirm its basic operation.

II. Simulation Results and Discussions

Because the SETD is sensitive to the charge of one electron, charge fluctuation will produce an unacceptable error. Therefore, thermal error is caused by an undesirable tunneling induced by thermal agitation. The thermal operation error rate is given in [5] as

$$ER = \frac{\Gamma_2 + \Gamma_3 + \Gamma_4 + \cdots}{\Gamma_1 + \Gamma_2 + \Gamma_3 + \Gamma_4 + \cdots}, \quad (1)$$

while the tunneling rate across the *j*-th tunnel junction is given in [5] as

Manuscript received Aug.4, 2004; revised Oct. 1, 2004.

Young-Kyun Cho (phone: +82 42 860 6561, email: ykcho@etri.re.kr) is with Basic Research Laboratory, ETRI, Daejeon, Korea.

Yoon-Ha Jeong (email: yhjeong@postech.ac.kr) is with the Department of Electrical and Electronics Engineering, POSTECH, Pohang, Korea.

$$\Gamma_j = \frac{1}{e^2 R_j} \cdot \frac{-\Delta F}{1 - \exp(-\Delta F / k_B T)}, \qquad (2)$$

where e is the electronic charge, R_j is the tunnel resistance of the *j*-th tunnel junction, k_B is Boltzmann's constant, T is the absolute temperature, and ΔF is the difference of free energy. In most cases, the expected tunneling (Γ_1) occurs, and the circuit transforms to the expected subsequent state. However, the tunneling probability of the other tunnel junction is not zero; an error sometimes occurs due to such undesirable tunneling. Also, the tunneling rate is a function of the corresponding free energy difference, which depends on the circuit parameters and voltages of the clocks and inputs. Therefore, in order to diminish the thermal operation error, it is very important to modulate the parameters of the SETD.

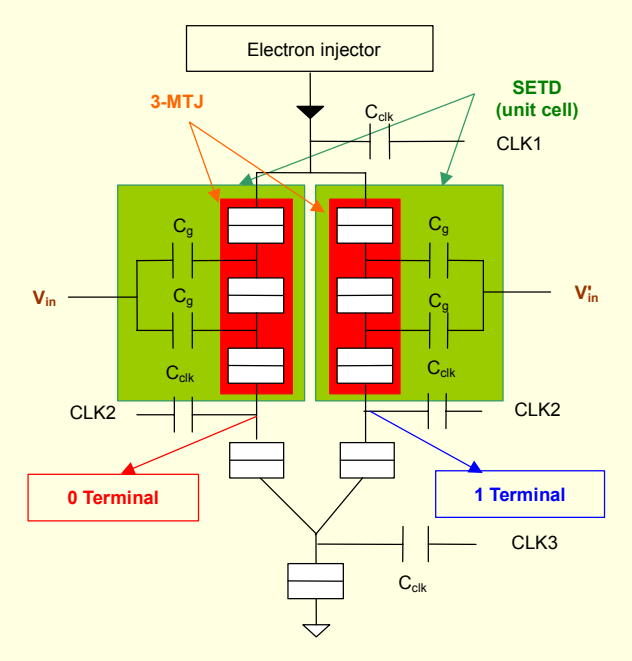

Fig. 1. Equivalent circuit of the SEPTL inverter using two 3-MTJs.

Figure 1 shows an equivalent circuit of the SEPTL inverter using two 3-MTJs. C_g and C_T are the gate and tunnel capacitances of the SETD, R_T is the tunnel resistance, C_{clk} is the clock capacitance, V_{clk} is the clock voltage, and V_{in} is the input voltage. The bias conditions determined under the MTJ are stable, and multiphase clocking schemes are used for precisely controlling electron flow.

Parameters of the unit cell such as the number of tunnel junctions, tunnel resistance, and voltage gain are considered below. Figure 2 shows an error rate comparison of SEPTL when the SETD is composed of either 2-MTJs, 3-MTJs, or 4-

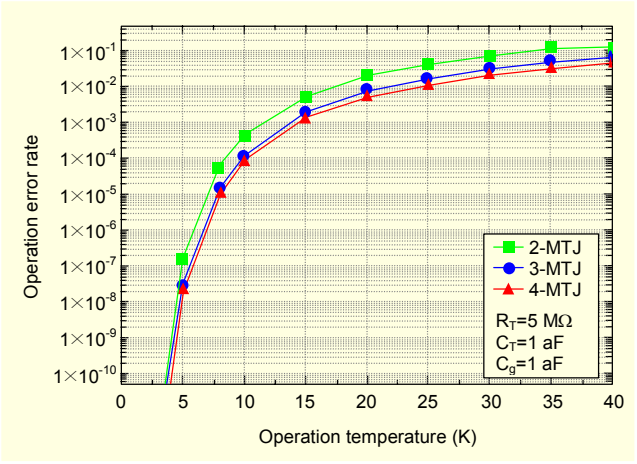

Fig. 2. Error rate comparison of the SEPTLs when the SETD is composed with either 2-MTJs, 3-MTJs, or 4-MTJs.

MTJs. MTJs may allow for the operation of logic circuits at a substantially higher temperature, scaling roughly as $\sqrt{N}$ (N: the number of tunnel junctions) [7]. The parameter margins for MTJs with three or more tunnel junctions are also considerably better than that for the 2-MTJ. So, by increasing the number of tunnel junctions, we expect to reduce the operation error. Also, cotunneling [7] may play an important role in logic families in which the digital information is coded by a single electron; hence, a single undesirable cotunneling event may lead to an error. On the contrary, cotunneling is much less important in the MTJ system because the cotunneling contribution decreases with the increase in junction resistance. In the present calculation, the cotunneling effect is ignored for simplicity. Though the MTJs have an advantage in the operation temperature, the use of more than three tunnel junctions adds a very slight contribution in the increase of the circuit's working temperature. Therefore, we opt for 3-MTJs.

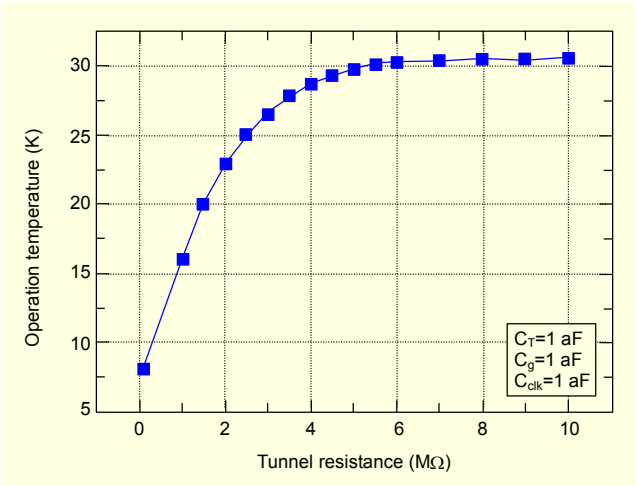

Fig. 3. Dependence of the operation temperature on the tunnel resistance.

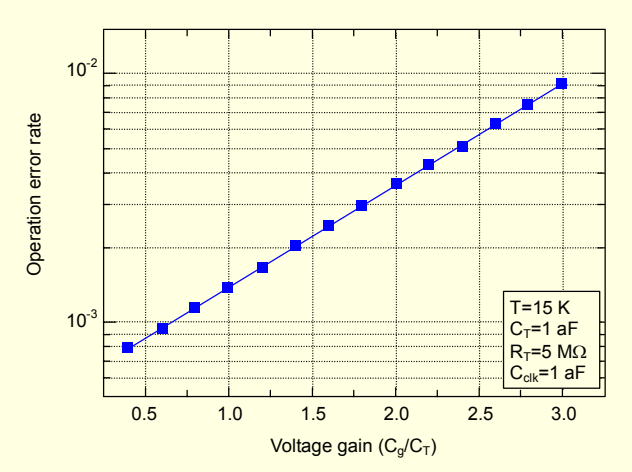

Fig. 4. Dependence of the error rate on the voltage gain.

Figure 3 shows the dependence of the operation temperature on tunnel resistance. The thermal characteristic of SEPTL is improved with an increase of tunnel resistance. But, when the tunnel resistance reaches 5 MΩ, the improvement is saturated. Moreover, a large tunnel resistance needs an additional bias voltage enhancement and leads to a slower circuit. Therefore, we take the proper tunnel resistance value, 5 MΩ.

Figure 4 shows the dependence of the error rate on the voltage gain (=C_g/C_T) at a fixed tunnel capacitance. The large voltage gain deteriorates thermal immunity exponentially due to the large total capacitances. However, as SEPTL doesn't require a large fan in/fan out, the voltage gain can be low.

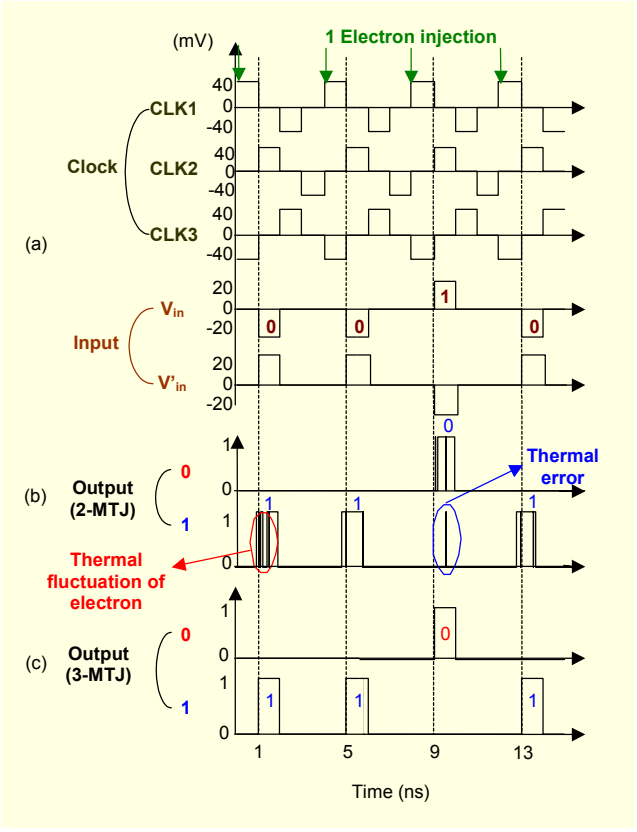

Fig. 5. Simulation results of the MTJ-SEPTL inverter: (a) sequential operation of the clocks and input voltages, (b) output characteristics of the 2-MTJ SEPTL at 10 K, and (c) output characteristics of the 3-MTJ SEPTL at 15 K.

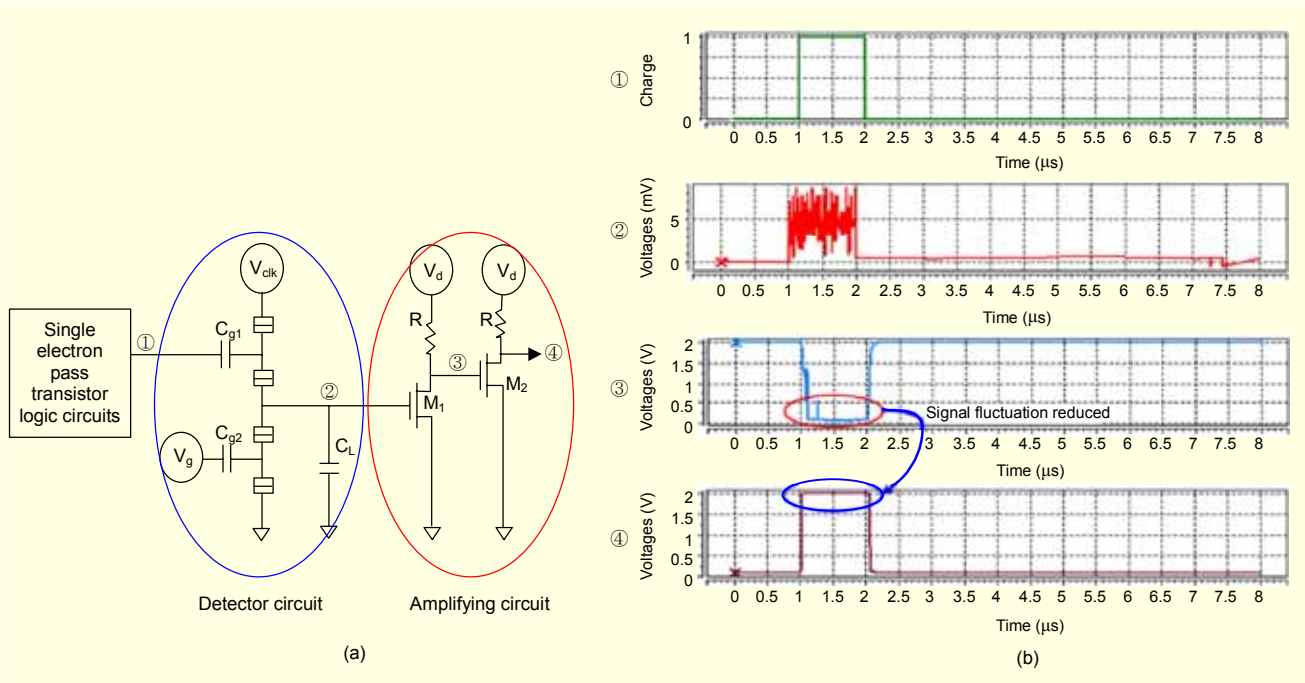

Fig. 6. The hybrid circuit simulation results: (a) equivalent circuit, (b) output characteristics at each output node.

Therefore, we settled on a voltage gain of 1.

Figure 5(a) shows the sequential operation of clocks and input voltages, while the characteristics of the output terminals using 2-MTJs at 10 K and 3-MTJs at 15 K are shown in Figs. 5(b) and 5(c). The parameters used are $C_g=C_{clk}=C_T=1$ aF, $R_T=5$ MΩ, $V_{clk}=40$ mV, and $V_{in}=20$ mV. As shown, the thermal operation error (near 9 ns) and the thermal fluctuation of the electron (at every output state) are observed when 2-MTJs at 10 K are used. On the other hand, when 3-MTJs are used, the error signal is not detected.

Figure 6 shows the cascade connection of SEPTL, the detector, and the amplifying circuit. A SPICE-compatible SET model is used to simulate SETD/MOSFET hybrid circuits [8]. The detector circuit senses the charge state output (①) and translates this signal to the voltage stage output (②). Though it has the voltage state output, this signal is very small (up to 5 mV) and noisy. The MOSFET circuits rectify the signal fluctuation and amplify the voltage level. Therefore, we can get a clear and stable voltage state output (④). The detector circuit parameters are $C_{g1}=C_{g2}=C_T=1$ aF, $R_T=10$ MΩ, $C_L=60$ aF, and T=10 K. The threshold voltages of MOSFET M1 and M2 are 0 V and 1.55 V, respectively. With hybridization, we can transform the charge state logic to a voltage state logic and guarantee a stable operation of the SETD logic circuits.

III. Conclusion

In summary, we proposed the SEPTL inverter employing 3-MTJs and adjusted the low temperature operation condition to reduce the error rate. The proposed 3-MTJs structure suppresses the fluctuation of electrons. The operation temperature was increased to 15 K using parameters $C_g=C_T=C_{clk}=1$ aF, $R_T=5$ MΩ, $V_{clk}=40$ mV, and $V_{in}=20$ mV. Also, the SETD/MOSFET hybrid circuit alleviates the thermal fluctuation of the electron translating the charge state logic to a voltage state logic. This designed logic architecture will be suitable for high density and low power integrated logic circuits in the future nanotechnology era.

References

[1] D. Averin and K.K. Licharev, *Mesoscopic Phenomena in Solid*, Elsevier, Amsterdam, 1991, pp. 173-271.

[2] Y. Ono and Y. Takahashi, "Single-Electron Pass-Transistor Logic: Operation of Its Elemental Circuit," *Int'l Electron Device Meeting*, 2000, pp. 297-300.,

[3] C.S. Lent, P.D. Tougaw, and W. Porod, "Bistable Saturation in Coupled Quantum Dots for Quantum Cellular Automata," *Appl. Phys. Lett.*, vol. 62, 1996, pp. 912-923.

[4] K. Uchida, K. Matsuzawa, and A. Toriumi, "A New Design Scheme for Logic Circuits with Single Electron Transistors," *Jpn. J. Appl. Phys.*, vol. 38, 1999, pp. 4027-4032.

[5] N. Asahi, M. Akazawa, and Y. Amemiya, "Single-Electron Logic Device Based on the Binary Decision Diagram," *IEEE Trans. Elec.*, vol. 44, no. 7, 1997, pp. 1109-1116.

[6] J.R. Tucker, "Complementary Digital Logic Based on the Coulomb Blockade," *J. Appl. Phys.*, vol. 72, 1992, pp. 4339-4413.

[7] R.H. Chen and K.K. Likharev, "Multiple-Junction Single-Electron Transistors for Digital Applications," *Appl. Phys. Lett.*, vol. 72, 1998, pp. 61-63.

[8] B.H. Lee and Y.H. Jeong, "A Novel SET/MOSFET Hybrid Static Memory Cell Design," *IEEE Trans. Nanotech.*, vol. 3, 2004, pp. 377-382.