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High Performance of SWIR HgCdTe Photovoltaic Detector Passivated by ZnS

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Abstract

Short wave infrared (SWIR) photovoltaic devices have been fabricated from metal organic vapour phase epitaxy (MOVPE) grown n- on p- HgCdTe films on GaAs substrates. The MOVPE grown films were processed into mesa type discrete devices with wet chemical etching employed for meas delineation and ZnS surface passivation. ZnS was thermally evaporated from effusion cell in an ultra high vacuum (UHV) chamber. The main features of the ZnS deposited from effusion cell in UHV chamber are low fixed surface charge density, and small hysteresis. It was found that a negative flat band voltage with –0.6 V has been obtained for Metal Insulator Semiconductor (MIS) capacitor which was evaporated at 910°C for 90 min. Current-Voltage (I-V) and temperature dependence of the I-V characteristics were measured in the temperature range 80 – 300 K. The Zero bias dynamic resistance-area product (R_0A) was about 7500 Ω-cm^2 at room temperature. The physical mechanisms that dominate dark current properties in the HgCdTe photodiodes are examined by the dependence of the R_0A product upon reciprocal temperature. From theoretical considerations and known current expressions for thermal and tunnelling process, the device is shown to be diffusion limited up to 180 K and g-r limited at temperature below this.

Key Words : SWIR, MOVPE, HgCdTe, ZnS passivation, infrared detector

1. Introduction

Short Wavelength Infrared (SWIR) (1 – 3 μm) HgCdTe photovoltaic (PV) detectors have been developed for years owing to their important application in many fields such as optical fiber communication, aviation remote sensing, and earth resource exploration. Recently, there have been some reports and papers concerning this kind of detectors[1-3].

However, the number of studies on SWIR HgCdTe IR detectors and their properties are still small. In this paper, we would like to investigate some features of SWIR detectors such as diode characteristics, contact resistance. This work was concentrated especially on passivation of SWIR HgCdTe photovoltaic detectors.

The passivation layer plays very important and dominant roles in determining HgCdTe device performance. HgCdTe surface passivation is of complex nature because of the compound nature of HgCdTe, the difference in the chemical properties of the constituents, and the tendency of electrically active defects to form in the interface region during the passivating process. Furthermore, due to the extreme temperature sensitivity of bare HgCdTe surface, passivation treatments and deposition processes should be performed at near room temperature. In order to have good passivation characteristics, interfaces should have low interface state density, low fixed charges, thermal stability, high dielectric breakdown strength, good insulation, large band gap, good adhesion and chemical stability. Because HgCdTe is the narrow band gap semiconductor, the surface potential band bending is often of the order of the band-gap energy and it can easily accumulate, deplete, or invert the surface significantly, thus drastically affecting device performance.

Hence, the development of good passivation layer and its processing technique is essential for the further improvement of device performance. Up to now, there have been a lot of results reported on passivants for HgCdTe devices[4-5]. An excellent review of HgCdTe

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native and deposited insulators useful for HgCdTe device passivation was published by Nemirovski and Bahir[6]. This review is concerned about some passivants such as ZnS, SiO_2 and SiN_x as well as the methodologies suitable for these passivants. ZnS is one of the most widely used materials for HgCdTe passivation because its adhesion on freshly etched HgCdTe surfaces is excellent, and it has very low fixed surface charges at the interface as well as very good insulating properties.

In this paper, we report our experimental results on SWIR HgCdTe passivation and its device performance. The experimental results are concerned about the dynamic-resistance-voltage characteristics of $Hg_{1-x}Cd_x$ Te n- on p- photodiode with $x = 0.53$. Besides that, Capacitance-Voltage (C-V) characteristic was also measured to determine the quality of the ZnS layer which was deposited in UHV chamber.

2. Experimental Procedure

We followed the same sequence of HgCdTe growth method as in our previous reports[7,8]. The Interdiffused Multilayer Process (IMP)[9] was used to grow HgCdTe. The (001) GaAs wafer with 4° off oriented toward <100> was rinsed in KOH containing water solution to suppress hillock formation[10]. Dimethyl cadmium (DmCd) and diisoprophyl telluride (DiPTe) were used as precursors for Cd and Te, respectively. A CdTe buffer layer 5 μm thick was grown on the substrate first and either a p-type HgCdTe single layer or an n-on-p HgCdTe diode structure was grown on the top of it. Iodine donor and arsenic acceptor doping were carried out with isopropyl-iodide (IPI) and tris-dimethyl amio-arsenic (DMAAs), respectively. In order to make a SWIR diodes, the following methodology was used. 5 μm thick p-type layer was grown first and 1 μm thickness of iodine doped n-type layer was grown on top of it. Then, the HgCdTe wafer was annealed at Hg-saturated condition for arsenic activation and removal of Hg vacancies.

To make SWIR diodes, the top n-type cap layer were mesa etched by HBr solution to a depth of over 2 μm, which is deep enough to reach the p-layer. Then dummy etching was carried out to make a clean surface before loading the substrate into the chamber. About 4000 Å thick ZnS was deposited in UHV chamber. Indium (In) and gold (Au) were used to make ohmic contact with n and p HgCdTe, respectively.

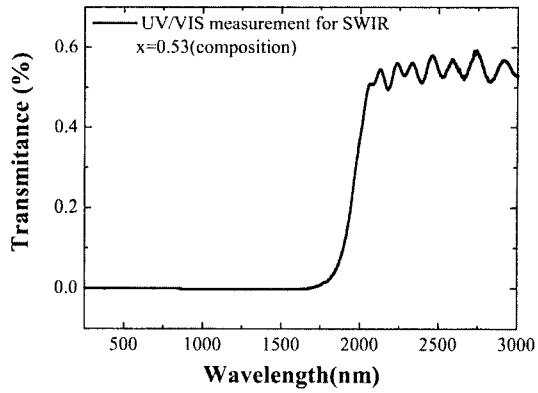

Fig. 1. UV/VIS measurement for HgCdTe SWIR n-on-p junction at room temperature.

I-V characteristics of SWIR diodes were measured by using Keithley 236 source measure unit. Dark current mechanism was investigated by measuring the temperature dependence of I-V. The MIS structures were fabricated to estimate the interface properties as well as insulating properties of ZnS layer on HgCdTe. The C-V characteristics were measured by Keithley 590 C-V analyzer.

3. Results and Discussion

Using a UV/VIS spectrometer, we determined the cut off wavelength of HgCdTe layers. We could determine the alloy composition x of $Hg_{1-x}Cd_xTe$ with the cut off wavelength measurement. Fig. 1 is the UV/VIS transmittance spectrum of MOVPE grown HgCdTe n on p junction. The cut off wavelength is about 1.9 μm at room temperature. By using Finkman and Schacham[11] method, the alloy composition x was calculated, which is about 0.53 for this wafer. To determine the carrier concentration and mobility of this substrate, the van der Pauw Hall measurement was used. The carrier concentration and mobility of p-type absorber layer were obtained after stripping the top n-HgCdTe layer. They were about 5×10^{16} hole/cm^3 and 80 cm^2/vs, respectively.

The insulating layer of the MIS devices was formed by thermally deposited ZnS in UHV chamber. The deposition time was varied from 50 to 90 min at constant source temperature of 910°C. The gate electrodes of

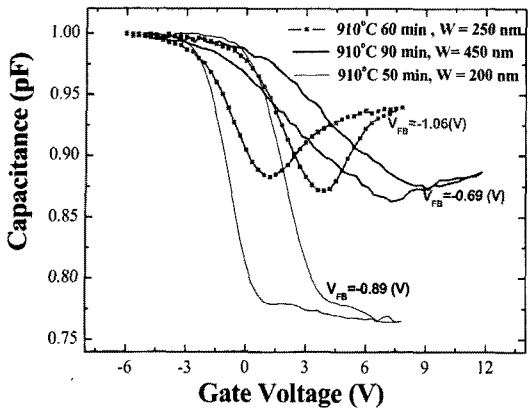

Fig. 2. The C-V characteristics for MIS device measured at 77 K with 1 MHz.

500 μm diameter were patterned using the thermal evaporation of Au through a metal mask. Fig. 2 shows the measured C-V characteristics of MIS devices.

As shown in Fig. 2, we have got three different shapes of C-V characteristics. For the first case, passivated for 90 min, it shows the high frequency C-V characteristics. The surface of p-HgCdTe is slightly inversed with flat band voltage (V_{fb}) of –0.69 V. If work function differences are ignored, this value correspond to a interfacial positive fixed charge of 7×10^{10} cm^{-2}. In this sample, the voltage stretch-out is larger than that of other two curves. This means that the fast interface state density is larger than that in other case. In the second case, passivated for 50 min, it also shows high frequency C-V characteristics. The surface of this sample is also slightly inversed with flat band voltage of –0.89 V. The voltage stretch-out does not occur in this one but the hysteresis loop width at the flat band voltage is 2.4 V. This means the slow interface state density is larger than other two ones. The last one revealed a low frequency C-V characteristics. The surface of this sample is also slightly inversed with flat band voltage of –1.0 V.

From Fig. 2, the V_{fb} of three cases are almost the same that means fix charge in three cases doesn't change much during the time for evaporation. But degree of voltage stretch-out in the curve is increased with evaporating time. It is considered that ZnS passivation layer was affected by thermal duration heat during the time for evaporation. Thus, cooling for substrate holder have to be needed to obtain a good passivation layer for HgCdTe. The thickness of ZnS layer (W) was calculated from the following equation.

$$W=\frac{\varepsilon A}{C_{max}} \tag{1}$$

Where, C_{max} is the maxium capacitance of MIS structure, is relative dielectric constant of ZnS ($\varepsilon=7.45$), and A is the device area ($A=1.96\times10^{-3}$ cm^2).

To make a good passivation, the flat band voltage (V_{fb}) should be close to the ideal value (V_{fb}=0) as much as possible. In addition to that, the thickness of insulating layer must be thick enough to get a step coverage at the mesa structure. Therefore, the first condition (passivated in 90 min at 910°C) is selected for our device, because flat band voltage in this condition is the smallest and the thickness of passivation layer is thick enough, even though voltage stretch-out is big.

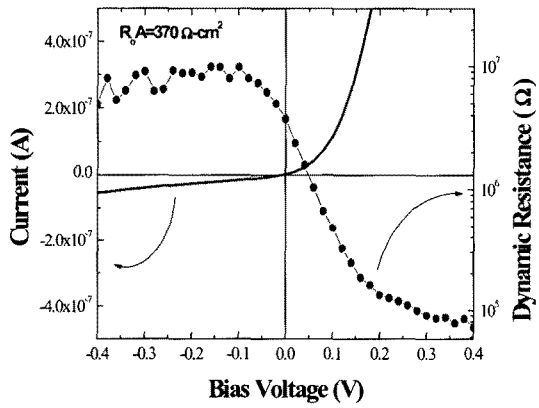

Fig. 3. The I-V characteristic and dynamic resistance of diodes for 4 min mesa etched sample.

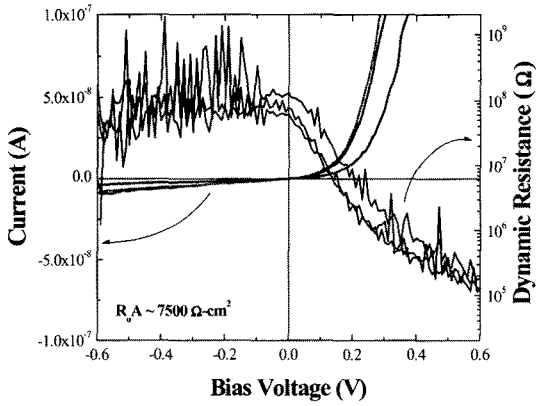

Fig. 4. The I-V characteristics and dynamic resistance of diodes for 2 min mesa etched sample.

In order to investigate the photodiode performance, the I-V characteristics were also measured at room temperature. I-V characteristics for two diodes processed with different etching times were measured and shown in Fig. 3 and 4, respectively. In Fig. 3, the I-V and dynamic resistance of the diode processed with etching time of 4 min are shown, with R_0A product of about 370 Ω-cm^2.

Fig. 4 shows the I-V result of SWIR diode processed with etching time of 2 min. The R_0A product was about 7500 Ω-cm^2 at room temperature.

Actually, these two diodes were fabricated by using the same processing sequence. The only difference between them was mesa-etching time. We can explain the different result for these two diodes as follows. For the first diode, the mesa depth is quite deep (about 45 μm) so that ZnS might not have been deposited uniformly over all the surface area of the diode with some limitation for diode performance. For the second diode, the mesa depth is around 2 μm that might have resulted in homogeneous deposition of ZnS.

The zero bias resistance-area R_0A product is an importance figure of merit characterizing the performance of HgCdTe photovoltaic detectors. Fig. 5 shows the R_0A versus reciprocal temperature plots for a typical SWIR photodiode processed by the above-mentioned process in the temperature range of 80 – 300 K compared with the temperature dependence of diffusion current (broken line) and generation-recombination (g-r) current (solid line).

As shown in Fig. 5, in the high temperature region (T > 180 K), R_0A product is governed by diffusion current (the broken line).

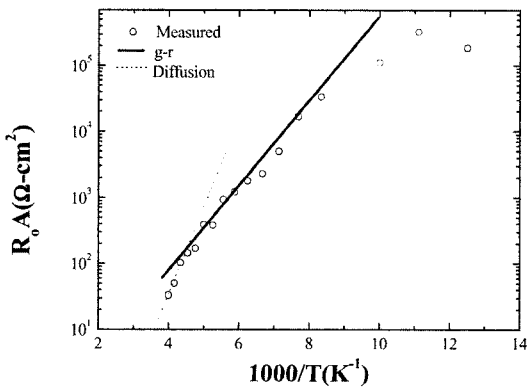

Fig. 5. R_0A product versus 1000/T for second n-on-p HgCdTe SWIR photodiode.

In the intermediate temperature region (100 K < T < 180 K) the R_0A product is governed by g-r current (solid line), while in the low temperature region (T < 100 K) R_0A product has a weak temperature dependence and a considerable deviation from thermal current limit. The deviation from thermal current limit in the low temperature region may be due to the dark current.

4. Conclusion

This work has demonstrated the excellent performance of our SWIR n-on-p HgCdTe mesa photodiode. The R_0A value at room temperature is 7500 Ω-cm^2. This value is bigger than that of planner photodiodes fabricated by ion implantation technique from MBE grown HgCdTe on CdZnTe substrates. This result can be explained in terms of insulating property and step coverage. It has been reported that ZnS has high insulating property compare to CdZnTe. In our SWIR diodes, high insulating property and step coverage are decisive factor to determine a diode performance. Therefore, high insulating property and good step coverage are needed to obtain a good performance of SWIR HgCdTe diodes. This result is different from the case in MWIR and LWIR HgCdTe diodes, where the interface propertis are dominant factor to determine diodes performance.

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