The scheme to implement Rate Adaptive Shaper for Differentiated Service Network – srRAS and G-srRAS –

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Abstract—This paper has addressed the implementation of the single rate Rate Adaptive Shaper(srRAS) described in RFC2963. This shaper has been proposed to use at the ingress of differentiated services networks providing Assured Forwarding Per Hop Behavior (AF PHB).

srRAS is typically used in conjunction with single rate Three Color Marker(srTCM) described in RFC2697. srRAS itself is the tail-drop FIFO that is drained at a variable rate, and srTCM is the marker with metering function. G-srRAS is the same as srRAS except that RAS receives the green token state information from the downstream srTCM to avoid delaying a packet in RAS although there are sufficient tokens available to color the packet green.

In this paper, we have addressed the algorithm and the architecture of srRAS, and the scheme to implement srRAS using VHDL(Very high-speed integrated circuit Hardware Description Language) and its related tools.

Index Terms—Single rate Rate Adaptive Shaper(srRAS), srTCM(single rate Three Color Marker), Assured Forwarding Per Hop Behavior (AF PHB). Differentiated Service CodePoint(DSCP)

I. INTRODUCTION

Recently, with growing new application services that requires Quality of Service(QoS) guarantee, Internet Protocol(IP) QoS become one of the most important issues in next generation Internet. In IP network, in order to provide all users with the diverse QoS satisfactorily while using network resources effectively, traffic regulation function at network edge is necessary. Shaping is to control burst data or traffic rate to send data streams according to the traffic profile. If a flow does not conform to the traffic profile, shaping function can be used to delay non-conforming traffics until they conform to the profile.

srRAS described in RFC2963 is the shaper used in conjugation with downstream srTCM. it is tail-drop First Input First Out (FIFO) queue that is drained at a variable rate. srTCM meters IP packet streams from srRAS and marks its packets to be either green, yellow, or red. This shaper has been proposed to use at the ingress of differentiated services networks providing AF PHB. And then srRAS can reduce the burstiness of the upstream traffic of srTCM. By reducing the burstiness of the traffic, srRAS increases the percentage of packets marked as green by the downstream srTCM.

srTCM consists of meter and marker. Meter measures the instantaneous properties of the selected packets streams according to a traffic profile specified in a Traffic Conditioning Agreement(TCA), and then passes the metering result and the packet to the marking function to trigger a particular action for each packet, which is either in-profile or out-of-profile. Marker sets the Differentiated Service (DS) field of a packet to a particular codepoint, adding the marked packet to a particular DS behavior aggregate.

G-srRAS is the same as srRAS except that it receives the amount of green tokens from the downstream srTCM to avoid delaying a packet in srRAS although there are sufficient tokens available to mark the packet green.

This paper is organized as follows. In section 2, we describe Estimated Arrival Rate (EAR), the departure time, and shaping rate of both srRAS and G-srRAS described in RFC2963. In section 3, we address the parameters and the operation of srTCM. And in the section 4, the marking scheme in differentiated networks has been addressed. In section 5, we conclude this paper.

II. RATE ADAPTIVE SHAPER

The main objective of the shaper is to produce the output traffic that is less bursty than the input traffic. And rate shaping is used to bound, or constrains the unpredictability of a certain traffic class, and requires queues, queue management, and scheduling function.

In this section, we describe only two of four RASs (srRAS, trRAS, G-srRAS, and G-trRAS) described in RFC2963, srRAS and G-srRAS, which can be used in combination with the srTCM. srTCM is the marker based on token bucket. The only difference between srRAS and G-srRAS lies on whether the downstream srTCM informs srRAS of the green token information or not.

A. single rate RAS(srRAS)

Fig. 1 shows srRAS used in conjunction with srTCM. srRAS is set up by initially assigning values to four parameters. These parameters are two rates and two buffer thresholds. Two rates in bytes per second are Committed Information Rate (CIR) and Maximum Information Rate (MIR).

Two buffer thresholds in bytes are CIR_th (CIR_ threshold) and MIR_th (MIR_threshold).

Manuscript received July 24, 2003.

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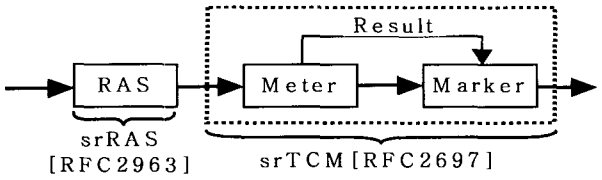

Fig. 1 srRAS model

As shown in Fig. 2, the shaping rate of srRAS is based on the average rate of incoming traffic and the instantaneous FIFO buffer occupancy.

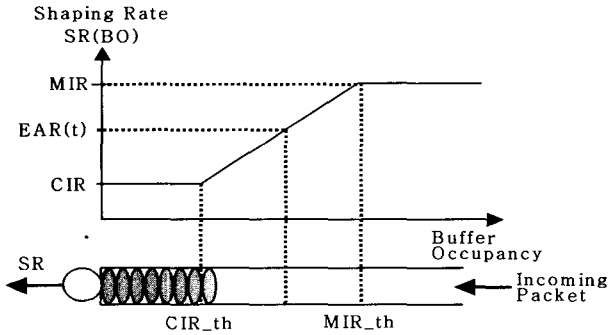

Fig. 2 Shaping Rate of RAS

The average rate can be computed by several means, but in this paper, we adapt the method used in [1][7]. The function of the arrival rate is as follows.

EAR(t)=[1-exp(-T/K)*L/T]+exp(-T/K)*EAR(t-1)

Where EAR(t) is the updated Estimated Arrival Rate, EAR(t-1) is the previous value of the Estimated Arrival Rate, T is the time passed since the previous packet arrives, L is the size of arrival packet, and K is constant for filtering out the estimation inaccuracies due to exponential smoothing. Another factor is the instantaneous FIFO buffer occupancy of srRAS. The relationship between the buffer occupancy and the shaping rate is as follows.

1) For buffer occupancy<CIR_th,
   SR(BO)=max(EAR(t),CIR),
   BO=Buffer Occupancy
2) For CIR_th≤Buffer Occupancy<MIR_th,
   SR(BO) = max(EAR(t), F(BO)),
   F(BO)=CIR +
   ((MIR-CIR)/(MIR_th–CIR_th))*(BO–CIR_th)
3) Buffer Occupancy≥MIR_th,
   SR(BO) = MIR

In srRAS, a time schedule T1 is based on the output rate(=shaping rate) in srRAS. T1 is the time that the packet at the head of the queue of srRAS is to be released from the srRAS.

For CIR ≤ EAR(t) ≤ MIR, $T1 = t + L_i^k/SR(BO)$, Where t is current time, L_i^k is the length of k^{th} packet for flow i, and SR(BO) is the shaping rate(=output rate) of srRAS.

B. Green-single rate RAS(G-srRAS)

G-srRAS is the same as srRAS except that it receives the green token status information from srTCM shown in Fig. 3.

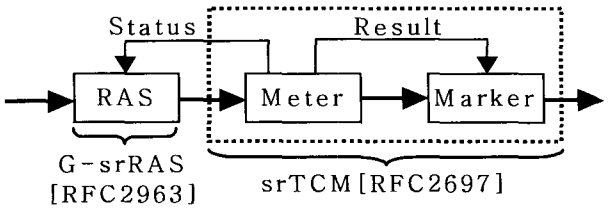

Fig. 3 G-srRAS model

In srRAS, the shaper is not aware of the status of the meter in srTCM. This entails that shaper can unnecessarily delay the packet although there are enough tokens available to mark the packet green.

G-srRAS solves this problem by coupling srRAS with the meter. The meter in srTCM informs srRAS of the green token status, and then srRAS can decide whether it sends the packet to srTCM immediately or not, according to the green token status. Therefore, the green packets can be released sooner than srRAS, and the delay in G-srRAS can be reduced.

Using the same method as srRAS, G-srRAS computes the time schedule when the packet at the head of G-srRAS queue is to be released.

G-srRAS is set up in the same way as the srRAS described in section A. And the shaping rate of G-srRAS is also calculated in the same way as srRAS. This shaping rate determines the same time schedule, T1. Another time schedule according to the green token state information from srTCM, T2, is calculated as the earliest time instant when the packet at the head of G-srRAS queue would be marked as green by srTCM.

$$T2=\max(t, t+(L - Bc(t))/CIR)$$

Where t is current time, L is the packet length in bytes at the head of G-srRAS queue, Bc(t) is the amount of green tokens in the token bucket of srTCM at t, and CIR in bytes per second is the Committed Information Rate of srTCM.

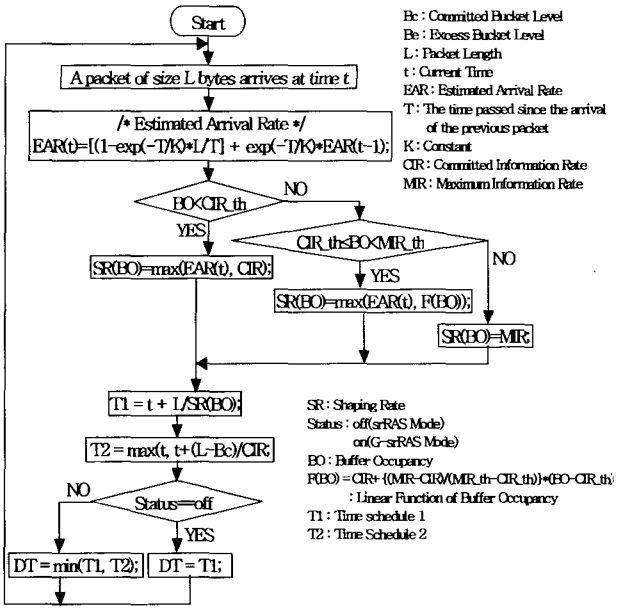

Fig. 4 Time Schedule Algorithm

If T2 is earlier than the release time computed from the current schedule time, T1, then the packet can be released at T2. Otherwise, the packet at the head of G-srRAS queue will be released at the time T1. Fig. 4 shows this time schedule algorithm for both srRAS and G-srRAS. When a packet arrives at the head of srRAS(or G-srRAS) queue, in the case of srRAS, it will leave this queue at DT=t1, and in the case of G-srRAS, it will leave this queue at DT=min(T1, T2) from G-srRAS. Therefore, the advantage of G-srRAS is to have the green packets departing sooner, thus reduce the delay in G-srRAS, and increase the probability of a green packet.

III. SINGLE RATE THREE COLOR MAKER

The srTCM meters an IP packet stream, and marks its packets green, yellow, or red. Marking in srTCM is based on three parameters, CIR, CBS, and EBS.

Fig. 5 shows srTCM described in RFC2697. srTCM consists of meter and marker. Meter consists of two token buckets, c and e. The function of meter is to meter each packet, and then pass the packet and the metering results to the marker. The function of marker is to set the Differentiated Service(DS) field of a packet to a particular codepoint according to the metering result.

srTCM is configured by assigning values to the three parameters CIR, CBS, and EBS in initial time.

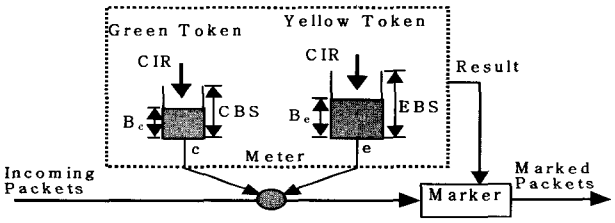

Fig. 5 srTCM model

Fig. 6 is token bucket update algorithm of meter in srTCM.

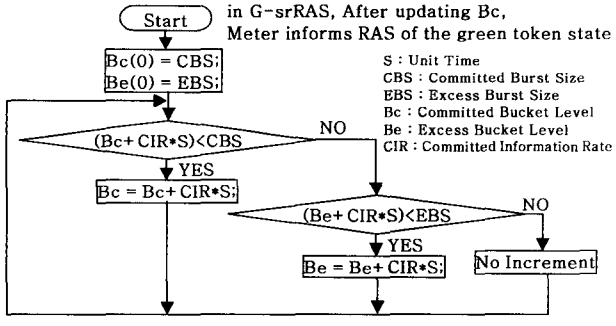

Fig. 6 Token counter update operation in srTCM

This algorithm is specified in terms of two token buckets c and e, which both share the common token generation rate, CIR. Two burst size CBS and EBS are measured in bytes. At least one of them must be larger than zero. Each burst size is related to each token bucket size. The maximum size of the token bucket c is CBS and the maximum of the token bucket e is EBS. Initially, the levels of two buckets, Bc and Be are assigned to Bc(0)=CBS and Be(0)=EBS respectively. And then the updating of Bc and Be is done with CIR as shown in Fig. 6.

Fig. 7 shows the metering algorithm in srTCM. The algorithm is done in two different modes, and set in the initial time. In color-blind mode, the meter assumes that the incoming packet stream is uncolored. In this mode, all packets are processed in the same method. In the color-aware mode, the meter assumes that the incoming packet stream has been pre-marked as green, yellow, or red. In this mode, the packet is additionally processed in different method based on its color. In Fig. 7, L is the size of packet and measured in bytes. Bc and Be are level of each bucket and also measured in bytes.

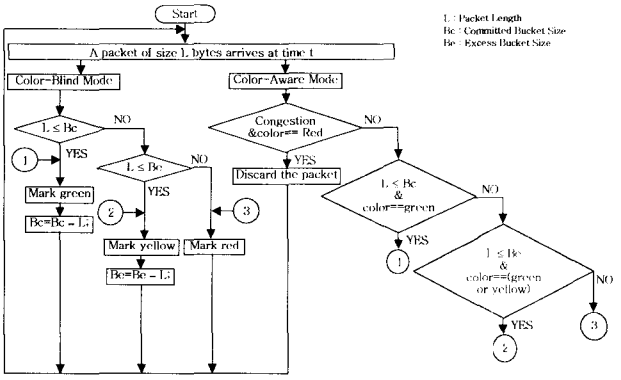

Fig. 7 Metering function in srTCM

IV. MARKING SCHEME OF srTCM

In Differentiated Services Networks, besides the existing Best-Effort(BE) service, there are two others kind of service, Assured Forwarding (AF) service and Expedited Forwarding(EF) service. Internet Engineering Task Force (IETF) has addressed the difference between Best-Effort service and two services using the specific byte in IP header.

In IPv4, packets have always contained a Type of Service (ToS) byte to allow simple, per-hop packet classification. Fig 8 a) shows the ToS byte in IPv4 header. In this format, the lower 3 bits present the packet's precedence, the upper 4 bits present the desired type of routing metric information, and the last bit is set to zero for reserved use. DS(Differentiated Service) field shown in Fig 8 b) has replaced these functions. DSCP (DS Code Point) is an extension to 3bits used by IP precedence. Like IP precedence, DSCP can be used to provide differential treatment to the appropriately marked packets.

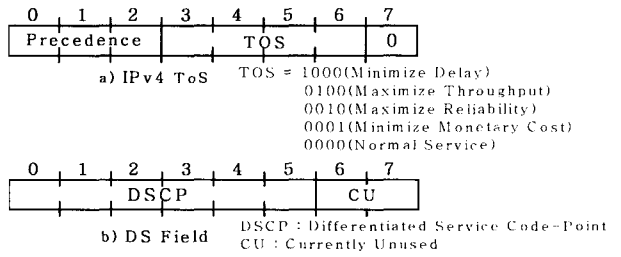

Fig. 8 TOS and DSCP

The marking in srTCM reflects the metering results by setting the DS field of the packet to a particular codepoint. In case of the AF PHB, the color can be coded as the drop precedence of the packet. AF codepoint value is recommended in RFC2597 as shown in Table 1. It defines four AF traffic classes, with each service class having three-drop precedence levels. Each AF traffic class is services in its own queue, enabling independent capacity management like Weighted Fair Queuing(WFQ) for the four traffic classes. Within each AF class, there are three-drop precedence levels having queue management like Random Early Detection (RED). AF codepoint consists of total 6 bits, where upper 3 bits presents the class for the packet, and lower 3 bits presents the drop precedence level within the corresponding class.

Table 1 AF Codepoint and Their Color Code

Dropping Precedence	Class1	Class2	Class3	Class4	Color
LOW	001010	010010	011010	100010	Green
Medium	001100	010100	011100	100100	Yellow
High	001110	010110	011110	100110	Red

V. ARCHITECTURE AND OPERATION OF srRAS

A. The architecture of srRAS

Fig. 9 shows the architecture of IP shaper consisting of srRAS and srTCM. This shaper is different from the shaper for ATM because of variable packet length. So the address management of memory is different from that of ATM. But another operation is similar to that of ATM.

srRAS consists of input interface&IP header extractor block, searching function block, lookup table block, timing control block, queue control block and DT calculator block, generates the appropriate address to read(write) packets from (to) the packet memory.

srTCM also consists of the token metering block and the marking function&output interface block. The token metering block consists of the token update function and the metering function.

Token update function consists of two token buckets, green token bucket and yellow token bucket. The token generation rate of both buckets is CIR. The metering function the necessary signals to exchange DSCP field to the new color value. This signal is used in the marking function&output interface block.

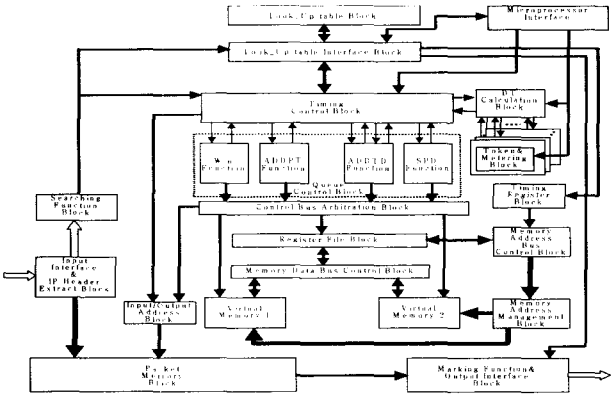

Fig. 9 The architecture of RAS

In this architecture, the virtual memories are divided into three major queues. First, packets that belong to the same flow are linked together in a logical queue, called the flow queue. Second, packets that have the same time stamp (DT : Departure Time) are linked together in the timing queue. Third, packets whose departure time is due or overdue are linked together in the departure queue.

The contents in the flow queue are the address of packets stored in packet memory. The contents of both the timing queue and the departure queue are FID(Flow Identifier) values. There is also an idle-address linked list (IALL) that keeps the available space of the packet memory. Queue control block generates the necessary signals that are used to access all logical queues.

Table 2 shows the virtual memory architecture of srRAS that we will consider. It consists of address management RAM(AD RAM), Flow queues(Flow RAM), Timing queues(Timing RAM), departure queues(departure RAM), and their registers.

Table 2 Memory Architecture

	AD RAM	Flow RAM		Timing RAM		Departure RAM	
RAM	AD RAM	FHP	FTP	THP	TTP	FID	NP
Reg.	ADB	FHTB	FHPB	THPB	TTPB	FID	NPB

Fig. 10 shows the virtual memory map according to memory architecture. We will consider only 16 flows because of per-flow treatment for srTCM and srRAS on one FPGA chip. Size of virtual memory1 is 4131x16, and Size of virtual memory2 is 2083x16. The reason why we uses the separate virtual memories is to access the memories simultaneously, and then save the time. Total memory size is 6214 x 16 and implemented on one FPGA chip. srTCM is also implemented based on per-flow so that we consider only 16 srTCM. Packet memory is implemented using commercial chip.

Virtual Memory 1		Virtual Memory 2	
Block	Size	Block	Size
THPB	2k X16	TTPB	2k X16
ADB	2k X16	NPB	16 X 16
FHPB	16 X 16	FTPB	16 X 16
FIB	16 X 16	IFTPB	1 X 16
IFHPB	1 X 16	IATPB	1 X 16
IAHPB	1 X 16	DTPB	1 X 16
DHPB	1 X 16		

Fig. 10 Virtual Memory Map

B. The operation and the performance of srRAS

Timing control block arbitrates Win function, ADDTD function, ADDPT function, and SPD function, of queue control block, and then generate the necessary to control the virtual memories and the packet memory.

In Win function, Newly arriving packets are appended to corresponding flow queue according to their FID values. In ADDPT function, when a packet becomes the HOL(Head of Line) packet of flow queue, it will be assigned a departure time from DT calculator block and join a timing queue. In ADDTD function, As the real time ticks, the timing queue whose DT is equal to RT(Real Time) will become the departure queue or be appended to the tail of the departure queue, dependent on whether or not the departure queue is constructed. In SPD function, The HOL packet of the departure queue is read out. Its content, FID is then used to access the HOL packet of the corresponding flow queue, where the packet address is obtained to transmit the packet in the packet memory.

Fig 11 shows the operation of queue control block in srRAS. It consists srRAS and srTCM whose operations are parallel. Each function of queue control block according to Fig 10 is shown in table 2. As the bottleneck of srRAS operation is the time for calculating the DT from DT calculator block, another many operations can be performed during DT calculation.

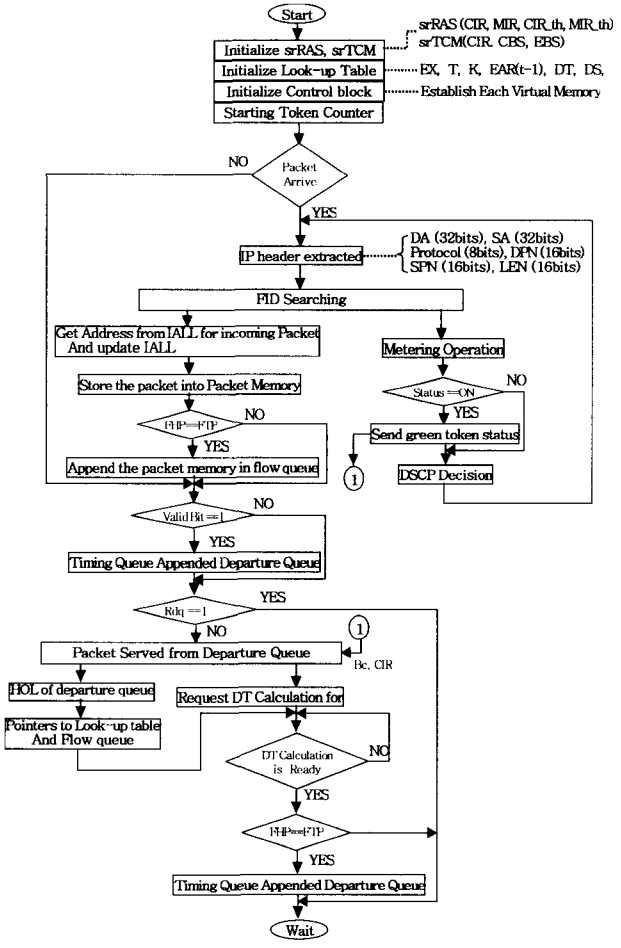

Fig. 11 Operation Flow of srRAS

Now we will consider quantitative analyses for RAS design, which can evaluate the performance of srRAS. Four parameters for design are memory size and it's structure, the number of clock cycles, clock rate, and DT calculation time.

Table 3 Processing Time of each block

block	Operation	Time
Decision	*Decide according to conditions*	6T
Win	*Write FID to flow queue*	8T
ADDPT	Send FID from flow queue to timing queue	7T
ADDPD	Send FID from timing queue to departure queue	7T
SPD	Read FID from departure	9T
	Read packet from packet memory according to FID	9T
Total		46T

Table 3 shows the clock required in each function block of queue control block. We must consider the total clock of each control block plus DT calculation ready time. In this architecture, we will consider 50MHz clock cycle(20ns) for stable action in FPGA. Therefore the performance of srRAS is dependent of DT calculations delay time.

VI. CONCLUSION

In this paper, we have addressed the scheme to implement srRAS. It is different from shaper of ATM because of variable packer length. This shaper performs the shaping function, and then the marking function for each packet based on RFC2963. The device is the shaper designed to use in conjunction with meters such as srTCM. In this architecture, IP shaper mainly consists of a packet memory, a register, a flow identifier searching function, a DT calculator, a look-up table, virtual memories and Timing and queue control block.

Timing and queue control block of these components is key elements in this architecture. Virtual memory consist of three parts, flow part, timing part, and departure part. Each memory part may contain a number of logical queues, and that logical queue is operated by the concept of linked queue. Timing and queue control block generates the necessary signal that are used to access all logical queues, and the appropriate address to read/write a packet from/to the packet memory.

Microprocessor doesn't play a many role in this architecture because of processing and accessing time. It sets the initial values of parameters. The calculation of the departure time of arriving packet, and the decision of packet's color are done in another block. Packet memory uses commercial memory to store the arriving packet. Using the necessary information of IP header in each packet makes flow identifier, and then this flow identifier is used internally in conjunction with the concept of linked queue.

In the near future, we will implement the IP shaper in FPGA using VHDL.

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