A 3 V 12b 100 MS/s CMOS D/A Converter for High-Speed Communication Systems

Min-Jung Kim, Hyuen-Hee Bae, Jin-Sik Yoon, and Seung-Hoon Lee

Abstract— This work describes a 3 V 12b 100 MS/s CMOS digital-to-analog converter (DAC) for high-speed communication system applications. The proposed DAC is composed of a unit current-cell matrix for 8 MSBs and a binary-weighted array for 4 LSBs, trading-off linearity, power consumption, chip area, and glitch energy with this process. The low-glitch switch driving circuits are employed to improve linearity and dynamic performance. Current sources of the DAC are laid out separately from the current-cell switch matrix core block to reduce transient noise coupling. The prototype DAC is implemented in a 0.35 um n-well single-poly quad-metal CMOS technology and the measured DNL and INL are within ±0.75 LSB and ±1.73 LSB at 12b, respectively. The spurious-free dynamic range (SFDR) is 64 dB at 100 MS/s with a 10 MHz input sinewave. The DAC dissipates 91 mW at 3 V and occupies the active die area of 2.2 mm x 2.0 mm

***Index Terms*— binary-weighted array, current-cell matrix, current-steering, digital-to-analog converter**

I. INTRODUCTION

Recently developed high-performance communication and image processing systems have requested both analog and digital circuits implemented on the same single chip, resulting in the concept of the so-called System-on-a-Chip. Data converters integrated in the interface of such mixed-mode systems have played more and more important roles with improved system performance. Particularly, on-chip high-speed high-resolution digital-to-analog converters (DACs) based on the same CMOS process as digital circuits are essential for system applications such as very high-data rate digital subscriber line (VDSL), direct digital synthesis (DDS), wireless local area network (WLAN), quadrature modulation (QAM), direct intermediate frequency (IF), and global system for mobile telecommunication (GSM), simultaneously to achieve low power, small chip area, and high speed performance. Conventional high-speed high-resolution CMOS DACs have employed a current-steering architecture with advantages of speed and linearity, while some performances have been degraded due to process variations, current-source mismatch, and high glitch energy at outputs[1]-[5].

The proposed DAC in this work consists of a unit current-cell matrix for 8 MSBs and a binary-weighted array for 4 LSBs to obtain high linearity at 12b level. In the unit current-cell matrix, a random switching scheme for 255 current cells is adopted to improve integral nonlinearity (INL), which can be degraded by the symmetrical error and the two-dimensional graded error of the DAC. The delay time difference of digital signals is minimized with the intermediate latches placed in front of the related decoders. The proposed switch driving circuit for digital input synchronization reduces the glitch energy at the outputs of the DAC. The current sources of the DAC are laid out separately from the current-cell switch matrix to minimize the noise coupling by current switches. Dummy cells are added around the current source block to reduce current mismatch.

The architecture of the proposed 12b 100 MHz current-mode DAC and the switching scheme of 255

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current cells for 8 MSBs are discussed in Section II. Section III describes the current cells and the switch driving circuits of the DAC for the improved dynamic performance. The measurement results of the prototype DAC implemented in a 0.35 um CMOS are summarized in Section IV.

II. Proposed DAC Architecture

Conventional current-steering DACs are classified into two groups of a binary-weighted array and a unit current-cell matrix. The binary-weighted array architecture based on binary-weighted current cells requires a relatively small active die area with a small number of transistors, operates at high speed, and doesn't need the separate decoders driving current cells. However, the architecture is very sensitive to process variations and tends to show high glitch energy at major code transitions. On the other hand, the unit current-cell matrix based DACs offer lower glitch energy and better monotonicity by minimizing the number of switched current cells at code transitions. The unit current cells in the matrix show less mismatch effects since the cells are turned on and off sequentially. The DAC linearity can be improved much more depending on the switching method of the current cells in the matrix. But, the unit current-cell matrix based DACs tend to be complicated and slow with more power and larger chip area due to the required additional decoders and latches. As results, most of the high-performance DACs use both architectures of the binary-weighted array and the unit current-cell matrix together, optimizing linearity, operating speed, die area, and power dissipation as required [1]-[5]. Fig. 1 summarizes the differences of the two DAC architectures.

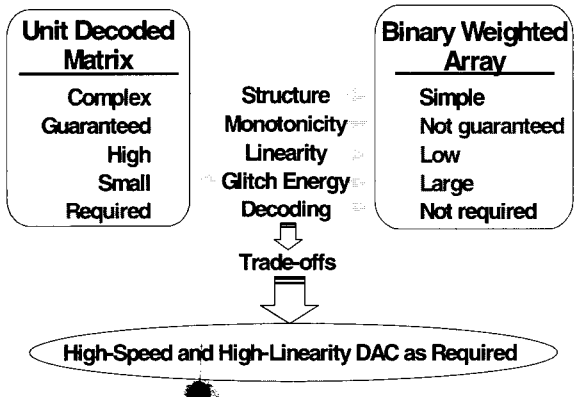

Fig. 1. Comparison of unit current-cell matrix and binary-weighted array architectures.

The proposed 12b 100 MS/s CMOS DAC is based on the segmented architecture as shown in Fig. 2. The DAC is composed of the unit current-cell matrix for 8 MSBs and the binary-weighted array for 4 LSBs, considering speed, power, area, linearity and glitch energy at 12b resolution.

The digital latches in the DAC inputs and the intermediate latches in each unit current cell of the matrix remove the delay time difference of digital signals on different paths. Switching sequence of the unit current cells in the matrix for 8 MSBs is illustrated in Fig. 3. The symmetrical and two-dimensional graded errors of the DAC are minimized by alternately turning

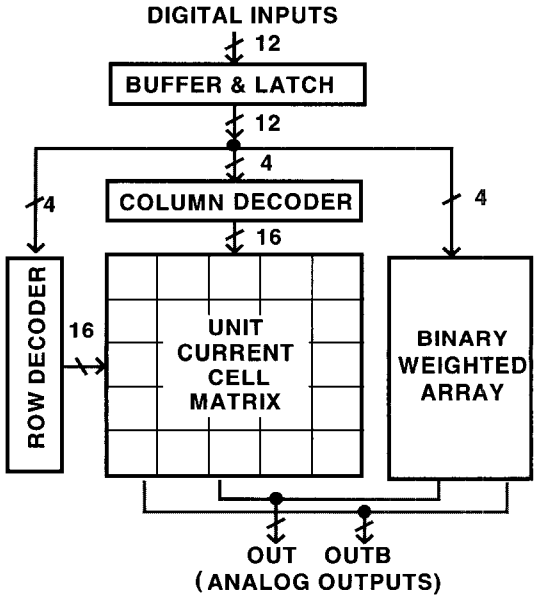

Fig. 2. Proposed 12b 100 MS/s DAC.

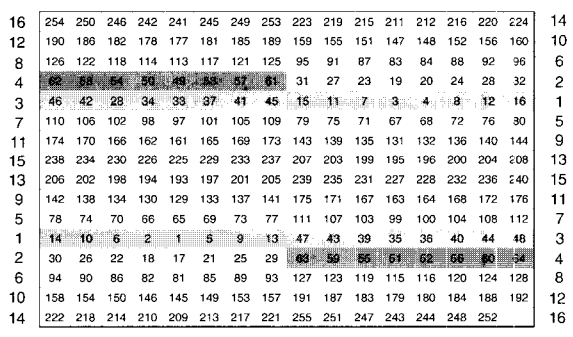

Fig. 3. Switching sequence of the unit current cells in the matrix for 8 MSBs.

on the current cells located in the diagonally symmetrical positions.

This kind of switching scheme typically needs complicated decoding circuits for actual implementation. However, the proposed DAC reduces its design complexity so that the decoder outputs can be matched to the sequence of current cells to be turned on [6]-[7]. On the other hand, temperature- and supply-insensitive CMOS current and voltage references are integrated on chip and the resistor mismatch of about ±30% can be calibrated with a single external resistor to obtain a required reference cell current [8].

III. Circuit Design

The static linearity performance of current-steering DACs is limited by the current variation of each current cell depending on the output voltages of the DACs. In the proposed DAC, a conventional cascode structure for the unit current cells is employed to minimize the current variation as shown in Fig. 4. The channel length of the cascoded transistors needs to be optimized for the required sampling speed of 100 MHz at 12b resolution.

The output impedance at the output node, OUT, of Fig. 4 needs to satisfy the following formula considering the resolution and the load impedance of the DAC [5].

$$INL = \frac{I_{unit} R_L^2 N^2}{4 Z_{imp}} \quad (1)$$

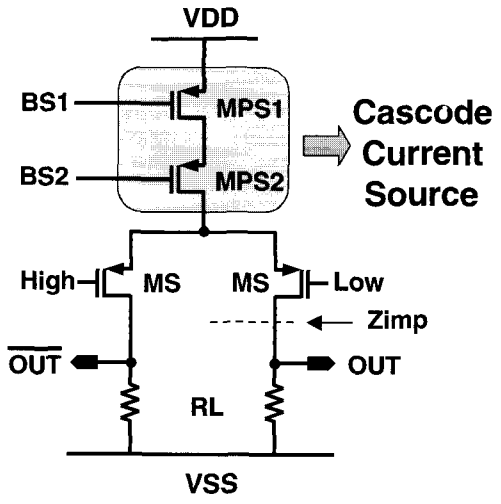

Fig. 4. Unit current cell of the proposed DAC.

(Iunit : 1 LSB current, N : total number of unit cell currents, R_L: load resistance, Zimp : output impedance at node, OUT)

Equation (1) shows that the impedance at the output node, OUT, should be high enough to improve the INL of the DAC. However, the excessively long channel length to obtain the required high impedance can let the cascoded transistors operating in the triode region. With this specific CMOS process, the W/L of the transistors MPS1 and MPS2 in Fig. 4 is designed to be 32 um / 2 um so that the transistors can be operated in the saturation region with enough margin at a 3 V supply.

On the other hand, the dynamic performance of current-steering DACs is mainly limited by the final settling time and the glitch energy of analog output signals generated by the current cells. The glitch energy is caused by various factors such as the current variation by the output voltage variation of the current sources during conversion operation, the feedthrough voltages of clocks and digital signals through the parasitic capacitances of the current

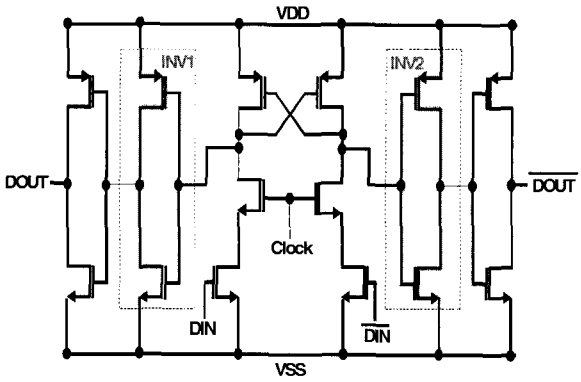

Fig. 5. Proposed switch driving circuit.

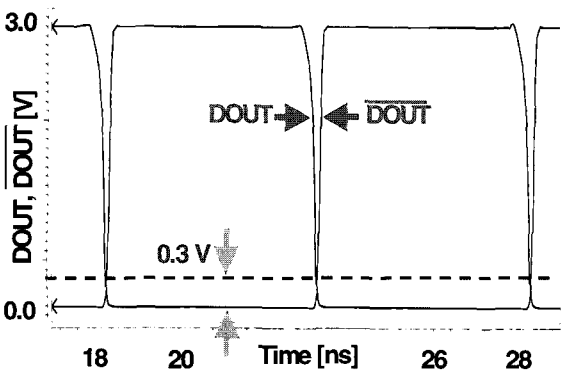

Fig. 6. Simulation result of the switch driving circuit.

steering switches, and the imperfect synchronization of the signals driving the current cell switches. The proposed DAC employs extra digital latches just before the unit current cells to synchronize the digital inputs as well as the cascoded current sources to minimize the current variation effect. In addition, the switch driving circuit as proposed in Fig. 5 reduces the glitch of analog output signals by the clock feedthrough voltages.

The switch driving circuit synchronizes the digital input signals of DIN and $\overline{\text{DIN}}$ and produces DOUT and $\overline{\text{DOUT}}$ crossing each other at a voltage close to VSS. Since the two digital outputs DOUT and $\overline{\text{DOUT}}$ directly drive the current-steering switches of each current cell, the switches are not turned off simultaneously, and instead, are turned on simultaneously for a short time, which maintains the output voltages of the current sources relatively constant without abrupt changes. The inverters in the outputs of the switch driving circuit intrinsically minimize the clock feed-through voltages. The simulated outputs of the proposed switch driving circuit are illustrated in Fig. 6, where the intersection point of two output signals D0 and D0 is set to be approximately 0.3 V at a 3 V power supply to suppress the glitch energy effectively.

IV. Prototype Dac Implementation And Measurements

Current-cell mismatch is one of the major error sources to limit the static and dynamic performances of current-mode DACs. As results, the current sources of the proposed DAC are laid out spatially separately from the current-switch matrix to minimize the inevitable mismatch between current sources by decreasing the ratio of the current sources to the total chip area. The current sources are surrounded with the guard rings composed of n-well and substrate layers to improve the dynamic performance by protecting the switching noise from the substrate.

The proposed DAC achieves the static linearity and the dynamic performance of 12b level with a 100 MHz clock by separating power supplies for analog and digital functional circuit blocks to reduce noise coupling, by isolating digital circuit blocks from sensitive analog circuit blocks with n-well and substrate layers, by employing multiple pads for power supplies to decrease the effect of parasitic bonding-wire inductances, and by placing dummy cells to minimize the mismatch around the current sources. The die photo of the prototype DAC is shown in Fig. 7. The prototype DAC was fabricated in a 0.35 um single-poly quad-metal n-well CMOS process and occupies the active die area of 2.2 mm $\times$ 2.0 mm.

The DAC was measured at a 3 V supply and the maximum output current to the 50 Ω termination resistor is 20 mA to obtain the maximum single-ended analog output voltage of 1 Vpp. As shown in Fig. 8, the measured DNL and INL of the prototype DAC are within $\pm$0.75 LSB and $\pm$1.73 LSB, respectively.

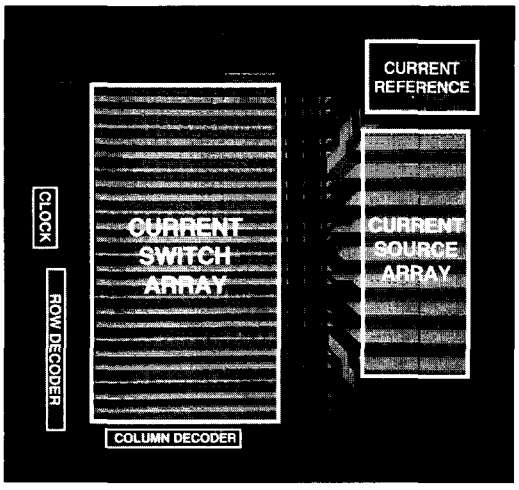

Fig. 7. Die photo of the prototype DAC.

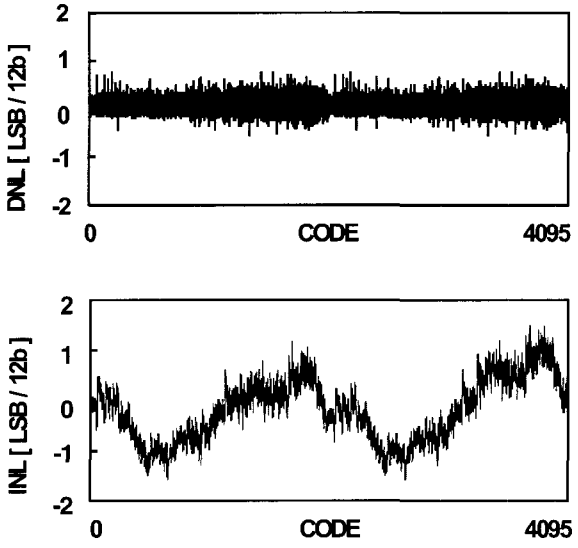

Fig. 8. Static characteristics of the prototype DAC: (a) DNL, (b) INL.

Fig. 9 shows the output spectrum of the DAC with a 10 MHz input signal at the sampling frequency of 100 MHz. The measured spurious-free dynamic range (SFDR) is 64 dB. The dynamic performance is differentially measured with a commercially available transformer connected to the DAC outputs, which reduces common-mode noise and even-order harmonic distortion components.

Fig. 10 shows the measured SFDR of the prototype DAC with different input signal frequencies at 100 MS/s. The measured performance of the proposed 12b 100 MS/s DAC is summarized in Table I.

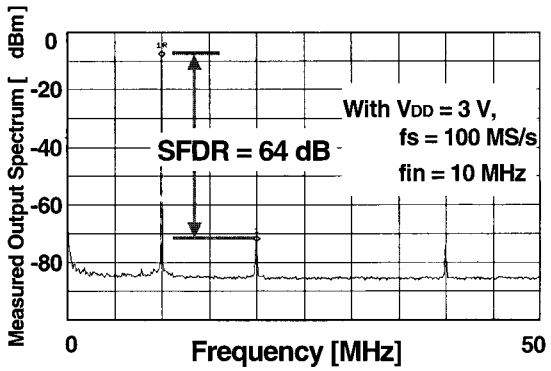

Fig. 9. Output spectrum of the prototype DAC.

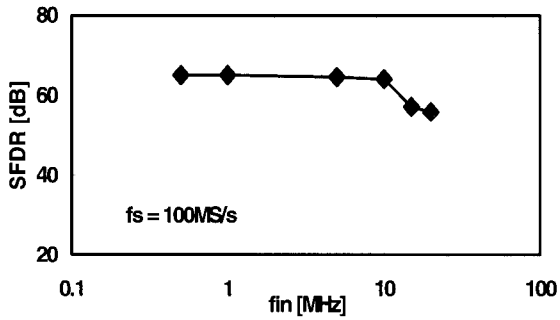

Fig. 10. Measured SFDR.

Table I. Measured performance of the prototype DAC.

Resolution	12 bits
Update Rate	100 MS/s
DNL / INL	± 0.75 / ± 1.73 LSB
SFDR (10MHz @ 100MS/s)	64 dB
Voltage Supply	3.0 V
Power Consumption	91 mW
Chip Area	2.2mm × 2.0mm
Process	0.35 um n-well 1 poly 4 metal CMOS

V. Conclusion

In this paper, a 3 V 12b 100 MS/s CMOS DAC for high-speed communication system applications is proposed. The AC employs the switch driving circuit and a variety of layout techniques simultaneously to improve the static and dynamic performances. The prototype DAC is fabricated in 0.35 um single-poly quad-metal n-well CMOS process. The measured DAC consumes 66 mW in the analog circuit blocks including the on-chip current reference and 25 mW in the digital circuit blocks, resulting in the total power consumption of 91 mW with a 3 V supply at 100 MS/s. The measured DNL and INL are within ±0.75 LSB and ±1.73 LSB, respectively, and the measured SFDR is 64 dB for a 10 MHz input signal at 100 MS/s.

Acknowledgment

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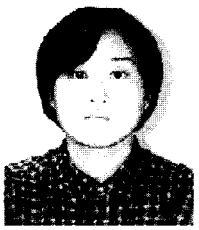

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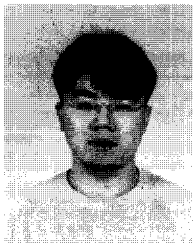

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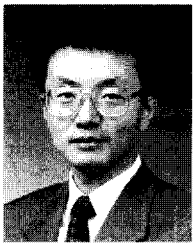

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