3- Transistor Cell OTP ROM Array Using Standard CMOS Gate-Oxide Antifuse

Jinbong Kim and Kwyro Lee

Abstract — A 3-Transistor cell CMOS OTP ROM array using standard CMOS antifuse (AF) based on permanent breakdown of MOSFET gate oxide is proposed, fabricated and characterized. The proposed 3-T OTP cell for ROM array is composed of an nMOS AF, a high voltage (HV) blocking nMOS, and cell access transistor, all compatible with standard CMOS technology. The experimental results show that the proposed structure can be a viable technology option as a high density OTP ROM array for modern digital as well as analog circuits.

Index Terms — CMOS antifuse, OTP ROM, gate-oxide breakdown

I. INTRODUCTION

Among various memory types, the one-time programmable (OTP) ROM is one of the cheapest memories storing data, which can be configured permanently after fabrication, in comparison with EEPROM based on charge retention because of its additional process [1]. There are many types of OTP ROMs, most of which are based on either fusing or anti-fusing. Poly fusing using laser has widely been used in most of the memory manufacturer's for the memory cell repair for high-density memories, such as DRAM and SRAM. This, however, is not only very expensive, but

Manuscript received October 30, 2003; revised November 20, 2003.
Dept. of EECS, KAIST Also with MICROS Research Center
373-1, Kusong dong, Yusong gu, Taejon, 305-701, Republic of Korea.
Tel : +82-42-869-5433, Fax : +82-42-869-8590
E-mail : bong@dimple.kaist.ac.kr

has a limitation that it can only be done on wafer test,

and that it is impossible to use at final test after packaging [2]. Poly fusing using joule heating has also been tried for trimming various CMOS analog circuits, such as, CMOS RF circuits, CMOS OP Amps, and ADC's and DAC's requiring on-chip trimming ROM to compensate for the process variations, device mismatches and so on [3]. However, this is not reliable enough to be used for manufacturing.

Antifuse (AF) based on anti-fusing thin oxide between two conductors is more reliable and has been adopted successfully in some commercial circuits. The via AF used in FPGA(Field Programmable Gate Array) from Actel [4] and AF using oxide-nitride-oxide (ONO) capacitor cell in DRAM proposed for repairing the failed memory cells at package level as well as at wafer level [5–6], are notable examples. The ONO AF OTP has very reliable AF characteristics, but it is not directly applicable to other standard CMOS products where thin ONO capacitor is not available.

One of the most promising candidate as AF element in standard CMOS technology is the gate oxide. Until recently, gate oxide breakdown voltage is much higher than that of the power supply. However, due to the continued scaling of gate oxide which is much faster than the power supply voltage scaling, we are now in a position to consider AF based on very thin gate oxide.[7–8]

In addition to AF element, for OTP to be useful, high voltage switching circuitry is also needed to program OTP selectively. In general, high voltage CMOS device is needed for this, which requires process change. The drift nMOS technology with AF based on gate oxide breakdown is a good example, but it needs large chip area and additional masks [9]. The construction of this high voltage circuitry using low voltage standard CMOS devices is a great challenge.

In this paper, we propose a novel 3-Transistor OTP

cell, which is fully compatible with the standard CMOS technology. It is based on 1-T AF and 2 additional transistors as high voltage switching devices, comprising 3-T cell. Sec. II describes AF characteristics of a nMOS. The operation of OTP array employing proposed 3-T CMOS OTP cell is explained in detail in Sec. III followed by conclusion.

II. CMOS ANTIFUSE STRUCTURES

Fig. 1 is the cross sectional view of nMOS AF programming (PGM mode), where applied high voltage of V_{PP} whose value is much higher than the power supply voltage is applied to the CMOS gate. The channel is inverted and the source/drain edge regions below the gate are accumulated, which favor higher electric field in edges and channel regions. We found similar phenomena happen for the pMOS AF.

Before breakdown, the gate current shows basically tunneling characteristics with very large pre-breakdown resistance of R_{OFF} more than $1G\Omega$ (@V_{PP} =2.5V), however, gate oxide is broken down permanently when V_{PP} is larger than 9V for 0.25μm CMOS process (gate oxide thickness of T_{OX} = 58Å). During the breakdown of an AF, the increasing current supply reduces the value of R_{ON} [10].
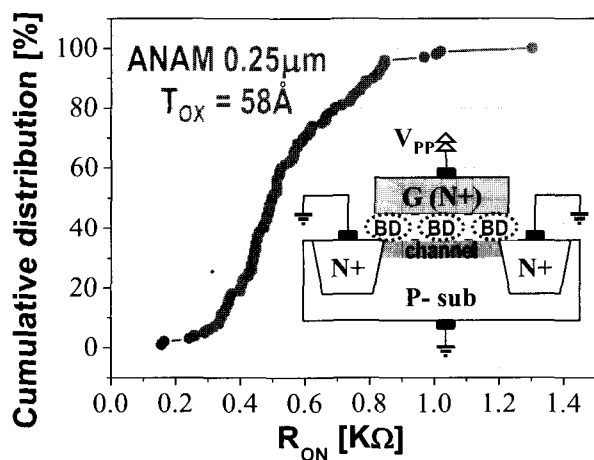

Fig. 1. The cumulative distributions of R_{ON} for 100-nMOS samples, and cross sectional diagram showing ruptured regions for channel breakdown. Breakdown conditions : V_{PP} = 9.5V,and current compliance = 1mA.

Fig. 1 shows the cumulative distributions of R_{ON}

(post-breakdown resistance) for 100 nMOS samples. The measurement of R_{ON} is performed with HP 4156A (precision semiconductor parameter analyzer) after gate oxide breakdown. The breakdown conditions are the applied V_{PP} (high-voltage) of 9.5V, the constant current of 1mA, and the sampling duration of 1 second (sampling period = 1m sec). The R_{ON} is measured at the V_{PP} of 2.5V using Ohm's law (V_{PP}/I_{PP}). From these measurement results, designing the OTP ROM array, if we set the R_{ON} as more than 5KΩ and the $t_{BREAKDOWN}$ as above 1 second, at most 1-bit failure occurs every 10^{12} bits programming.

III. 3-TRANSISTOR/1-BIT CMOS OTP ROM ARRAY

To use CMOS AF into an OTP ROM array, we propose 3-T OTP cell as shown in Fig. 2(a), which is composed of an nMOS AF (AF), a HV blocking nMOS (BM), and a cell access transistor (AT). In the PGM mode, HV is applied to the tied gates of all nMOS AF's (V_{PP} node) and only one AF selected by corresponding word-line (WL) and bit-line (BL) selection, is programmed. In the read mode, V_{DD} is applied to the V_{PP} node. In the programmed cell, current will flow through the AF to BL, which can be detected in the BL sense amplifier, while no current flows from the non-programmed cell.

Fig. 2(b), (c), (d) and (e) show various operation conditions during programming for selected/non-selected cells to explain programming/possible disturbances. In selected cell shown in Fig. 2(b) and Fig. 3.(a), after AF ruptured, HV would be applied the drain-substrate junction of blocking nMOS in case of small R_{ON}. To avoid this situation, we inserted a blocking resistor (R_{BLK}) in series with HV supply source, which also helps to keep constant current level for uniform rupturing.

For the non-selected cell with already broken AF as shown in Fig. 2(c) and Fig. 3(b), HV is now applied directly to the drain-substrate junction of blocking nMOS, which cannot also be destructive to blocking nMOS. Because the access transistor is now in OFF-state, only very small GIDL (Gate Induced Drain Leakage) current of blocking nMOS flows through drain-to-

substrate junction(<1μA/1-bit cell @ V_{PP} = 9.5V), which
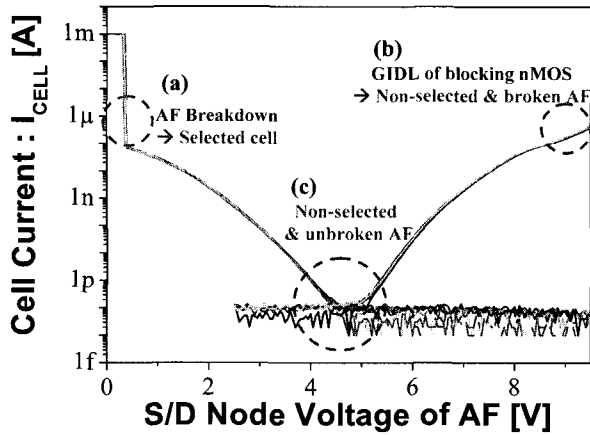

Fig. 3. The load-line plots for operation voltage : (a) selected cell for rupture, (b) non-selected cell with broken AF, (c) non-selected cells with unbroken Afs

is non-destructive during long programming duration above 1-hour.

Both of these are necessary conditions for proper array operation. As for the case of non-selected cell with unbroken AF shown in Fig. 2 (d), (e) and Fig. 3(c), we also find that there are no disturbance problems. The HV is divided by the ratio of two resistors (AF R_{OFF} and blocking nMOS resistor from GIDL), that is, the equilibrium conditions between two currents which are the tunneling current of unbroken AF and the GIDL current of blocking nMOS. Therefore, non-selected and unbroken AF gates are not ruptured during programming. And the breakdown voltage of V_{PP} for non-selected cell is at least above 16V.

The 4-bit cell measurement results are shown in Fig. 4. In programming mode shown in Fig. 4 (a), selected cells, i.e. (cell 0,1) and (cell 0,0), are successively prog
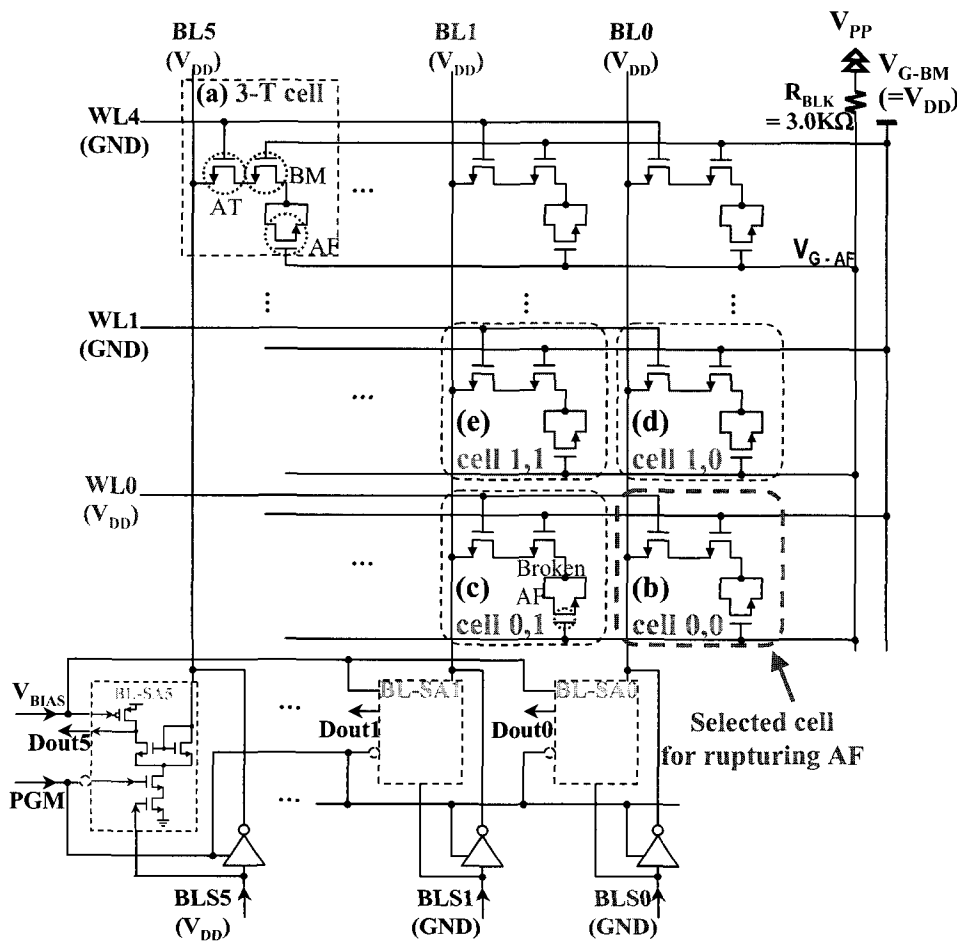

Fig. 2. (a) Proposed 3-T CMOS OTP ROM cell, (b) selected cell for programming, (c) non-selected cell with broken AF, (d) and (e) non-selected cells with unbroken AF's
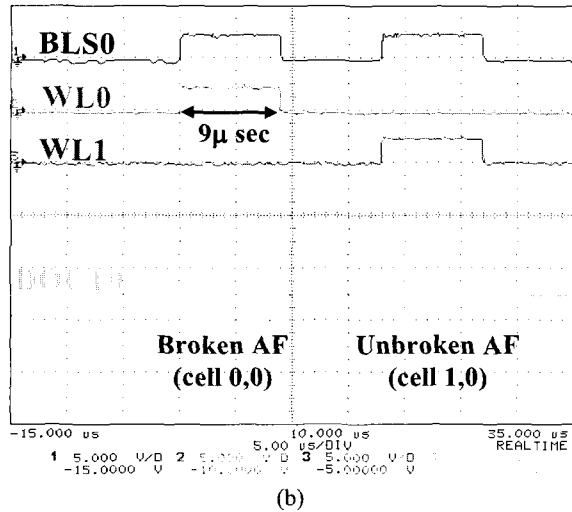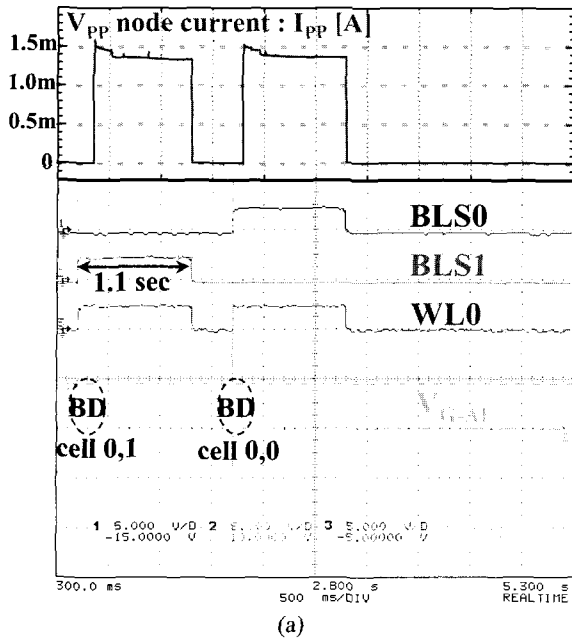
(a)

(b)

Fig. 4. OTP ROM array measurement results ; (a) Programming mode, and (b) Reading mode

rammed with input 'V$_{DD}$' signals of (WL0, BLS1) and (WL0, BLS0). When AF's are ruptured, the gate voltages of AF's are gone down to 5V and supplied currents are about 1.4mA for both cases. In the reading mode shown in Fig. 4 (b), previously ruptured cell (cell 0,0) and unbroken AF cell (cell 1,0) are read. The output value for programmed cell is '0V' and unbroken AF cell is 'V$_{DD}$', respectively.

The microphotograph of 30-bit OTP ROM array is shown in Fig. 5. The cell area of the proposed 3-T OTP ROM is 35μm^2/1-bit with 0.25μmANAM CMOS technology.
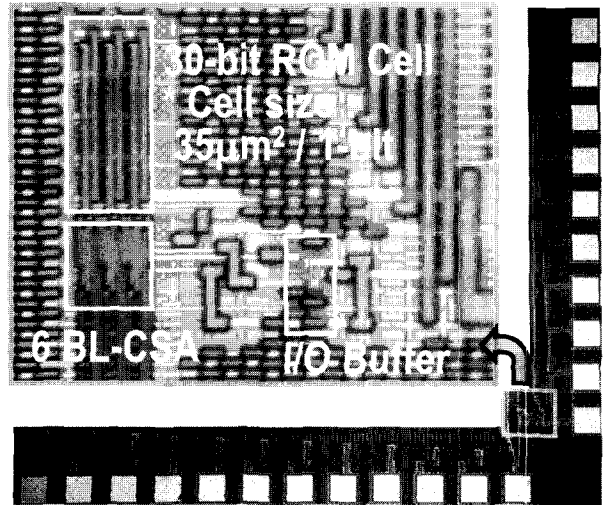

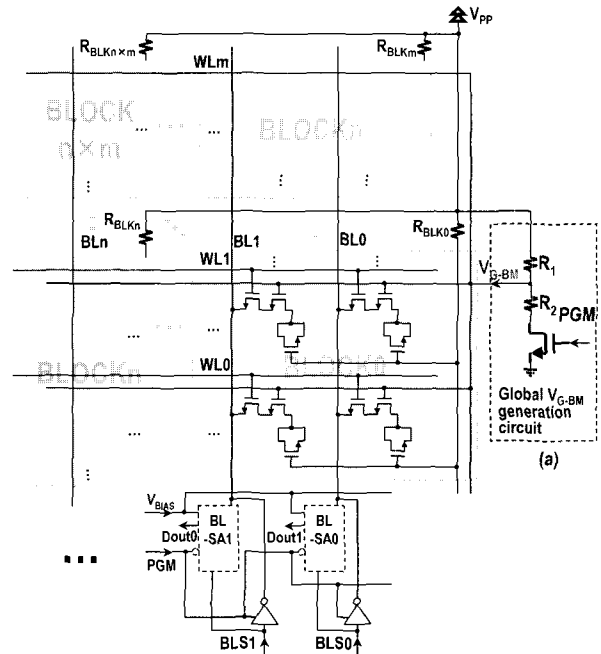**Fig. 5.** Chip microphotograph : 30-bit ROM cell

Fig. 6. The high-density OTP ROM structure ; (a) the high-voltage blocking nMOS biasing circuit using programming high-voltage, and (b) the high-density OTP ROM structure which is composed of a group of blocks and global blocking nMOS biasing circuits

To implement high-density OTP ROM array, we have considered highly reliable operation during long programming duration. The GIDL current is at most several hundreds of nA in single cell, but in several thousands of OTP ROM array the GIDL current is more than several mA. This GIDL current and a blocking resistance make programming voltage drop between two

electrodes of AF. A unit block, which is composed of several hundreds of cells and a blocking resistance, can solve this problem. In the non-selected and already broken AF cell, another possible problem is the gate-oxide reliability of blocking nMOS, which can be broken-down during long programming time. To avoid this situation, we introduce the high-voltage gate biasing of blocking nMOS. In the Fig. 6 (a), we show the global V_{G-BM} biasing circuit, which is made of just two resistors and one nMOS. From these considerations, we can design the high-density OTP ROM array that is shown in Fig. 6 (b). In addition to higher reliability, higher V_{G-BM} biasing enables us to design smaller 3-T cell and to consume lower GIDL current in the non-selected and already broken AF cell during PGM-mode.

IV. SUMMARY AND CONCLUSION

In this paper, we firstly measured CMOS AF electrical characteristics before and after programming, which shows high enough fresh gate oxide resistance of $R_{OFF} > 1G\Omega$ and low enough programmed resistance of $R_{ON} < 5K\Omega$. The breakdown characteristics are uniform enough to use it as an OTP memory element. Based on this CMOS AF's, we proposed 3-Transistor cell OTP ROM array, which is composed of an nMOS AF, a HV blocking nMOS, and cell access transistor, all compatible with standard CMOS technology. Experimental results show that the proposed structure can be a viable technology option as a high density OTP ROM array for modern digital as well as analog circuits.

ACKNOWLEDGEMENT

REFERENCES

[1] K.-H. Kim and K. Lee, "An 8-b Resolution 360 μs Write Time Nonvolatile Analog Memory Based on Differentially Balanced Constant-Tunneling-Current Scheme (DBCS)," in IEEE International Solid-State Circuit Conference (ISSCC)1998, pp. 336–337, 459.

[2] Chih-Yuan Lu, James D. Chlipala, and Leonard M. Scarfone, "Explosion of Poly-Silicide Links in Laser Programmable Redundancy for VLSI Memory Repair", in IEEE Transaction on Electron Devices, vol.36, No.6, pp.1056-1062, Jun., 1989

[3] O.Kim, C.J.Oh and K.S.Kim, "CMOS trimming circuit based on polysilicon fusing", in Electronics Letters, vol.34, No.4, pp.355-356, Feb., 1998

[4] http://www.actel.com/products/antifuse.html

[5] Jae-Kyung Wee, Jeong-Hoon Kook, Sang-Hoon Hong, and Jin-Hong Ahn, "Antifuse Circuits and Their Applications to Post-Package of DRAMs", in Journal of Semiconductor Technology and Science (JSTS), vol.1, No.4, pp.216-231, Dec., 2001

[6] Joo-Sun Choi, Jae-Kyung Wee, Ho-Youb Choi, Phil-Jung Kim, Jin-Keun Oh, Chang-Hyuk Lee, Jin-Yong Chung, Sea-Chung Kim, and Woodward yang, "Antifuse EPROM Circuit for Field Programmable DRAM", in IEEE International Solid-State Circuit Conference (ISSCC) 2000, pp.406-407

[7] Jinbong. Kim and Kwyro. Lee, "3-Transistor OTP(One-Time Programmable) ROM Cell Array Using Standard CMOS Gate Oxide Antifuse", in Electron Device Letters (EDL), Vol.24,No.9, Sep. 2003

[8] Jinbong. Kim and Kwyro. Lee, "3-Transistor Antifuse OTP ROM Array using Standard CMOS Process", in Symposium in VLSI Circuits (SOVC) 2003, pp.239-242

[9] Philippe Candelier, Nathalie Villani, Jean-Pierre Schoellkopf, and Patrick Mortini, "One Time Programmable Drift Antifuse Cell Reliability", in IEEE International Reliability Physics Symposium, pp.169-173, 2000

[10] Guobiao Zhang, Chenming Hu, Peter Y. Yu, Steve Chiang, Shafy Eltoukhy, and Esmat Z. Hamdy, "An Electro-Thermal Model for Metal-Oxide-Metal Anti-fuses", IEEE Transition on Electron Devices, vol.42, pp.1548-1558, 1995

Jinbong Kim was born in Changwon, Republic of Korea, in 1971. He received the B.S. and M.S degrees in Electrical Engineering and Computer Science (EECS) from the Korea Advanced Institute of Science and Technology (KAIST), Taejon, in 1997 and 1999, respectively. From 1999, he is pursuing the Ph.D. degree in EECS from KAIST. His current research interests are in CMOS non-volatile memories and Micro-controller units.

Kwyro Lee received the B.S. degree in Electronics Engineering from Seoul National University in 1976 and the M.S. and Ph. D. degrees from the University of Minnesota, Minneapolis in 1979 and 1983 respectively, where he did many pioneering works for modeling Heterojuction Field Effect Transistor.

After graduation, he worked as an Engineering General Manager in GoldStar Semiconductor Inc. Korea, from 1983 to 1986, responsible for development of first polysilicon CMOS products in Korea. He joined KAIST in 1987 in the Department of Electrical Engineering, where he is now a Professor. His research interests are focused on RF device, circuit and polylithic integration of heterogeneous system on a single chip. He led the development of AIM-Spice and is the principal author of the book titled, "Semiconductor Device Modeling for VLSI", 1993, Prentice Hall. He is a Senior Member of IEEE and a Life Member of IEEK. He served as the Chairman of IEEE Korea Electron Device Chapter and is currently serving as the elected member of IEEE EDS AdCom. He has also been working as the Director of MICROS(Micro Information and Communication Remote-object Oriented Systems) Research Center since 1997.