A novel 622Mbps burst mode CDR circuit using two-loop switching

Pyung-Su Han , Cheon-Oh Lee, and Woo-Young Choi

Abstract— **This paper describes a novel burst-mode clock and data recovery (CDR) circuit which can be used for 622Mbps burst mode applications. The CDR circuit is basically a phase locked loop (PLL) having two phase detectors (PDs), one for the reference clock and the other for the NRZ data, whose operations are controlled by an external control signal. This CDR was fabricated in a 1-poly 5-metal 0.25μ m CMOS technology. Jitter generation, burst/continuous mode data receptions were tested. Operational frequency range is 320Mhz~720Mhz and BER is less than 1e-12 for PRBS31 at 622Mhz. For the same data sequence, the extracted clock jitter is less than 8ps rms. Power consumption of 100mW was measured without I/O circuits.**

Index Terms— **PON(Passive Optical Network), burst mode, CDR(Clock and Data Recovery), PLL(Phase Locked Loop)**

I. Introduction

In the passive optical network (PON) systems, the optical network units (ONUs) are connected to a shared optical bus. ONUs use short burst pulses to transmit data to the optical line terminator (OLT), and OLT receives a sequence of bursts[1]. Unlike in the continuous mode operation, the received signals have neither a fixed power nor a continuous phase, and the OLT receiver must reset the decision level and the clock phase at every beginning of the burst. Since the conventional CDRs require a few hundreds of bits to track these intermittent phase jumps, they are not suitable for burst mode applications.

Several techniques have been reported to implement the burst mode CDR. Almost all of them adopt the phase-resettable gated oscillators, which lead to very poor jitter transfer characteristics and the susceptance to the duty cycle distortion of input signal [2].

We propose a new burst mode clock recovery circuit whose jitter characteristics can be easily determined and which requires only four preamble bits.

II. Circuit Operation

Basically, the proposed CDR is a PLL that has a singe VCO and two PDs, one PD for the reference clock and the other PD for the NRZ data. Fig.1 shows the circuit structure.

The first PLL loop is called the reference locked loop, which adopts PFD(Phase Frequency Detector) and locks to the local reference clock. This loop is a conventional PLL loop. It compares the VCO oscillation frequency and the local reference clock frequency, and preserves the VCO control voltage against leakage currents during the data packet gaps.

The second PLL loop is called the clock recovery loop, which adopts PD for NRZ data and actually extracts clock from the data bit sequences. This loop acts just like a conventional continuous mode CDR.

The external control signal, BSTE (BurST Enable) controls the switching operation between two loops. Then the control circuit generates the turn on and off signals for the internal blocks, along the pre-defined

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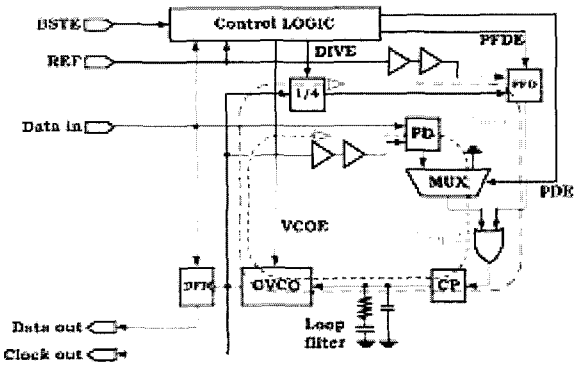

Fig. 1. Block diagram

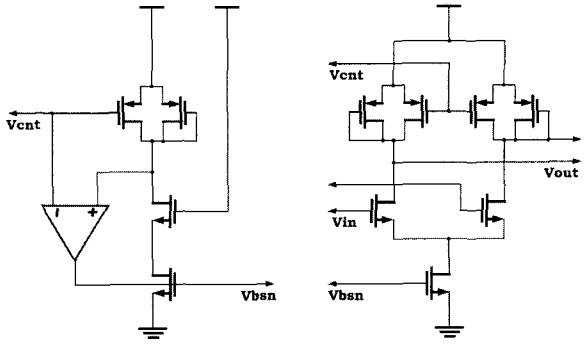

Fig. 2. VCO delay stage and bias circuit

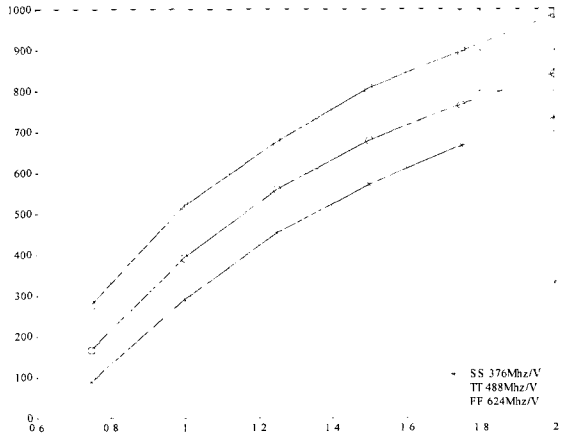

Fig. 3. Characteristic curve of designed VCO

sequence. The control circuit is a simple FSM (finite state machine), whose detailed description is given in the next section. Loops are switched in step with the data transition edges, and the additional phase acquisition time is not necessary. In other words, the loop instantly locks.

Contrary to the gated-VCO-based burst mode CDR, the proposed CDR shows the same jitter performance as the PLL-based CDR and is less susceptible to the duty cycle distortion.

III. Building Block Design

A. Phase-resettable gated VCO

In the CMOS VCO design, a ring oscillator is very popular for its compactness and no need for inductors that are difficult to implement and take large area. In the ring oscillator design, the resistive loads in delay stages should have good linearity. A parallel combination of a DC biased MOS and a diode connected MOS is called the symmetric load, and the replica biasing scheme allows designers to use the most linear region of the I/V characteristic of the symmetric loads. The scheme used in VCO delay stage and bias circuits of Fig.2 are the same as those given in [3]. As a gating stage, a MUX is used among the buffer chain and the signals from the previous buffer are inverted. The second input terminal is tied with logical high. When VCOE (VCO Enable) is low, the MUX selects the second input. If VCOE signal goes to high, the oscillation begins. Fig.3 shows the simulated characteristic curve of the designed VCO.

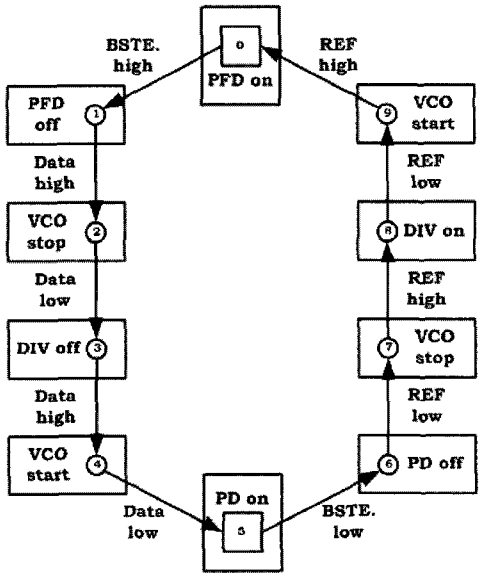

Fig. 4. Control circuit state diagram

B. Control logic circuit

The FSM has ten states in total and two of them are stable; the state 0 is locked at the local clock state and

the state 5 is locked at the data state. Fig.4 shows the state diagram. All the state transitions are initiated by the BSTE signals and the data/local clock edges make the FSM move into the next state. For example, when the FSM is in the state 0, the circuit is locked to the local clock and ready to receive the burst mode data. Then BSTE goes to high, notifying the FSM that the burst data are coming, and the FSM moves into the state 1 and waits for the data transition. Following the data transition the state advances, and finally the VCO starts with the loop nearly locked. After data receiving is finished, BSTE goes to low, and the similar activities resume after another half-circle transition.

C. Other building blocks

All the logic circuits are designed with differential logic gates. Although the differential signaling consumes more power and is cumbersome to design, it is faster and less susceptible to noises.

IV. Loop Dynamics

The second order loop filter is employed and the loop transfer function becomes the third order. By assuming that the second capacitor is small enough, the second order loop transfer function can still be used for the analysis of the third order loop dynamics [4].

Loop bandwidth and damping factor describe the loop dynamics and they can be calculated as follows:

$$\text{Loop bandwidth : } \omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{NC}}$$

$$\text{damping factor : } \varsigma = \frac{R}{2}\sqrt{\frac{K_{PD}K_{VCO}C}{N}}$$

Since the reference locked loop employs a 1/4 frequency divider but the clock recovery loop does not, careful loop filter design is required. N means the reciprocal of feed back gain. For reference locked loop, N= 4 because this loop use the 1/4 frequency divider. For clock recovery loop, N is 2 because the input data transition probability is 0.5 for its random nature. With KPD = 75μA/rad, KVCO=500MHz/V, C=150pF, and R=500Ω , reference locked loop has ω_n = 15MHz and ζ = 0.6, and clock recovery loop has ω_n = 21MHz and ζ = 0.85 .

V. Experimental Results

The proposed circuits were implemented in a five-metal one-poly 0.25um CMOS process. Fabricated chips were bonded in 44pin TQFP(thin quad flat package), and assembled in test board. The micrograph in Fig.5 shows the designed CDR circuit. The chip has a core area of 500μ m x 600μ m including the loop filter.

A. Operational frequency range/jitter generation

The operational frequency range of the VCO was measured. The VCO showed stable oscillation for the local reference clock range of 80Mhz~180Mhz. With 1/4 frequency divider, the correspondent VCO oscillation range was 320Mhz~720Mhz. Jitter generation of the PLL at each low, high corner and target frequency was also measured. The measured peak to peak jitter is less than 26ps and the rms jitter is less than 3.6ps for all over the operational frequency range.

B. Burst mode data reception

As described above, the control logic needs two up and two down transitions as preamble bit sequence, for

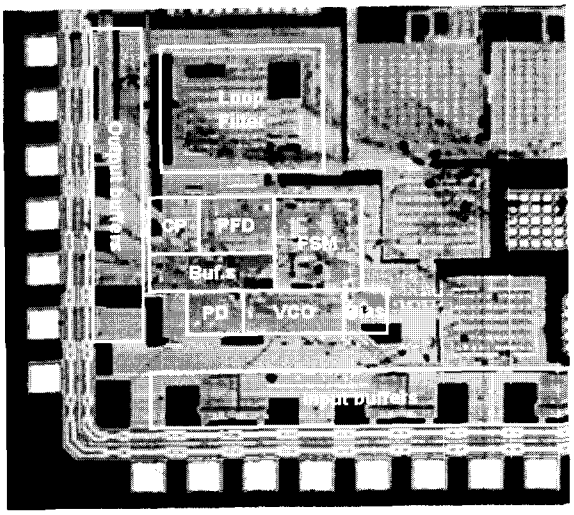

Fig. 5. Micrograph of fabricated circuit

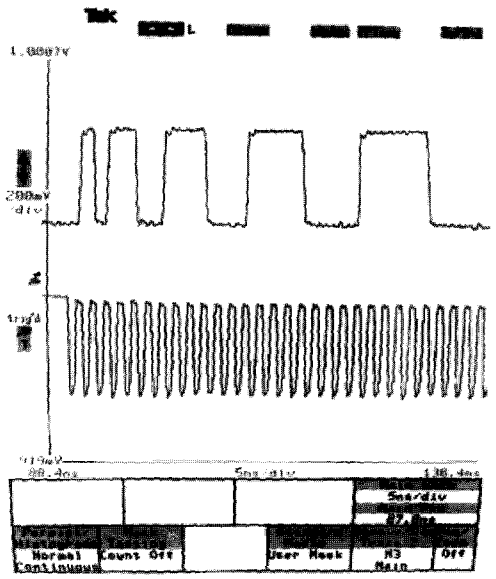

Fig. 6. Burst mode data reception

example 1010. Control signal and bursting data pattern generated using high-speed AWG (Arbitrary Waveform Generator) were supplied and the extracted clock and retimed data were observed. Fig.6 shows the output signal captures, retimed data and extracted clock. Various lengths of preamble patterns were tested, and the circuit successfully extracted data clock with preamble of 4bits, 1010.

C. Continuous mode data reception

Using BER tester, PRBS (Pseudo Random Bit Sequence) were generated and supplied, BER and extracted clock jitter were measured. BER is less than 1e-12 for PRBS31 at 622Mbps, and for the same data pattern and the same data rate, the extracted clock jitter is less than 7.7ps. Fig. 7 shows the output clock jitter histogram capture and Fig. 8 shows retimed data eye-diagram for PRBS31.

D. Effect of frequency offset of reference clock

For the ideal operation of our circuit, the local reference clock frequency should be exactly 1/4 of the data rate. With non-zero frequency offsets of reference clock, more data transitions in preamble pattern are required to get rid of the frequency difference between the VCO output clock and the incoming data.

Error-free ranges of operational reference frequency are measured for the preamble bit patterns of various lengths followed by the 8 identical bit sequences. For example, with the 6-bit preamble, the test data pattern is '101010 + 11111111 + 00000000...'.

The measured error-free operational frequency ranges for the given data pattern are ± 1.12% for 8 bit preamble, ± 1% for 6 bit preamble, and ± 0.8% for 4 bit preamble.

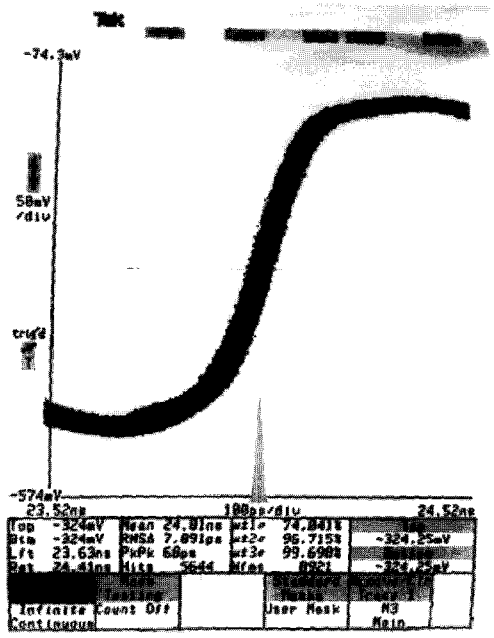

Fig. 7. Recovered clock jitter from PRBS31

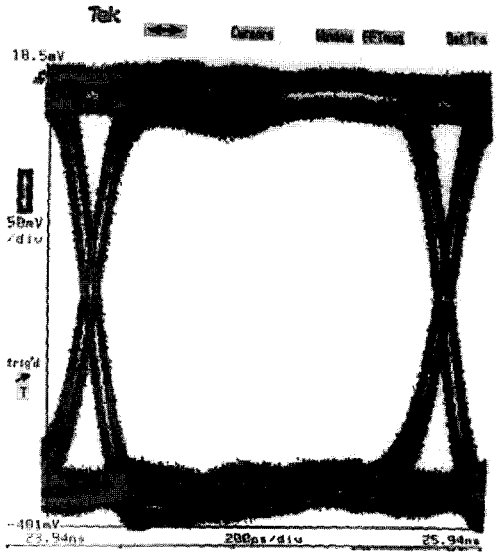

Fig. 8. Retimed data eyediagram from PRBS31

E. Effect of input data PWD(Pulse Width Distortion)

The gated-VCO-based burst mode CDR circuit resets the output clock phase at data transitions. Consequently, any input data pulse width distortion (PWD) causes PWD in the extracted clock signals. However, in the PLL based CDR circuits, the data PWD is filtered out.

With AWG (arbitrary waveform generator), data with distorted duty cycles (62.5% for wide 1 and 37.5% for narrow 1) are produced for the bit sequence of 1010110011110000. The measured rms clock jitters and duty cycles are 7.7ps and 52% for both cases. Fig. 9 shows that wide-1 (duty cycle larger than 50%) data pattern and retimed data signals.

In the measurement, 3.3V power supply voltage is used and power consumption measured is 100mW excluding I/O circuits. Measured results are summarized in Table 1.

Table 1. Summary of experimental results

Operational Data rate	320Mbps ~ 720Mbps
VCO jitter generation	26ps(p2p), 3.6ps(rms)
Required preamble pattern	1010(4bits)
BER for PRBS31	Less than 1e-12
Recovered clock jitter for PRBS31	8ps(rms)
Power consumption	100mW without I/O
Power supply voltage	3.3V
Area	500μ m by 600μ m including loop filter

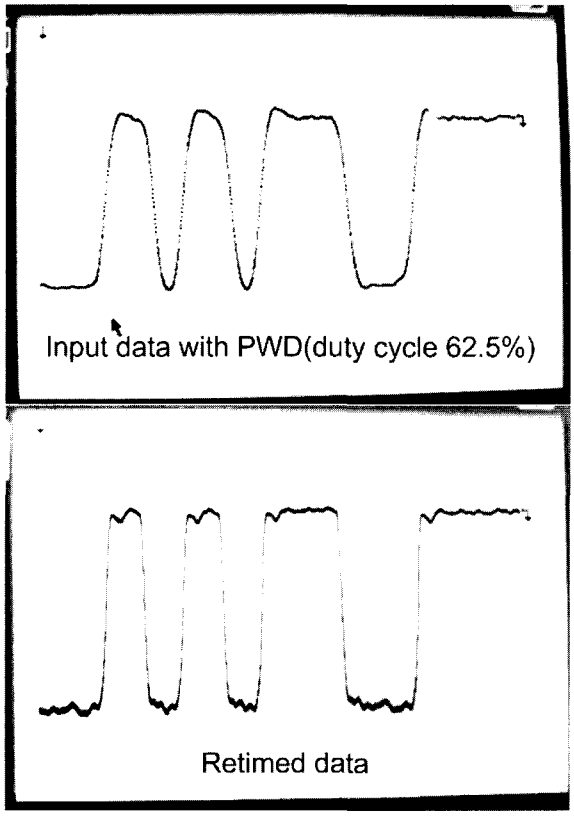

Fig. 9. Retimed data capture from pulse width distorted data

VI. Conclusion

A burst mode CDR circuit for 622Mbps NRZ data was designed and fabricated in a 0.25um 5-metal 1-poly CMOS process. The proposed circuit is capable of rejecting jitter and has the duty cycle distortion immunity as well. The designed building blocks include the fully differential gated-VCO, PFD/PD, the frequency divider, the charge pump/loop filter and the control logic circuit. All the logic gates and VCO are replica biased for constant signal swing levels. Designed circuit was fabricated and assembled in test board for performance verification. Experimental results show that the circuit functions successfully with 622Mbps burst mode data. For PRBS31 data, the patterns recovered clock jitter is less than 8ps rms and the measured power dissipation is 100mW.

Acknowledgements

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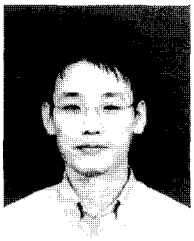
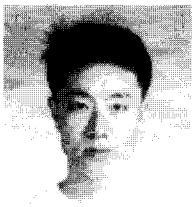


Pyung-su Han was born in Seoul, Korea, in 1976. He received the B.S degree in electrical and electronic engineering in 2002 from Yonsei University, Seoul, Korea, where he is currently working toward the M.S. degree. His research interests include high-speed serial communications and mixed mode singal circuits in CMOS.



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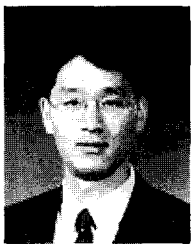

Woo-Young Choi received the B.S., M.S., and Ph.D. degrees, all in electrical engineering and computer science, from the Massachusetts Institute of Technology, Cambridge. For his Ph.D. dissertation, he investigated MBE-grown InGaAlAs laser diodes for fiber optic applications.

From 1994 to 1995, he was a post-doctoral Research Fellow at NTT Opto-electronics Labs, where he worked on femtosecond all-optical switching devices based low-temperature-grown InGaAlAs quantum wells. In 1995, he joined the Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea, where he is presently an Associate Professor. His current research interests are in the area of high-speed information processing technology, including high-speed optoelectronics, high-speed electronic circuits, and microwave photonics