Stress and Stress Voiding in Cu/Low-k Interconnects

Jong-Min Paik, Hyun Park, and Young-Chang Joo

Abstract—Through comparing stress state of TEOS and SiLK-embedded structures, the effect of low-k materials on stress and stress distribution in via-line structures were investigated using three-dimensional finite element analyses. In the case of TEOS-embedded via-line structures, hydrostatic stress was concentrated at the via and the top of the lines, where the void was suspected to nucleate. On the other hand, in the via-line structures integrated with SiLK, large von-Mises stress is maintained at the via, thus deformation of via is expected as the main failure mode. A good correlation between the calculated results and experimentally observed failure modes according to dielectric materials was obtained.

Index Terms—reliability, interconnection stress voiding, Cu damascene low-k dielectric

I. Introduction

As RC delay and crosstalk are becoming limiting factors in the next-generation integrated circuit interconnects, copper and low-k dielectrics are introduced to reduce electric resistance and parasitic capacitance. Cu interconnects are fabricated by the damascene process in which Cu is electrochemically deposited into the trenches and excess material over the trench is removed by chemical mechanical polishing (CMP). Due to the higher melting point and lower

diffusivity of Cu than that of Al, Cu interconnecct is expected to overcome reliability issues such as electromigration and stress-migration [1]. However, in reality, there are some reliability problems in Cu/low-k interconnect. For example, electromigration is still issued due to fast surface diffusion [2], and Cu ion drift into the dielectrics [3] can induce severe integration problems. Stress related issues such as stress voiding [4] and delamination [5] are also becoming more problematic in Cu/low-k, especially because of lower mechanical stress of low-k materials.

Since electroplating is a non-equilibrium process due to rapid deposition rate at room temperature, it is well known that electroplated Cu has the high density of defects, dislocation and vacancy densities [6] and shows the characteristic microstructure evolution at room temperature, known as self-annealing [7]. If this is the case, stress distribution as well as stress itself could be an important parameter because stress gradient drives vacancy diffusion [8]. Ogawa et al. [4] observed an abnormally huge void under the via during high temperature storage test. They suggested that supersaturated vacancies induced by grain growth diffuse due to stress gradient and accumulate at the stress concentration sites.

Integration using low-k material results in new failure modes related to stress. Generally deformation is not common to TEOS based interconnects because TEOS is relatively hard. However, low-k materials have very low elastic moduli and large thermal expansion coefficients comparing to those of TEOS (Table 1). Therefore, it is expected that low-k material may be mechanically deformed due to thermal stresses.

Two kinds of low-k dielectrics are classified; organo silicate glass (OSG) such as black diamond and $CORAL^{TM}$ and organic polymer based low-k materials such as $SiLK^{TM}$, polyimide, benzo-cyclobutane, etc. Generally, organic polymer based low-k materials have

Manuscript received August 17, 2003; revised August 28, 2003. School of Materials Science and Engineering, Seoul National University, Seoul 151-744, Korea, ycjoo@plaza.snu.ac.kr

Research Institute of Advanced Materials, Seoul National University, Seoul 151-744, Korea

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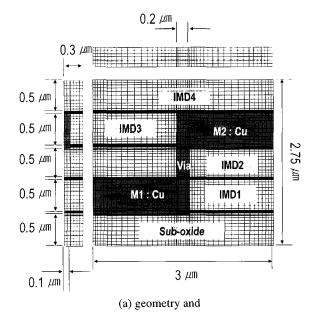
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	CTE (ppm/℃)	Modulus (GPa)	Poisson's Ratio
Cu	17.7	115	0.343
TEOS	0.51	71.7	0.16
SiLK	66.0	2.0	0.35
SiOC (BD)	20.0	6.3	0.3
Та	6.5	185.7	0.342
SiN	3.2	220.8	0.27
SiC	4.2	410.0	0.14

much larger thermal expansion coefficient and lower elastic modulus than OSG. Therefore, it is expected that the problems related to the thermo-mechanical properties would be much severer for organic polymer based low-k despite of their superior electrical properties. In this study, through comparing stress state of TEOS and SiLK-embedded structures, which are two extreme cases, the effect of low-k materials on stress and stress distribution in via-line structures were investigated using three-dimensional finite element analyses.

II. EXPERIMENTAL PROCEDURE

Figure 1 (a) and (b) shows the model geometry for 2level via-line structures and boundary conditions used in this study. The bottom plane (y=0) is assumed to be rigidly clamped on a substrate such that no displacement is allowed in any direction. The top surface is free to move during deformation. The other four surfaces have the conditions of the mirror symmetry normal to each surface. All interfaces are assumed to have perfect adhesion. A commercial finite element program ABAQUS 6.2 was used for the calculation. The discretizations used 8-noded linear brick-shape elements. The convergence of results was confirmed by various degrees of mesh refinements. Each material is characterized as an isotropic linear elastic solid and an isotropic elastic solid. This assumption is reasonable because it is known that Cu lines of which width is in sub-micron ranges show linear elastic behavior even up to 400°C [9]. The material properties used in this calculation are summarized in Table 1. Calculations were performed for cooling from the initial stress-free temperature assumed to be 400°C to room temperature (25°C). Since the zero stress state is known to be about 200°C, it should be noted that the present stress values calculated from the finite element analysis are about two times as large as practical counterparts. In order to consider the thermal expansion of the Si substrate, the substrate is chosen as the reference frame, and the CTE of all the other material are adjusted relative to the substrate.



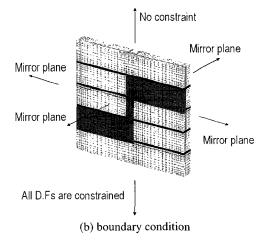


Fig. 1. The used model for 2-level via-line structures; description of .

III. FINITE ELEMENT ANALYSIS RESULTS

Figure 2 shows the individual stress components of TEOS-embedded via-line structures in the form of contour plots. It can be found that the stress state of the lines is different from that of via. The largest stress component was σ_{xx} and σ_{yy} for the lines (M1 and M2) and the via, respectively.

Hydrostatic stress is known to be the driving force for stress voiding, or in the more strict sense, driving force for stress void nucleation [10]. Therefore, the site where the hydrostatic stress is the most concentrated is thought to be most probable void nucleation site. The von-Mises stress, which is usually used as a criterion for plastic deformation, is in a form of octahedral shear stress which does not include the hydrostatic stress components and usually does not affect the volumetric changes of material. The hydrostatic stress and the von-Mises stress can be formulated using equations 1 and 2, with respect to the principal stresses.

$$\sigma_{H} = \frac{(\sigma_{x} + \sigma_{y} + \sigma_{z})}{3}$$

$$\sigma_{y} = \frac{1}{\sqrt{2}} \left[(\sigma_{y} - \sigma_{y})^{2} + (\sigma_{y} - \sigma_{z})^{2} + (\sigma_{z} - \sigma_{x})^{2} \right]^{\frac{1}{2}}$$
(2)

Figures 3 (a) and (b) show the hydrostatic stress distribution and the von-Mises stress distribution of TEOS embedded via-line structure, respectively. The highest and the 2nd-highest hydrostatic stress and found at the bottom plane of the via and at the top plane of the lines, respectively. Therefore, it is suggested that the dominant nucleation site would be either of the bottom of the via or the top of the lines.

The stress state of SiLK-embedded via-line structures is much different from that of TEOS embedded structures. Figure 4 shows the individual stress components for the SiLK-embedded structures. As shown in the Table 1, SiLK has very low elastic modulus and substantially high thermal expansion coefficient, which are typical mechanical properties of organic-based low-k materials. Especially, the thermal expansion coefficient of SiLK is four times as large as that of Cu and one hundred times as that of TEOS. Therefore, the sign of thermal stress of SiLK-embedded structures can be opposite to that of TEOS-embedded structures.

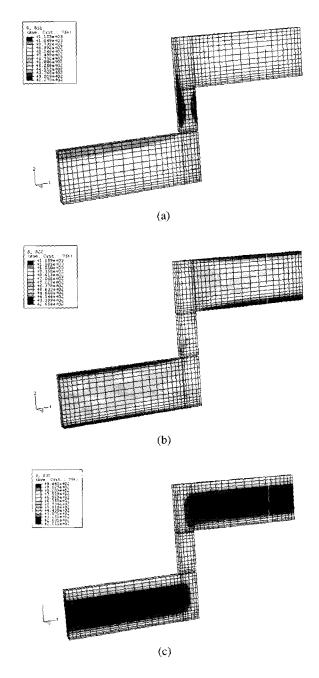


Fig. 2. The individual stress components of TEOS-embedded via-line structures in the form of contour plots; (a) stress in the x-direction (s11), (b) stress in the y-direction (s22), and (c) stress in the z-direction (s33).

Actually the y-direction stress component in the via shows compressive stress, although the x- and ydirection stress components still are tensile which is dominantly affected by the differences in thermal expansion coefficient of the substrate and that of the lines or via. Note that the stress along the y-direction is very high in the via. A via has relatively small dimen-

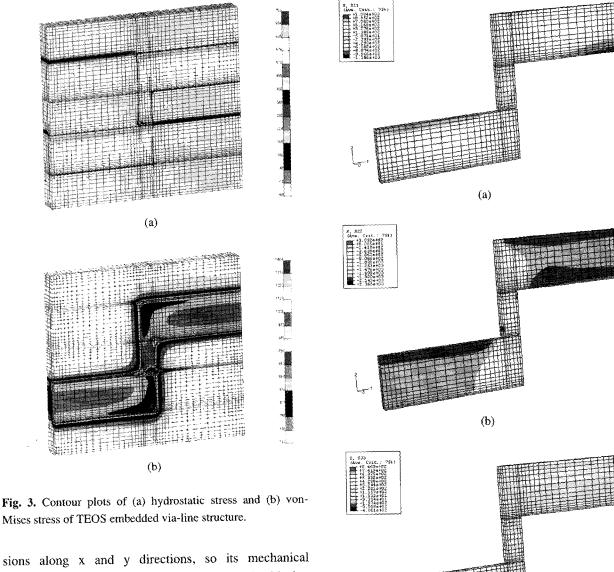


Fig. 3. Contour plots of (a) hydrostatic stress and (b) von-Mises stress of TEOS embedded via-line structure.

restriction by the substrate is small compared with that of the lines by the substrate which have larger dimensions along the x-direction. Therefore, thermomechanical properties of a via is dominated by the mechanical properties of the dielectric materials, and the large compressive stress is resulted in the SiLKembedded structures. The large compressive stress along the y-direction and the small tensile stress along the xand y-directions make the hydrostatic stress compressive and the von-Mises stress very large as shown in figures 5 (a) and (b). Since the hydrostatic stress of the via is compressive, void nucleation is thought to be difficult, while the plastic deformation could easily occur due to the large von-Mises stress.

Figure 6 is the hydrostatic stress and von-Mises stress distributions from the top of M2 to the bottom of the via

Fig. 4. The individual stress components of TEOS-embedded via-line structures in the form of contour plots; (a) stress in the x-direction (s11), (b) stress in the y-direction (s22), and (c) stress in the z-direction (s33).

(c)

for the TEOS-embedded and the SiLK-embedded structures. Hydrostatic stress in the TEOS structure was generally higher than that in the SiLK structures and the concentration center is the top of M2 and the bottom of the via. Meanwhile, the von-Mises stress of the SiLK structure was much higher than that of the TEOS

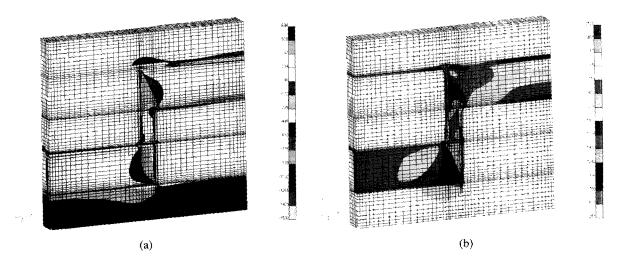


Fig. 5. Contour plots of (a) hydrostatic stress and (b) von-Mises stress of SiLK embedded via-line structure.

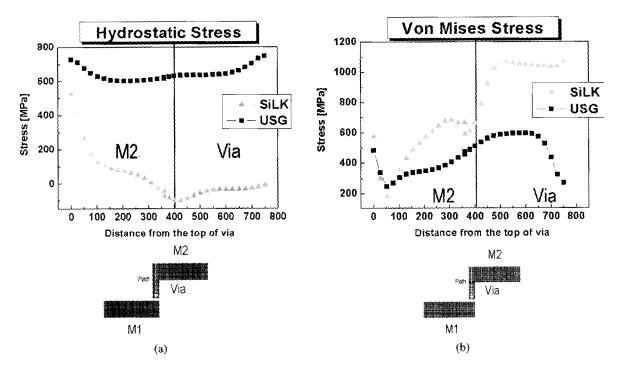
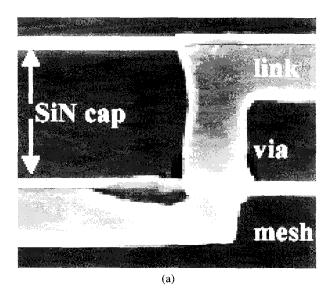


Fig. 6. Stress variation from the top of M2 to the bottom of the via for the TEOS-embedded and the SiLK-embedded structures; (a) hydrostatic stress and (b) von-Mises stress.

structures near the via. Therefore, the dominant failure mode of the TEOS structure will be void nucleation at the hydrostatic stress concentrated sites and its subsequent growth, while and that of the SiLK structure deformation of via due to large compressive stress along the y-direction.

IV. Discussion

Von Glasow et al. [11] observed two different failure modes of stress-induced voiding in the TEOS-embedded via-line structures as shown in Figure 7. They used two types of test structures: type A in which the source of



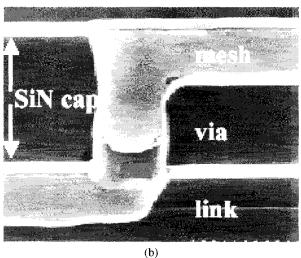


Fig. 7. Failure modes of stress-induced voiding in the TEOS-embedded via-line structures; (a) Type A: void formation at the top of M1 and (b) Type B: void formation at the bottom of the via [11].

supersaturated vacancies (designated as 'mesh' in Figure 7) is under the via, i.e. M1, and type B in which the source ('mesh' in Figure 7) is over the via, i.e. M2. In the type A structure, a stress-induced void formed in the M1, which grew along the top surface of the trenches. On the contrary, in the type B structure, a stress-induced void formed at the bottom of trenches.

This can be explained by our finite element analysis. A void can nucleate at the most stress-concentrated site only when there exists a vacancy source. However, in the type A structure, no void can be formed at the most stress-concentrated site, i.e. at the bottom of the via. It is

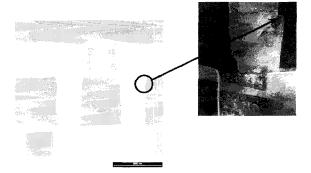


Fig. 8. Failure behavior of the SiLK-embedded via-line structures [12]; the via was deformed and the lower segment rose up with the respect to the slip plane which indicates that the deformation is due to the compressive stress in the via.

because the diffusion barrier layer such as Ta or TaN cuts off the vacancy diffusion path around the via. Therefore, the void is constrained to form at the second stress-concentrated site, i.e. at the top surface of the lines. Since the stress component in the x-direction is higher than that of any other direction, the void would grow along the top of the trenches. That's why an anisotropic void shape resulted in. On the other hand, in the type B structure, a void can form at the most stress-concentrated site, i.e. the bottom of the via. In this case, the void grows along the y-direction because its stress component is the highest. The von-Mises stress has a much higher magnitude along the corners between dissimilar materials, and its concentration centers seem to be correlated to the minor failure sites of the Figure 7.

Figure 8 shows the real failure behavior of the SiLK-embedded via-line structures [12]. It is noticed that the via was really deformed and the lower segment rose up with the respect to the slip plane, which indicates that the deformation is due to the compressive stress in the via as like our finite element analysis.

The experimental results and our finite element analysis tell that there are drastic differences in the failure mechanisms of stress-induced voiding between the Cu damascene structure built with a low-k material and that with TEOS dielectrics. Therefore, the proper selection of low-k materials for damascene Cu or the modification to the mechanical properties of the present low-k materials should be carried out from the integration point of view.

V. SUMMARY

Using a three-dimensional finite element analysis, the stress and its distributions of damascene Cu lines were calculated with two types of dielectrics and compared with the experimentally observed failure modes according to dielectric materials. In the case of integration with TEOS, hydrostatic stress was concentrated at the via and the top of the lines, where the void was suspected to nucleate. On the other hand, in the via-line structures integrated with SiLK, large von-Mises stress is maintained at the via, thus deformation of via is expected as the main failure mode.

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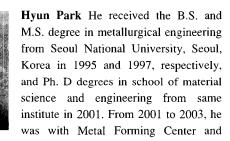
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interconnects.

Jong-Min Paik He received the B.S. and M.S. degree from Seoul National University in school of material science and engineering in 2000 and 2002, respectively, and currently is taking the doctoral course in the same institute. His main concerning is microstructure and stress related reliability of damascene Cu



Brain Korea 21 in Seoul National University, Seoul, Korea as post-doctoral researcher. In 2003, he joined Center for Microstructure Science of Materials in Seoul National University, Seoul, Korea. His main research field is microstructural evolutions in metallic materials including evolutions of grain structures and textures during deformation, recrystallization and grain growth in FCC metal wires, microstructure and stress in metal thin films, and abnormal grain growth mechanism in Fe-3%Si electrical steel.



Young-Chang Joo He received the B.S. and M.S. degree in metallurgical engineering from Seoul National University, Seoul, Korea in 1987 and 1989, respectively, and Ph. D degrees in electronic materials from Massachusetts Institute of Technology, Cambridge, MA, USA. His graduate work focused on

electromigration failure and reliability of Al interconnects.

From 1995 to 1997, he was with Max Plank Institute, Stuttgart, Germany as visiting scientist. From 1997 to 1999, he was with Advanced Micro Devices, Inc. (AMD), CA, USA as Senior Device Engineer working on reliability issues of Damascene Cu interconnects including electromigration and stress-migration. He joined Seoul National University, Seoul, Korea in 1999 and is currently a professor in school of material

science and engineering. His current research interests include electromigration and stress migration of damascene Cu and Cu-alloy interconnects, and Cu drift through low-k materials. He is also interested in reliability of electronic packaging including electromigration of solder bump and electrochemical migration.