Dual Edge-Triggered NAND-Keeper Flip-Flop for High-Performance VLSI

Jae-Il Kim and Bai-Sun Kong

Abstract— **This paper describes novel low-power high-speed flip-flop called dual edge-triggered NAND keeper flip-flop (DETNKFF). The flip-flop achieves substantial power reduction by incorporating dual edge-triggered operation and by eliminating redundant transitions. It also minimizes the data-to-output latency by reducing the height of transistor stack on the critical path. Moreover, DETNKFF allows negative setup time to provide useful attribute of soft clock edge by incorporating the pulse-triggered operation. The proposed flip-flop was designed using a 0.35 μm CMOS technology. The simulation results indicate that, for the typical input switching activity of 0.3, DETNKFF reduces power consumption by as much as 21 %. Latency is also improved by about 6 % as compared to the conventional flip-flop. The improvement of power-delay product is also as much as 25 %.**

Index Terms— **Low power, flip-flop, dual edge triggering, pulse triggered operation**

I. INTRODUCTION

Synchronous digital systems such as high-performance microprocessors and digital signal processors incorporate timing elements such as flip-flops and latches for storing temporal information available at every clock cycle [1]. Since timing elements are critical to the operation of these systems, they must be as simple as possible and satisfy various requirements such as low power consumption and rigid timing constraints [2]. Power requirement is becoming ever important, because the power consumption increases linearly with clock frequency while the power budget of high-performance portable digital systems is severely limited. Timing parameters such as data-to-output latency and setup and hold times are becoming equally important because the timing budget is getting tighter as the clock frequency approaches multi-GHz operating range. Some papers provide comparative analysis of latches and flip-flops commonly used in high-performance systems, and deal with the possibilities of trading off one for the other between speed and power [3].

Recently, various flip-flops have been proposed for achieving these goals. Hybrid latch flip-flop (HLFF) [4] shown in Fig. 1-(a) is popularly used for implementing high-speed digital systems due to relatively small data-to-output latency. However, the flip-flop can cause a large amount of redundant power consumption due to unnecessary precharge and discharge operations of internal nodes when the input retains a high logic value for more than one cycle. NAND-type keeper flip-flop (NDKFF) [5] shown in Fig. 1-(b) is proposed to address this issue, and eliminates redundant power consumption by using the NAND-type keeper circuit. However, the latency of the flip-flop is degraded because of reduced gate-source voltage of pull-down transistors on the critical path due to reduced clock swing. The NAND keeper pull-up transistor driven by the output also causes the pull-down transition to be slow due to signal fighting, further degrading the speed. This effect also leads to increased power consumption due to the short-circuit current during the fighting period. Finally, for both of the above flip-fops, the tallest transistor stack on the critical

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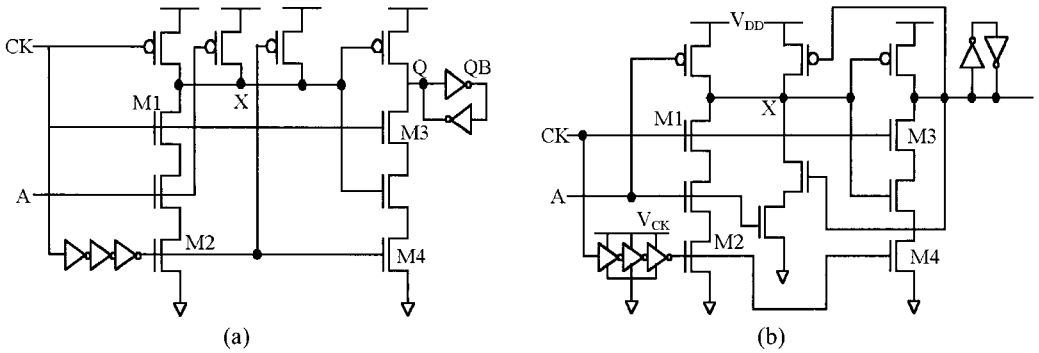

Fig. 1 Conventional flip-flops: (a) hybrid latch flip-flop (b) NAND-type keeper flip-flop.

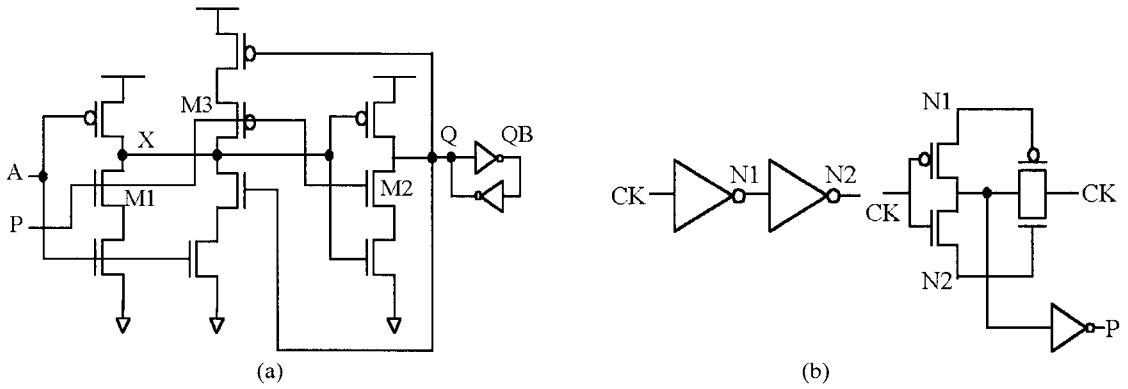

Fig. 2. Dual edge-triggered NAND-keeper flip-flop: (a) pulsed latch circuit (b) dual edge-triggered pulse generator.

path consists of three transistors in series, dictating use of large-sized transistors to avoid speed degradation.

To overcome these drawbacks, we introduce in this paper a novel flip-flop called dual edge-triggered NAND keeper flip-flop (DETNKFF). The flip-flop employs dual edge-triggered operation for clock power reduction and a modified NAND keeper to avoid problems stated above. Section II describes the circuit structure and operation of the proposed flip-flop. Relative advantages of using the flip-flop are also discussed in this section. Some simulation results are presented in Section III to assess the performance of the proposed flip-flop. Then, we draw the conclusion in Section IV.

II. Flip-flop Structure And Operation

Fig. 2 shows the schematic diagram of DETNKFF. The flip-flop is composed of a pulsed latch circuit and a dual edge-triggered pulse generator. The pulsed latch circuit shown in Fig. 2-(a) consists of two single-ended stages capturing the input data during the transparency period defined by a short pulse P, and a NAND keeper circuit modified from the original one in NDKFF by inserting transistor M3. The dual edge-triggered pulse generator generates the brief pulse signal for use in the pulsed latch circuit, which is synchronized at the rising and falling edges of the clock. The pulse generator can be shared by multiple pulsed latch circuits when a group of flip-flops are located closely. The operation of the proposed flip-flop is summarized as follows. Let us assume that input A was initially at a low logic value. Then, internal node X has a high logic value. Now, upon every incoming clock edges, the dual edge-triggered pulse generator activates pulse signal P for a short period of time, defining the transparency period. Then, if input A is low during this period, internal node X remains high and output Q is driven low. If the input stays low for multiple clock cycles, the internal node will retain the high logic value. On the other hand, if input A is high during the transparency period, node X transitions low, driving output Q to be high. In doing so, the pull-down

of X does not fight against the NAND keeper pull-up signal because transistor M3 is fully off. Once X is driven low, it remains low as long as the input is high. The NAND keeper pull-down circuit provides the ground signal for keeping X as a static node during the period in which the pulse signal is inactive. Only when the input is switched from high to low, X is pulled up to a high logic value and ready to be pulled down at subsequent clock edges.

The proposed flip-flop has several advantages over the conventional flip-flops. First of all, the flip-flop is triggered at both edges of the clock. We efficiently implemented dual edge-triggering operation using the pulse generator that generates a brief pulse at both clock edges. With this design, the opposite clock edge is no longer wasted and can be used for capturing a valid input data. Thus, clock frequency can be cut in half while preserving the rate of data processing. Using lower clock frequency translates into considerable power savings for the clocked portions of the circuit as well as for the clock distribution network. Use of explicit pulse generator can provide some additional advantages. For example, the pulse generator may be local to each flip-flop or shared among multiple flip-flops. Then, because the entire flip-flop needs not to be duplicated, the power and area overheads can be much less than for the conventional flip-flops. Use of NAND keeper also reduces power consumption by eliminating redundant transitions as in NDKFF. Namely, during the cycles in which the input stays high, no transition on X is noticed, making the power consumption of DETNKFF much less than that of HLFF. The proposed flip-flop is also attractive in terms of speed performance. In case of HLFF and NDKFF, the transparency period was implemented implicitly by incorporating both the clock and a delayed version of the clock into the pull-down paths. Transistor pairs M1-M2 and M3-M4 in Fig. 1-(a) and (b) are examples for this purpose. Hence, the height of transistor stack in each pull-down path must be at least three, degrading the pull-down speed. On the other hand, as for DETNKFF the brief pulse signal generated by the pulse generator explicitly defines the transparency period. Therefore, as can be seen in Fig. 2 the height of the tallest transistor stack of the pulsed latch circuit is just two, and thus, speed is expected to be improved and scale with technology. It is also noted that the modified NAND keeper in the proposed flip-flop totally eliminates signal fighting during the pull-down of X, leading to further speed improvement.

III. Comparison And Discussion

To evaluate performance advantage, the proposed flip-flop was designed using a 0.35 μm CMOS technology. The simulation was performed at typical process corners with supply voltage of 3.3 V at room temperature with 200fF load at the output. Fig. 3 summarizes the simulated waveforms of DETNKFF. Fig. 3-(a) depicts the brief pulse signal generated by the pulse generator at both clock edges. Fig. 3-(b) illustrates the case in which the output has a transition, where X transitions low and the output has a low-to-high transition. Fig. 3-(c) represents the case in which the output has no transition, where X stays low and the output remains at a high logic value. To compare the performance in terms of power consumption, the overall power consumption of HLFF

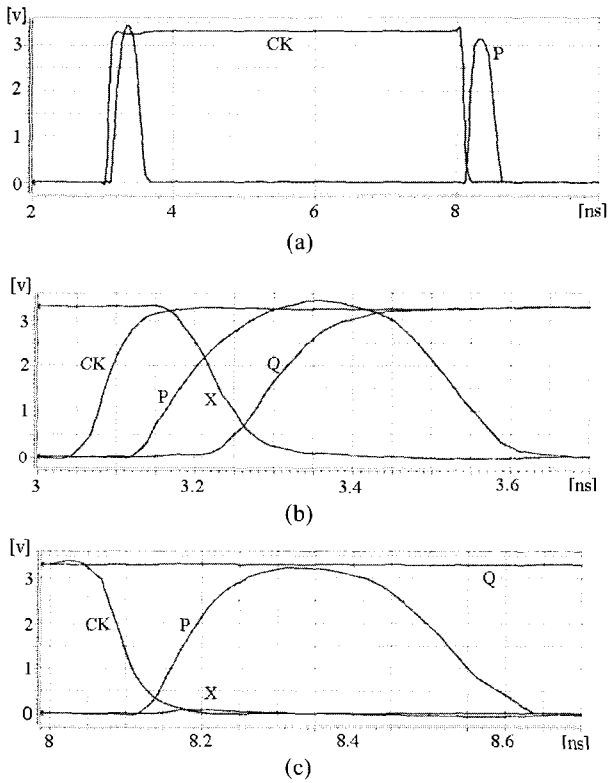

Fig. 3. Simulated waveforms: (a) for brief pulses at both clock edges (b) with low-to-high output transition (c) with no output transition.

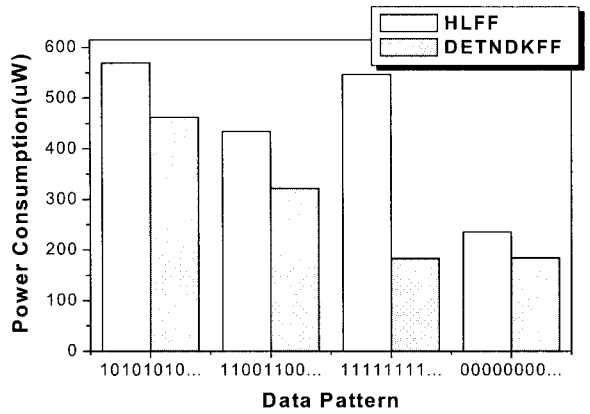

Fig. 4. Power consumption in terms of switching activity.

Table 1. Flip-flop characteristics.

	Device Count	Gate Width (μm)	D-Q Latency (ps)	Average Power (μW)	P*D Product (fJ)	Improvement
HLFF	20	95.9	260	336	87.4	-
DETNKFF	24	92.9	246	267	65.7	25%

and DETNKFF for different input patterns was simulated and plotted in Fig. 4. We applied four different data patterns to represent various input switching activity values. The sequence of ...01010101... represents the maximum input switching activity that reflects the maximum internal power consumption of flip-flops. The switching activity of 0.5 is represented by the sequence of ...00110011... Two other sequences, ...11111111... and ...00000000..., are used to represent the switching activity of zero because each flip-flop has somewhat different power distribution for each of these sequences. As shown by the figure, the proposed flip-flop consumes consistently less power for all the data patterns compared. Specifically, DETNKFF achieves the maximum power saving of about 67 % with all inputs high. For the remaining data patterns, the proposed flip-flop provides considerable power savings of around 18 ~ 20 %. Table 1 summarizes important flip-flop characteristics such as device count, total gate width, data-to-output latency, average power consumption, and the corresponding power-delay product. The data-to-output latency refers to the sum of the setup time and the clock-to-output latency. The average power consumption is measured with random input sequence having the switching activity of 0.3. As shown by the table, although the device count of the proposed flip-flop exceeds that of the conventional flip-flop, the former has less total gate width than that of the latter. This is mainly because the number of transistors on the critical path, having larger channel widths, is reduced due to reduced transistor stack. As far as the power consumption is concerned, which is measured with the average input switching activity of 0.3, DETNKFF achieves 21% reduction as compared to HLFF. Because the latency is also improved by about 6%, the improvement on power-delay product for a typical data switching activity is as much as 25%.

IV. Summary

In this paper, novel high-performance flip-flop is proposed. The flip-flop is synchronized at both clock edges and eliminates redundant transitions, leading to considerable reduction on power consumption. It also minimizes latency by reducing the height of transistor stack. In addition, the flip-flop has soft clock edge property to provide immunity to the uncertainty of clock arrival due to pulse-triggered operation. Simulation comparison indicates that the proposed flip-flop provides better performance in terms of power and speed.

Acknowledgement

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