Novel Robust Structure and High k Dielectric Material for 90 nm DRAM Capacitor

Y.K. Park, Y.S. Ahn, K.H. Lee, C.H. Cho, T.Y. Chung, and Kinam Kim

Abstract— **The robust stack storage node and sufficient cell capacitance for high performance is indispensable for 90 nm DRAM capacitor. For the first time, we successfully demonstrated MIS capacitor process integration for 90 nm DRAM technology. Novel cell layout and integration technology of 90 nm DRAM capacitor is proposed and developed, and it can be extended to the next generation DRAM. Diamond-shaped OCS with 1.8 um stack height is newly developed for large capacitor area with better stability. Furthermore, the novel Al_2O_3/HfO_2 dielectric material with equivalent oxide thickness (EOT) of 25 Å is adopted for obtaining sufficient cell capacitance. The reliable cell capacitance and leakage current of MIS capacitor is obtained with ~26 fF/cell and < 1 fA/cell by Al_2O_3/HfO_2 dielectric material, respectively.**

Index Terms— **Capacitor, Diamond-typed OCS, AlO/HfO, DRAM, DMO (Dual Mold Oxide)**

I. Introduction

As high density and high performance are required for a DRAM (Dynamic Random Access Memory) with a COB (capacitor Over Bit line) structure, cell capacitor technology needs to be developed to provide the required performance [1,2]. As the minimum feature size of DRAM decreases, it becomes more difficult to obtain sufficient capacitance of DRAM cell capacitor. Recently, DRAM with various cell capacitor structures, which apply 130 nm and 110 nm DRAM technology, was announced [3-6]. However, in future generation of DRAM manufactured with sub-0.1 um technology, the difficulty in realizing a sufficient cell capacitance and structural stability is expected. This results from remarkable decrease of cell dimension.

In 90nm DRAM capacitor, the maximization of cell area and the high K dielectric material is inevitable for obtaining sufficient cell capacitance. As shown in fig. 1, the stack height of 1.8 um and EOT of 25 Å is inevitable to get 25 fF per cell in the 90 nm design rule.

The higher storage node height causes instability of storage node structure, which is the cause of device failure due to the twin bit or multi-bit failure during DRAM operation [7]. Fig. 2 shows storage node bridge phenomenon due to the instability of the storage node structure. Therefore, the mechanical stability of the storage node structure is the key factor in increasing the cell capacitance.

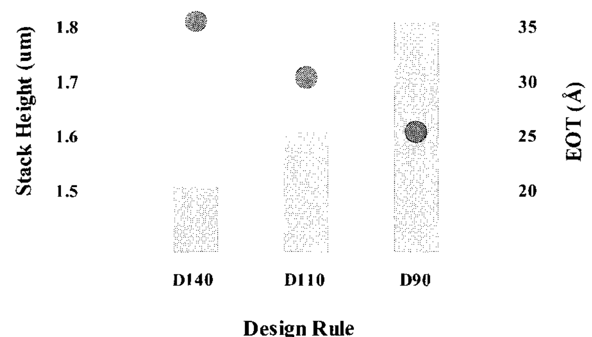

Fig. 1. Sufficient conditions for obtaining 25 fF cell capacitance with respect to design rule.

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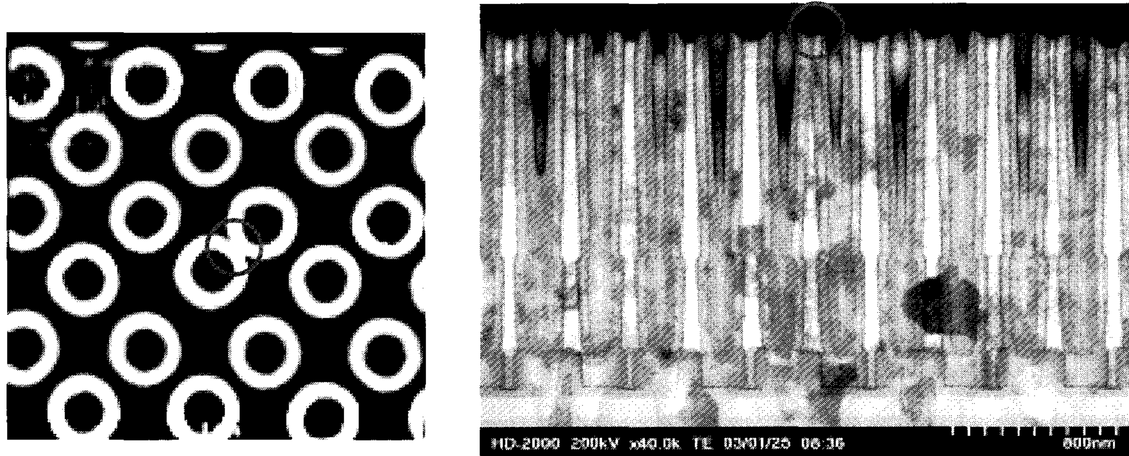

Fig. 2. Storage node bridge phenomenon due to the instability of the storage node structure.

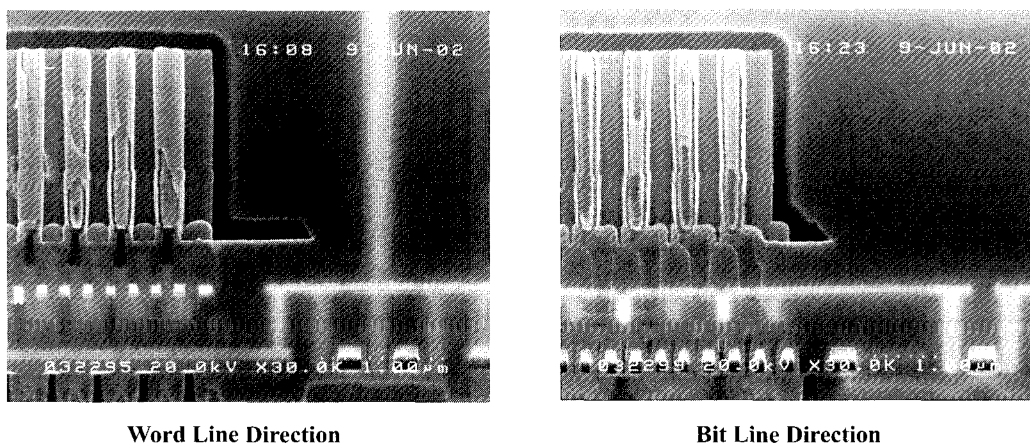

Fig. 3. Vertical structure of fully integrated 512 Mb DRAM using 90 nm process technology.

As reported earlier [6], the MIS Al_2O_3 capacitor has been considered as a promising candidate for the future capacitor. However, the EOT of Al_2O_3 capacitor for higher density DRAM device was limited to EOT 33 Å. Therefore, the high k dielectric material should be developed for next generation DRAMs.

In this paper, novel diamond-shaped cell layout and landing pad formation technology are proposed to overcome the decrease of cell capacitance and the mechanical instability, which is inevitable in small feature sized DRAM cell under 90 nm. At the same time, novel ALD (Atomic Layer Deposition) Al_2O_3/HfO_2 double-layer dielectric film with EOT of 25 Å is introduced for obtaining sufficient cell capacitance of DRAM cell.

II. EXPERIMENTAL

Fig. 3 shows the cross-sectional SEM images of fully integrated 512Mb DRAM cell array and its core interface area using 90 nm process technology. First, planar type cell transistors are formed, which is followed by S/D (Source/Drain) contact formation by SAC (Self Aligned Contact) process. After the patterning of BLs (Bit Lines), Storage Node (SN) contacts are formed also by SAC process [4].

To get robust capacitor structure for 90 nm DRAM technology, the newly proposed landing pad and diamond type OCS (one cylinder storage node) type cell capacitor structure are formed to obtain sufficient cell capacitance and mechanical stability. Using ArF photolithography, the critical patterns for landing pad are sharply defined with above 0.3 um DOF margin. Double

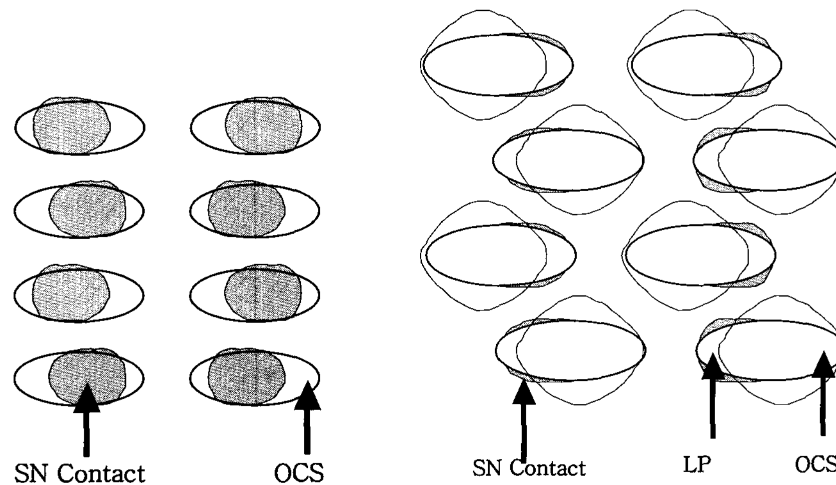

Fig. 4. Schematic diagrams of cell layout for (a) conventional OCS and (b) diamond-shaped OCS.

oxide layers such as BPSG (Boron Phosphorous Silicate Glass) and PETEOS (Plasma Enhanced Tetra-Ethyl-Ortho-Silicate) with different wet etching rates were deposited on the Si_3N_4 layer that served as the etch stopping layer during the storage node etch process. The double oxide layers were etched by anisotropic etching. The bottom area of the storage node was enlarged due to a different wet etch rate being used during the pre-cleaning process. A 400 Å thick poly-Si was deposited to form the OCS capacitor. The sacrificial oxide, double oxide, is removed by wet etching lift-off process.

Prior to film deposition on storage node with a cylinder structure, the phosphorus doped poly-Si substrate was nitridated by rapid thermal nitridation to prevent the oxygen penetration derived from the oxidant during the deposition process. The Al_2O_3 and HfO_2 were deposited at 350 ℃ by an ALD method. The reactant gas are TMA [$Al(CH_3)_3$], $Hf(OtBu)_4$ and O_3 for oxidant. After the HfO_2 film formation, post-treatment in an oxygen atmosphere was carried out to eliminate the contamination and cure oxygen defects. As a top electrode, TiN/poly-Si was deposited and activated as a plate.

III. Results And Discussion

Fig. 4 shows the schematic diagram of newly proposed diamond-shaped SN and landing pad, which enhances the stability of OCS type capacitor of DRAM cell. To maximize the cell area and enhance the mechanical stability of capacitor, novel cell layout is introduced. With this layout, the cell area can be increased than that of conventional cell layout. The cell capacitor structure was composed of SN contact and conventional oval-shaped OCS in the design rule over 100 nm. However, a conventional OCS has the asymmetry in distance to nearest OCS in the direction of bit line and word line, and is mechanically less stable in a special direction.

As the minimum feature size of DRAM cell decreases below 90 nm, the stability of this conventional OCS structure decreases drastically, which results in 2-bit

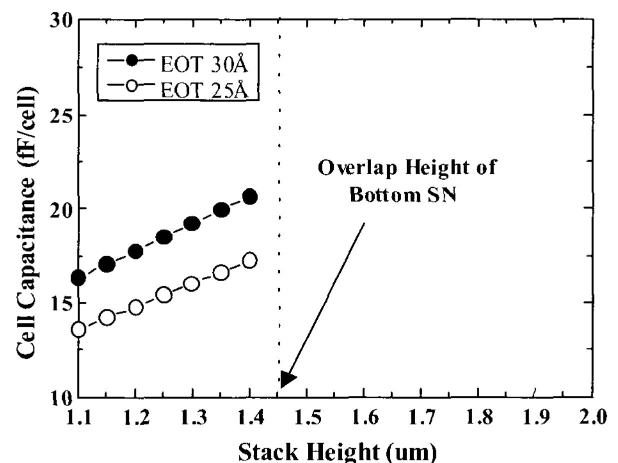

Fig. 5. Overlap margin and limitation of cell capacitance with conventional OCS structure.

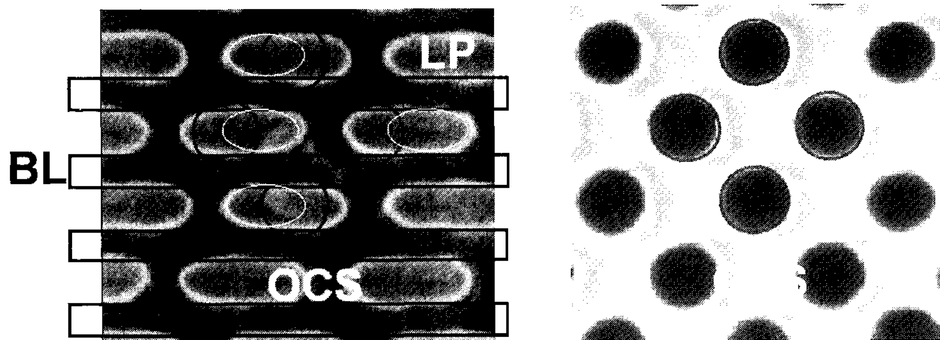

Fig. 6. Top-view SEM images of the landing pad (a) and OCS contact after the oxide inside OCS is etched out (b).

failure in the operation of DRAM. Moreover, if we solve the problem of mechanical instability, there are another problems such as limited stack height. The overlap of bottom SN limits the increase of the stack height in case of conventional OCS type structure. In our calculation, the overlap is occurred at the stack height of 1.45 um as shown in fig. 5. To overcome the mechanical instability and overlap issue of conventional OCS capacitor, diamond-shaped OCS is proposed in this paper, which needs the landing pad for connection between underlying SN contact and OCS itself.

Fig. 6 shows top-view SEM images of the landing pad (a) and OCS contact after the oxide inside OCS is etched out (b). With this diamond arrangement, we can eliminate the difficult patterning issue of conventional layout of storage node, which has rectangular shape. As a result, we can continuously use KrF photolithography to pattern the storage node even down to 90 nm technology. This structure enhances the process margin from the viewpoint of structural stability of OCS polycrystalline silicon, because the distances from one cylinder to the nearest cylinders are same.

Fig. 7 shows the cross-sectional SEM image of landing pad and bottom cell capacitor structure designed for DRAM cell with 90 nm technology. The storage node capacitor has diagonal arrangement where landing pad has orthogonal arrangement. Special poly pattern is used to connect the cell OCS to the landing pad.

Fig. 8 shows the cross-sectional SEM image of robust OCS structure with a stack height of 1.8 um. For achieving structural stability, DMO (Dual Mold Oxide) structure is adopted. The DMO structure utilizes the difference of etch rate between two materials against wet-chemical. Underlying high etch-rate oxide increases bottom size of cylinder and the cylinder of the DMO structure became more stable than that of the SMO (Single Mold Oxide) structure. In this paper, conven-

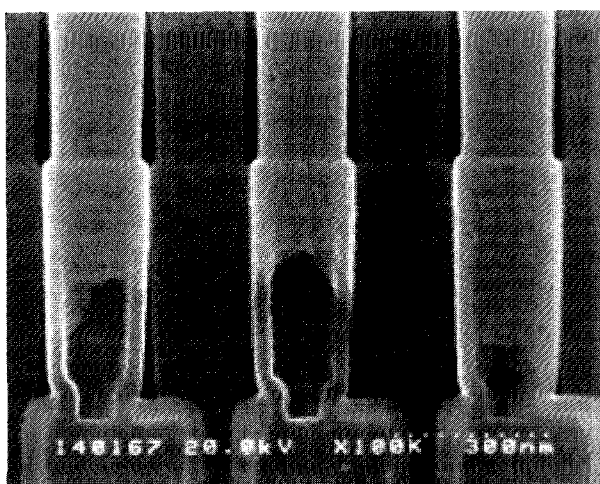

Fig. 7. Cross-sectional SEM image of landing pad and bottom cell capacitor structure designed for DRAM cell with 90 nm technology.

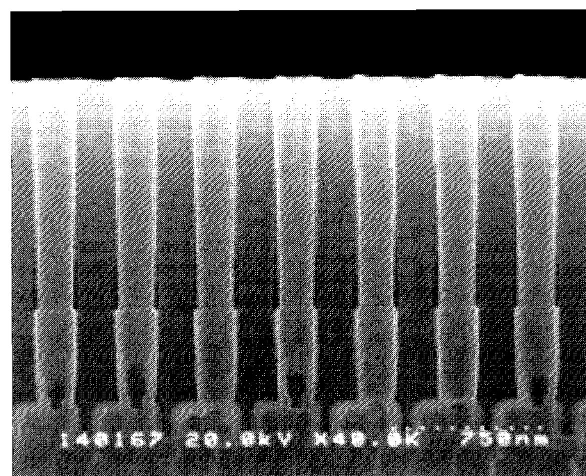

Fig. 8. Cross-sectional SEM image of robust OCS structure with a stack height of 1.8 um.

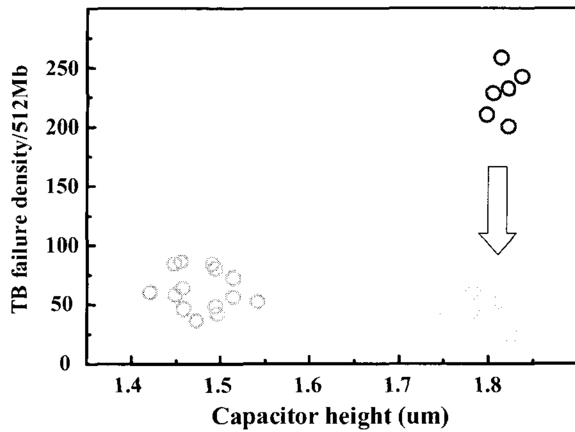

Fig. 9. Twin bit failure density per 512 M bit as a function of capacitor height.

tional BPSG and PETEOS films are used for first and second DMO materials, respectively.

Fig. 9 shows the twin bit failure density per 512M bit as a function of capacitor height. The twin bit failure density is strongly increased with the increase of stack capacitor height. To get reliable cell capacitance, it is inevitable to achieve the sufficient capacitor area by increased stack height. Furthermore, the process-induced heat budget is critical for twin bit failure. The OCS structure may become unstable after heat budget at capacitor dielectric deposition, pre-deposition treatment process, and post-deposition treatment process by the crystallization of SN polycrystalline silicon. By optimizing a deposition process of SN polycrystalline silicon and adopting novel capacitor process composed of DMO and novel diamond-shaped OCS, 2-bit failure density can be reduced to 25 % as shown in Fig. 9.

Fig. 10 shows cross-sectional TEM images of (a) overall SN of 1.8 um height with 90 nm feature size and (b) magnified top side SN. The step coverage of ALD

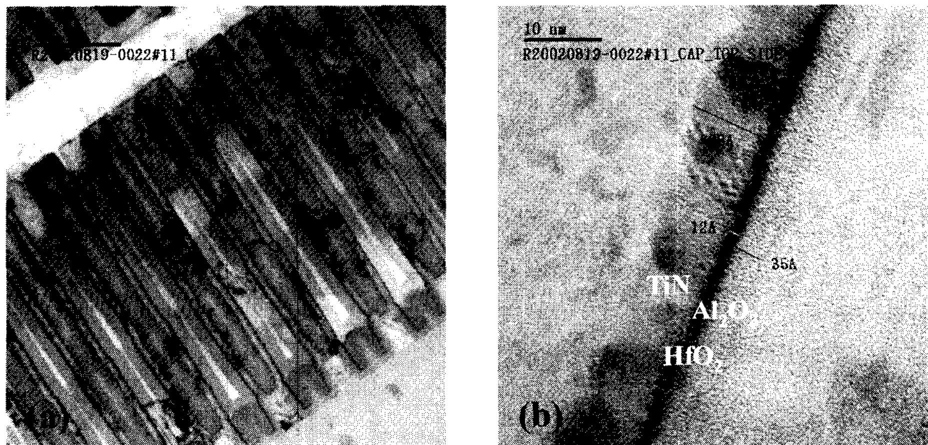

Fig. 10. Cross-sectional TEM images of (a) overall SN of 1.8 um height with 90 nm feature size and (b) magnified top side SN.

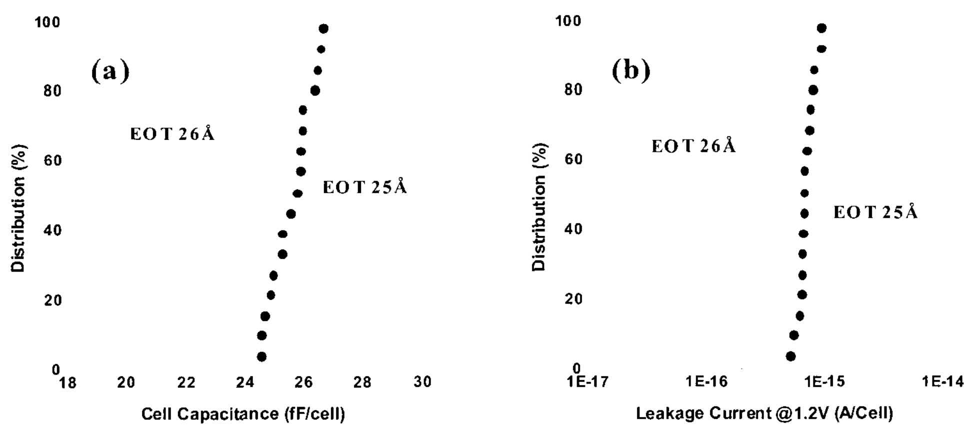

Fig. 11. Capacitance distribution and leakage distribution with respect to EOT scale down of DRAM cell capacitor with design rule of 90 nm.

Al_2O_3/HfO_2 double-layer dielectric with 1.8 um OCS height is over 90 %, which is applicable to DRAM with 90 nm technology node. The interfaces of Al_2O_3/HfO_2 and HfO_2/TiN were found to be both smooth and sharp, which means that interfacial reaction was not observed.

Fig. 11(a) shows the capacitance distribution of DRAM cell capacitor with design rule of 90 nm. The cell capacitance increases from 23.5 fF to 26 fF per cell by optimized ALD Al_2O_3/HfO_2 double-layer dielectric film with EOT (Equivalent Oxide Thickness) of 25 Å.

Fig. 11(b) shows the leakage distribution of capacitor dielectric film with respect to EOT scale down. The leakage current is less than 1 fA per cell even in EOT 25 Å with a good distribution in ALD Al_2O_3/HfO_2 films by optimized capacitor process. Therefore, it is possible to reduce EOT of Al_2O_3/HfO_2 capacitor around 25 Å while keeping stable leakage current.

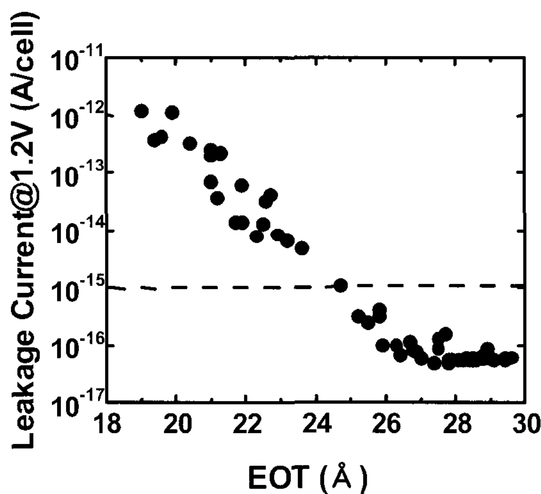

Fig. 12. Trend of leakage current at 1.2 V of MIS Al_2O_3/HfO_2 double-layer dielectric capacitor.

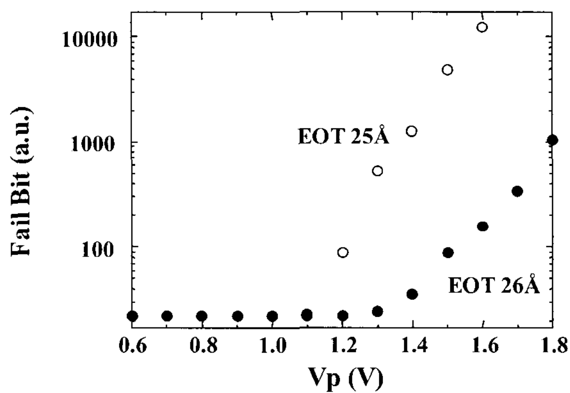

Fig. 13. Take-off Vp characteristics of Al_2O_3/HfO_2 capacitor with a respect to EOT scale down.

Fig. 12 shows the trend of leakage current at 1.2 V of MIS Al_2O_3/HfO_2 double-layer dielectric capacitor. It was possible to reduce the equivalent oxide thickness of Al_2O_3/HfO_2 double-layer in MIS capacitor to 25 Å with sub fA leakage level, which device applicable EOT to 90 nm design rule DRAM.

Fig. 13 shows the take-off Vp characteristics of Al_2O_3/HfO_2 capacitor with a respect to EOT scale down. The device functionality can be confirmed by Vp test for generating solid "0" 10 sec fail bit. The voltage for device operation is enough while this take-off Vp is decreased by 0.2 V for EOT 25 Å with compared with that of EOT 26 Å.

IV. CONCLUSIONS

In order to form cell capacitor of DRAM with design rule of 90 nm, the diamond-shaped OCS layout and landing pad scheme is proposed and realized by processes compatible with previous technology. Moreover, ALD Al_2O_3/HfO_2 double-layer dielectric film is adopted for the increase of cell capacitance and the enhancement of structural stability. As a result, cell capacitance of 26fF per cell, leakage current less than 1 fA per cell, and the twin bit failure density of 40 bit per 512 Mb chip are obtained.

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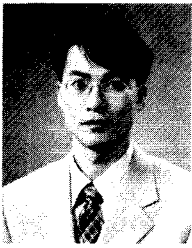

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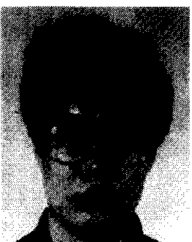

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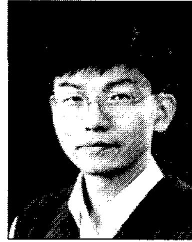

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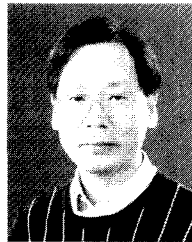

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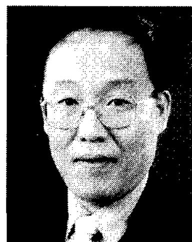

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