Data Retention Time and Electrical Characteristics of Cell Transistor According to STI Materials in 90 nm DRAM

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Abstract— **Cell transistor and data retention time characteristics were studied in 90 nm design rule 512M-bit DRAM, for the first time. And, the characteristics of cell transistor are investigated for different STI gap-fill materials. HDP oxide with high compressive stress increases the threshold voltage of cell transistor, whereas the P-SOG oxide with small stress decreases the threshold voltage of cell transistor. Stress between silicon and gap-fill oxide material is found to be the major cause of the shift of the cell transistor threshold voltage. If high stress material is used for STI gap fill, channel-doping concentration can be reduced, so that cell junction leakage current is decreased and data retention time is increased.**

Index Terms— **Data retention time, shallow trench isolation (STI), cell transistor, STI material, junction leakage current channel doping, DRAM**

I. Introduction

As the density of dynamic random access memory (DRAM) enters into the giga-bit era, it is essential for design rule to be scale down below sub-100 nm [1]. As design rule shrinks more down, short channel effect (SCE) increases and various device characteristics such as sub-threshold current and swing degrades [2]. The most critical issue is the decrease of threshold voltage and increase of sub-threshold current. Therefore the channel doping concentration should be increased in order to suppress short channel effects and minimize the sub-threshold leakage current. But high doping level leads to increase junction leakage current. After all, it will decrease retention time.

Recently, data retention time nearly doubles with each successive generation due to the need for high density, high speed and low power DRAMs [3]. The electric field in memory cell's storage node junction boundary is becoming stronger and leakage current has been increasing with each generation, resulting in poor retention characteristics. Retention time is projected to be an even more serious problem.

Process integration with design rule of sub-100nm, has a lot of problems. One of the serious problems in sub-100 nm process is shallow trench isolation (STI)

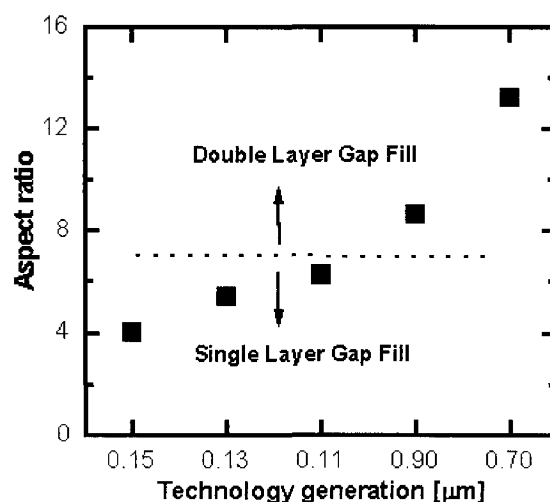

Fig. 1. Trend of STI gap fill aspect ratio according to technology generation.

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gap-fill process. Fig. 1 shows STI aspect ratio according to technology generation. To fill STI gap with high aspect ratio, multi-step deposition of high-density plasma (HDP) oxide or flowable oxide such as spin-on-glass (SOG), O3-TEOS are required. In this study, we used HDP oxide and poly-silazane (P)-SOG oxide as the gap-fill material and they are compared in characteristics of cell transistor. Behaviors of cell transistor's threshold voltage and junction leakage current are studied with different gap-fill materials. And, data retention time is also discussed.

II. FABRICATION PROCESS

Fig. 2 shows major process sequence for DRAM fabrication. Process sequence is as following. First, the

- Active Patterning
- Trench Etching
- STI Gap Fill Process
- Cell Vth Ion Implantation
- Gate (Poly + WSix) Patterning
- S/D N- Ion Implantation
- Gate Spacer & ILD1 Process
- S/D Pad Formation
- BL Formation
- Cap Process
- Metal Formation

Fig. 2. Major process sequences for fabrication of DRAM.

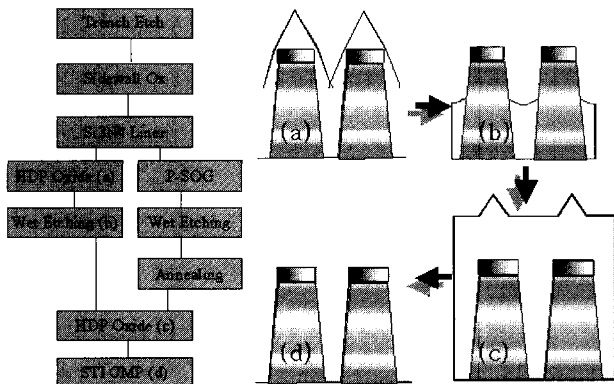

Fig. 3. Process flow for STI gap fill and schematics.

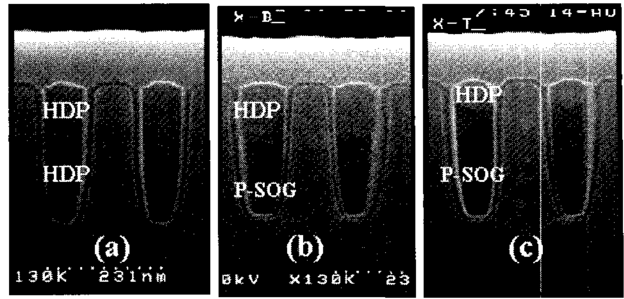

Fig. 4. Vertical SEM photograph of finally STI gap fill process using double HDP oxide (a) and P-SOG+HDP structure (b) and (c).

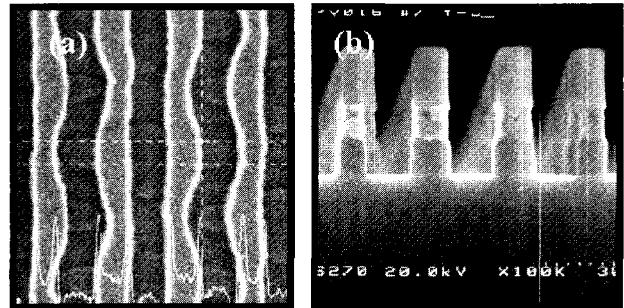

Fig. 5. Top view (a) and vertical SEM photograph (b) after gate etch of cell array region.

active region is defined on the silicon substrate by photolithography and etching process. After trench etching, sidewall oxidation and LPCVD Si3N4 liner was deposited such as shown Fig.3. Sequentially, double oxide layer process was used to make a void free STI structure. First, gap-fill layer was either HDP oxide or P-SOG oxide. Then proper amount of first oxide on active Si3N4 mask was chemically removed by wet etching process and exposed over-hang point around Si3N4 mask. In case of P-SOG oxide as the first oxide layer, 650 °C wet annealing was added to change the P-SOG layer into stable SiO2 [4]. Finally, second HDP oxide layer was deposited and chemical mechanical polishing (CMP) was used to make a planar surface. Fig. 4 shows cross-section of STI structure after deposition of gate poly-silicon. STI with P-SOG+HDP process shows clear wet boundary but STI with HDP+HDP process does not. To study the effect of P-SOG oxide gap-fill amounts on cell transistor's behavior, wet etch time was split into two conditions. After STI process, ion implant processes were executed to form well and to control transistors threshold voltage.

Dual gate oxide process was adopted to cover various

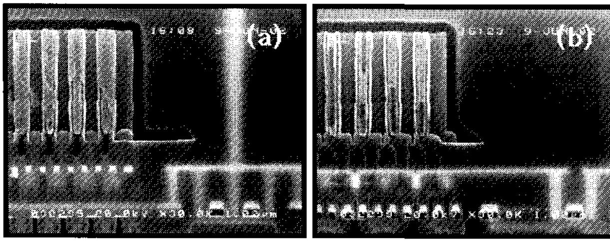

Fig. 6. Cross-sectional SEM photographs of (a) word line direction and (b) bit line direction in cell to core region.

performances of various transistors. For gate formation, 80-nm poly-silicon layer, 100-nm WSix layer, 180-nm Si3N4 layer were deposited. Following photo process and etching process defined gate patterns. Fig. 5 shows top view and cross-sectional view of cell array transistor after gate etching. Gate length of cell array with 512M-bit density was about 95-nm. The source/drain extension is formed by implantation. The gate spacer in formed using Si3N4 layer. We deposit the interlayer dielectric (ILD) and use CMP to form a flat surface of ILD in order to provide a sufficient depth of focus (DOF) margin for following photolithography process. The source and drain regions of cell transistors are etched by using a self-aligned contact (SAC) etching process, and an N-type dopant is implanted through the SAC openings, to reduce the contact resistance. The elevated source and drain contact pads are formed by deposition of doped poly-silicon, and the contact pads are separated by using a CMP process After that, bit line process, cap process and metal process are followed to complete the DRAM as shown Fig. 6.

III. RESULTS AND DISCUSSION

Cell junction leakage current is composed of three major components as shown Fig. 7. First one is channel surface (i.e. Si-SiO2 interface) region induced leakage current, ISUR. Second one is STI sidewall region leakage current, ISTI. Third one is junction bulk depletion leakage current, IBULK. As the design rule shrinks, the thickness of gate oxide scales down to compensate SCE and gated-induced drain leakage (GIDL) current increases. GIDL is dependent on gate etch and re-oxidation condition. This process dependent GIDL current has a strong relation with data retention time [5]. DC (bit-line contact) junction leakage current,

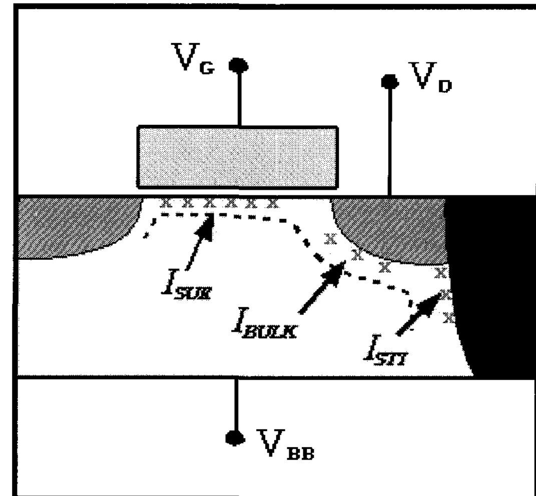

Fig. 7. Schematic cross-section view of three components in the cell junction leakage current.

shown in Fig. 8, is sum of ISTI and IBULK leakage current. This DC junction leakage is dependent on first gap-fill material and increases with increased amount of HDP oxide than that of P-SOG oxide. HDP oxide and P-SOG oxide, both have compressive mechanical stress, but P-SOG oxide has less stress than HDP oxide because of its lower density. Fig. 9 shows shear stress characteristics of using HDP oxide and P-SOG oxide material. It is simulated by TSUPREM4. This less stress on bulk silicon reduces leakage current. As the P-SOG oxide amount in STI region increases, total stress on bulk silicon is reduced and DC leakage current also decreases. BC (storage node contact) junction leakage current, which is shown in Fig. 8, is mostly composed of ISUR. Accordingly, BC junction leakage current is not changed for different STI gap-fill materials. ISUR is dependent on Electric (E)-field in BC junction edge and this E-field has little dependency with STI gap-fill material. Fig. 10 shows E-field contour simulation result with following bias condition Vds=3.5 V, Vbb=-0.7 V, Vgs=0 V. The simulation shows largest E-field value under gate edge and this value increases as deign rule scales down. With increased E-field, BC leakage current will increase and data retention time will decrease. For longer data retention time, channel and source/drain junction structure should be optimize as design rule decreases and it is not going to be further discussed in this paper.

Threshold voltage of cell transistor is dependent on STI gap-fill materials and P-SOG oxide volume. If STI

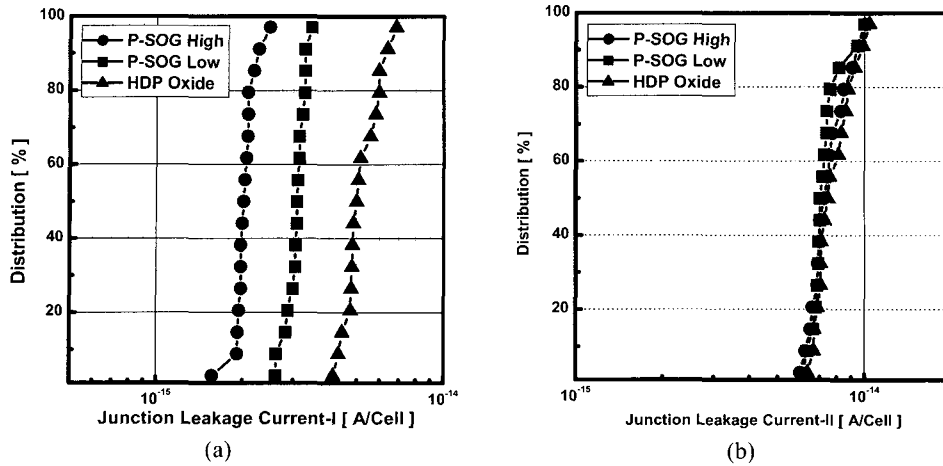

Fig. 8. Comparison of cell DC(a) and BC(b) junction leakage current according to STI gap fills material and P-SOG thickness at same dose.

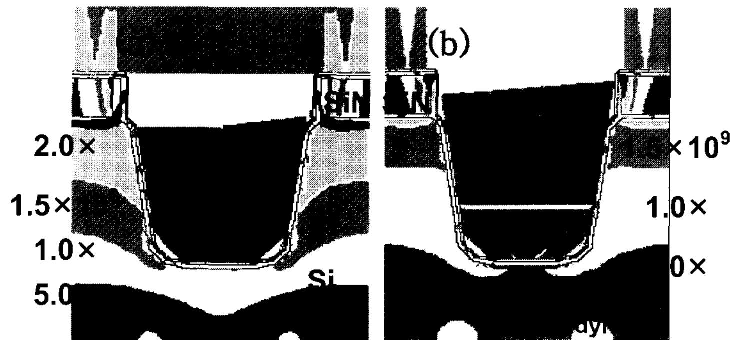

Fig. 9. Simulation shear stress contour of (a) STI HDP and (b) STI HDP+P-SOG.

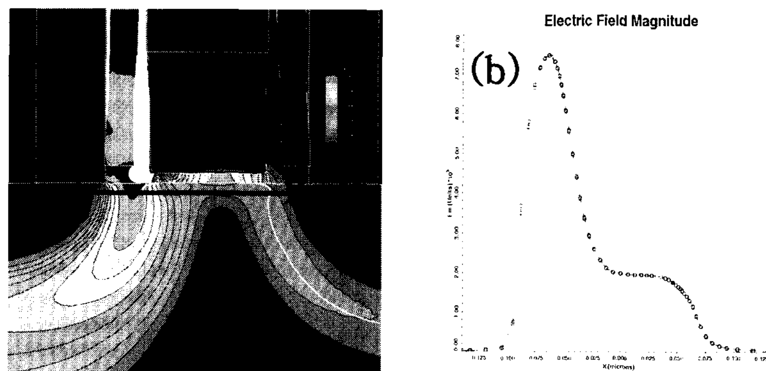

Fig. 10. E-field simulation with cell transistor at Vds=3.5 V, Vbb=-0.7 V and Vgs=0 V. (a) E-field contours, (b) cross-sectional view of E-field magnitude.

gap is filled only with HDP oxide, threshold voltage of cell transistor is largest. And threshold voltage decreases as P-SOG oxide amount increases. If P-SOG oxide amount in STI region increases, stress in bulk silicon decreases. And this less stress in silicon is helpful for enhancing out-diffusion of boron, channel dopant, during following heat process such as gate oxidation or re-oxidation. With same channel ion implant dose, the larger volume of P-SOG oxide decreases the threshold voltage of cell transistor. Oxide with larger stress, such

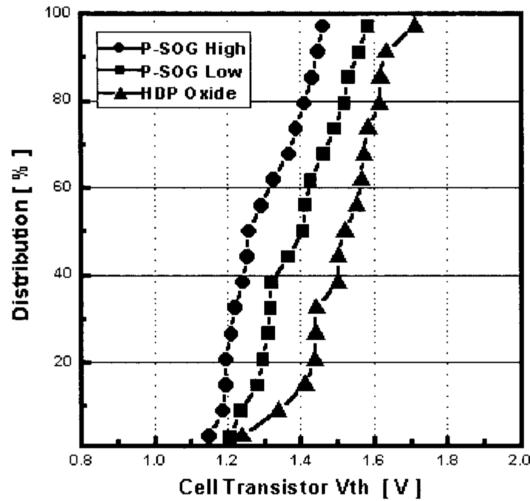

Fig. 11. Comparison of cell transistor Vth according to STI gap fill material and P-SOG thickness at same channel dose.

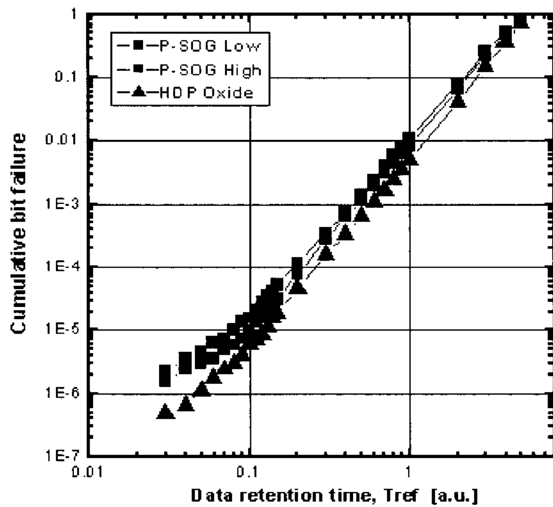

Fig. 12. Date retention curves of samples with different STI gap fill material and P-SOG thickness conditions at same cell TR Vth.

as HDP oxide, in STI region will increase threshold voltage of cell transistor for same ion implant dose, as shown Fig. 11.

Consequently, channel ion implant dose amount can be decreased to achieve target threshold voltage. And less channel ion implant dose will decrease defect density in junction boundary of cell transistor and thereby increase data retention time in DRAM [6]. Fig. 12 shows data retention time with same cell transistor threshold voltage. Compared with P-SOG oxide filled STI, HDP oxide filled STI needs smaller amount of channel ion implant to have same threshold voltage level. Consequently, this cell transistor has longer data retention time.

VI. Conclusion

Data retention time of 90 nm cell transistor with 512M-bit density DRAM can be improved with HDP oxide gap-fill in STI region. If STI region is filled with larger stress oxide, cell transistor threshold voltage is increased and channel ion implant dose can be reduced to achieve target threshold voltage. This less channel dose will increase data retention time.

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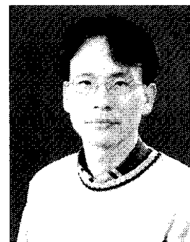

Soo-Ho Shin received the B.S. and M.S. degrees in electronic engineering from Koomin University, Seoul, Korea, in 1994 and 1996 respectively. In 1996, he joined Semiconductor R&D Center, Samsung Electronics Company, Ltd., Gyungki-Do, Korea, where he has been involved in the development of 512M DRAM with 90nm minimum feature size. His current interests are sub-100nm memory cell technology and metal gate process.

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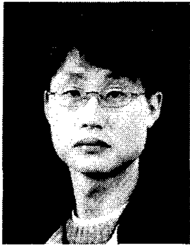

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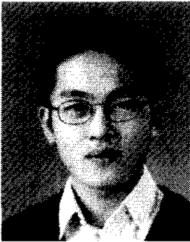

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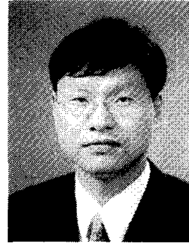
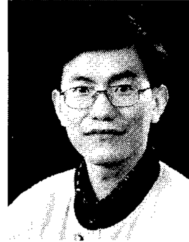


been involved in the development of 512M DRAM with 90nm minimum feature size. His current interests are sub-100nm memory cell technology and metal gate process.



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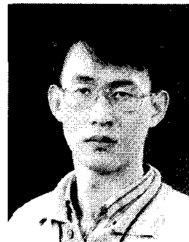

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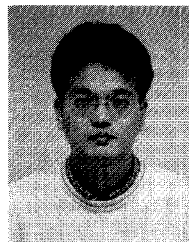

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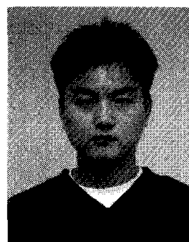

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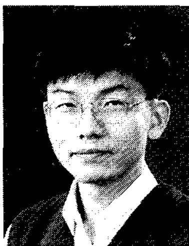

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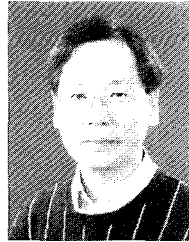

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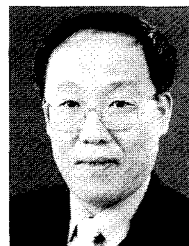

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