# On-chip Smart Functions for Efficiency Enhancement of MMIC Power Amplifiers for W-CDMA Handset Applications

**Youn S. Noh, Ji H. Kim, Joon H. Kim, Song G. Kim, and Chul S. Park**

*Abstract*—**New efficiency enhancement techniques have been devised and implemented to InGaP/GaAs HBT MMIC power amplifiers for W-CDMA mobile terminals applications. Two different types of bias current control circuits that select the efficient quiescent currents in accordance with the required output power levels are proposed for overall power efficiency improvement. A dual chain power amplifier with single matching network composed of two different parallel-connected power amplifier is also introduced. With these efficiency enhancement techniques, the implemented MMIC power amplifiers presents power added efficiency (PAE) more than 14.8 % and adjacent channel leakage ratio(ACLR) lower than –39 dBc at 20 dBm output power and PAE more than 39.4% and ACLR lower than –33 dBc at 28 dBm output power. The average power usage efficiency of the power amplifier is improved by a factor of more than 1.415 with the bias current control circuits and even up to a factor of 3 with the dual chain power amplifier.**

*Index Terms*—**Power Amplifier, Efficiency, HBT, MMIC, W-CDMA**

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## I. INTRODUCTION

RF power amplifiers are critical components that almost dominate a talk-time of mobile handsets. W-CDMA is one of the leading standards for the 3G wireless communication systems and adopts spectrally efficient HPSK (hybrid phase shift keying) as a digital modulation scheme. But HPSK has inevitably a non-constant envelope, requiring high linearity. Power amplifiers also need high efficiency characteristic over wide output power range for the W-CDMA systems, and the most probable output power is not a maximum output power but ranges from –20dBm to 20dBm. A back-off of the output power to the most probable output power makes a significant decrease in efficiency. Therefore both high linearity and efficiency are required at the same time for the W-CDMA applications. High linearity techniques were reported with on-chip linearizers[1],[2] in our group. These techniques used base emitter voltage predistortion for the high power injection improving gain compression and phase distortion of the amplifier. Recently, the techniques drawing high efficiency around the most probable output power range are emerging as one of the most significant issues in designing mobile handset power amplifiers. In order to increase the PAE at the low output power level, there were several reports using DC-DC converters [3]-[5]. However, integrating the DC-DC converter for a variable bias supply voltage results in a significant increase of the chip size and cost, which make the DC-DC converter not suitable for the mobile handset power amplifiers. Automatic bias control (ABC) system was

proposed to decrease a quiescent current at low output power levels [6]. Since the ABC-chip is separately needed in addition to the amplifier MMIC, the module size of the power amplifier increases. In this work, newly proposed MMIC smart power amplifiers, two types of the quiescent current selection circuits and a dual chain power amplifier, are described. Quiescent current selection circuits are implemented with on-chip bias control circuit switching the quiescent current level between high and low power mode. The amplifiers are operated in a Class AB(near Class B) mode at the high(low) output power level. The near Class B operation at the low output power level improves the PAE effectively with the reduced quiescent current. The dual chain power amplifier with single input and output matching networks is implemented with parallel integrating two power amplifiers for low and high power modes. Low quiescent current of 15mA at the low power mode operation shows remarkable improvement of the PAE.

## II. Bias Current Controlling Circuits

Biasing at the low quiescent current for the HBT power amplifier is the most basic method for high efficiency at the low output power level. Figure 1 shows an I-V characteristic of a HBT with two different bias points of Class AB and near Class B.

The power amplifier biased at Class AB operates as a HPM (High Power Mode) for the high output power region. Bias switching from Class AB to near Class B

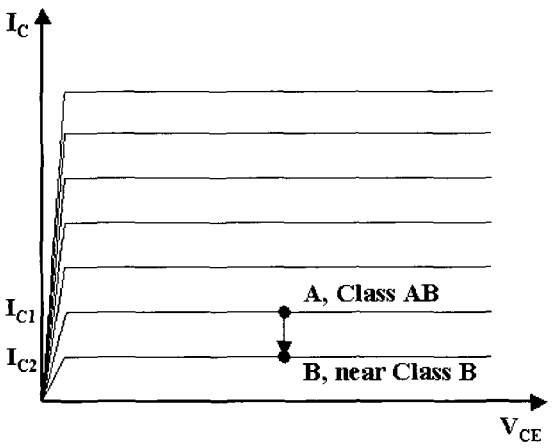



**Fig. 1** Current-voltage characteristic of a HBT.

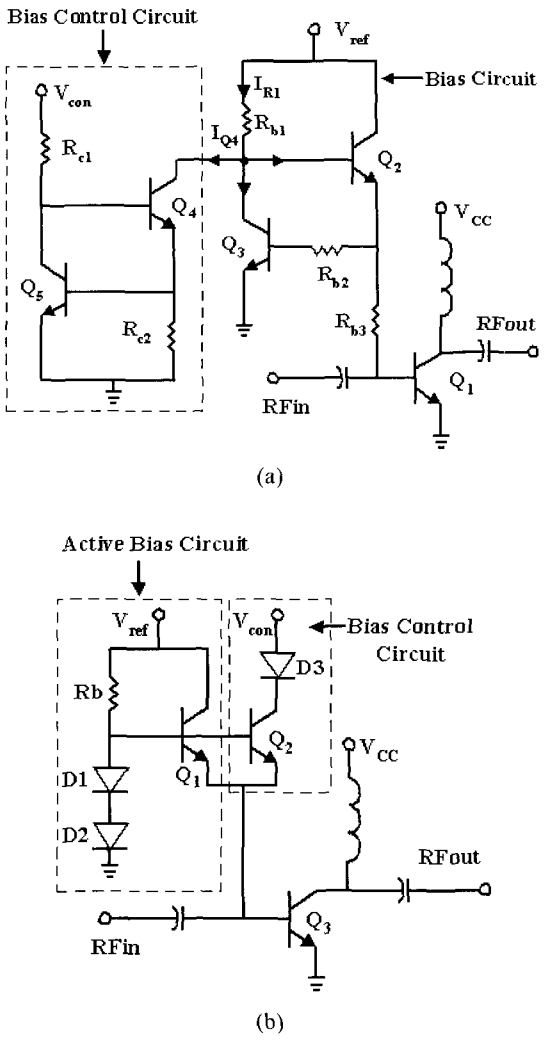



**Fig. 2** Schematic diagram of the bias current control circuits (a) of current bypass structure and (b) of current injection structure.

for LPM (Low Power Mode) operation results in high efficiency with trading off the linearity of the amplifiers. For a switching mode operation of the power amplifier, we devised two types of integrated bias current control circuits (Figure 2).

### A. *Bias current control circuit of current bypass structure*

Figure 2 (a) shows the schematic diagram for the bias control circuit of current bypass structure, which turns on and off the bypass path of the bias control circuit according to the Vcon logic signal. The outlined box represents a current mirror using the base-emitter voltage, $V_{BE}$, of the HBT as a reference. When the control signal

of Vcon is as low as 0 V, the transistors Q4 and Q5 will be off, resulting in $I_{Q4}$ current of 0 mA. Therefore, the bias controlling circuit does not draw any current from the bias circuit, which enables the RF transistor Q1 to operate with a high quiescent current like the bias point A in the Figure 1. Consequently, the state of the power amplifier enters the "High power mode". When the bias control circuit is turned on with the control signal of Vcon, the two transistors Q4 and Q5 will be switched to normal bias mode. Even though $I_{R1}$ increases slightly compared to the high power mode because of the drawn current of $I_{Q4}$, the collector current of a transistor Q2 decreases, which causes reduction of a quiescent current of the RF transistor Q1. The bias control circuit enables the transistor Q1 to operate with a low quiescent current like the bias point B in the Figure 1. As a result, the state of the power amplifier enters the "Low power mode." The devised bias control circuit shows two figures of merit as followed: (1) the bias control circuit scarcely uses additional chip area and dc power consumption, (2) there is no power loss associated with mode switching operation. The overall current variation of $I_C$ is simulated as small as 1.6 mA when the Vcon value fluctuates as much as 0.5 V.

### B. *Bias current control circuit of current injection structure*

Figure 2 (b) shows the schematic diagram for the bias controlling circuit of current injection structure, which controls the amount of bias current to the base of RF amplifier through an extra current path according to the Vcon logic signal. An active bias transistor Q1 in the active bias circuit supplies a constant base current to the amplifier transistor Q3 regardless of the Vcon logic state. A collector of an active bias transistor Q2 in the bias control circuit is connected through a diode D3 to the Vcon, and the Q2 determines the power amplifier operation as following;

1) Low power mode (Vcon low, 0V ~ 0.5V) : The $V_{CE}$ of the Q2 becomes to 0 V and the Q2 can't supply current to the base of the Q3. Therefore, only Q1 supplies current to the base of the Q3, and the amplifier Q3 is biased in the near Class B condition (point B in the Figure 1).

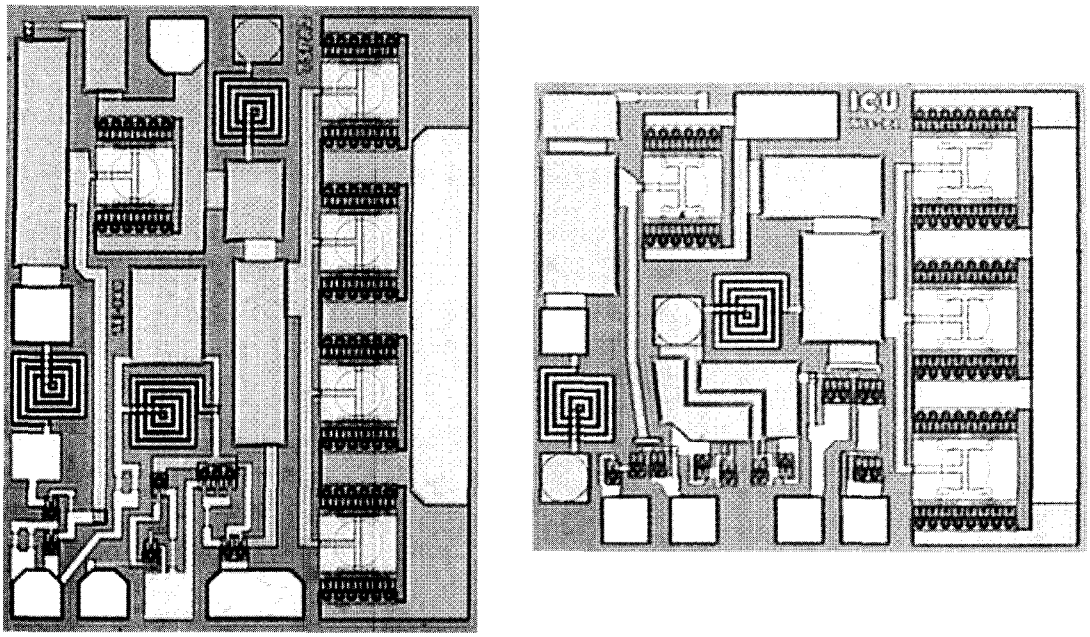
2) High power mode (Vcon high, 2.8V ~ 3.3 V) : The $V_{CE}$ of the Q2 is larger than the knee voltage of the HBT, and the Q2 can supply current to the base of the Q3. Therefore, both Q1 and Q2 supply current to the base of the Q3, and the amplifier Q3 is biased in the Class AB (point A in the Figure 1). The diode D3 prevents the saturation operation of Q2 when Vcon is low. Without the diode D3, the Q2 is operated in a saturation region, resulting a high voltage drop through a resistor Rb, then, the Q1 and the Q3 are turned down. The integrated bias current control circuit 2 has features of no additional dc current consumption, no insertion power loss for switching, almost no increase in chip area, and insensitive to the variation of the control signal.

## III. Dual Chain Power Amplifier

The power amplifier has been devised with two different parallel-connected InGaP/GaAs HBT power amplifiers, emitter area of each amplifier is fitted to different maximum power values in order to maximize PAE at appropriate output power levels: one to 17.5 dBm for low power mode and the other to 28 dBm for high power mode. One of the amplifiers appropriated to the selected power mode is activated through the bias selection while the other is disabled, and the dedicated matching network between parallel-connected amplifiers transfers the signal power along the selected chain preventing power leak to the disabled amplifier. We have designed and fabricated the dual chain MMIC power amplifier with single matching network, of which power added efficiency for 16 dBm output power is as much as 21%, which results in a factor of 3 improvement of an average usage efficiency [7].

## IV. Implementation To The Mmic Power Amplifiers

Two-stage InGaP/GaAs HBT MMIC smart power amplifiers applying each bias current control circuit are designed using multiple fingers of unit transistor of 60 $\mu m^2$-emitter-area InGaP/GaAs HBT : 2,880 $\mu m^2$ for the power stage and 720 $\mu m^2$ for the driver stage. The fabricated MMIC power amplifiers with the two different bias current control circuits are shown in Figure 3, and the chip size are as small as 0.76x1.03 $mm^2$ for



(a) (b)

**Fig. 3** Photograph of the two-stage smart power amplifier MMICs with the bias current control circuits (a) of current bypass structure and (b) of current injection structure.

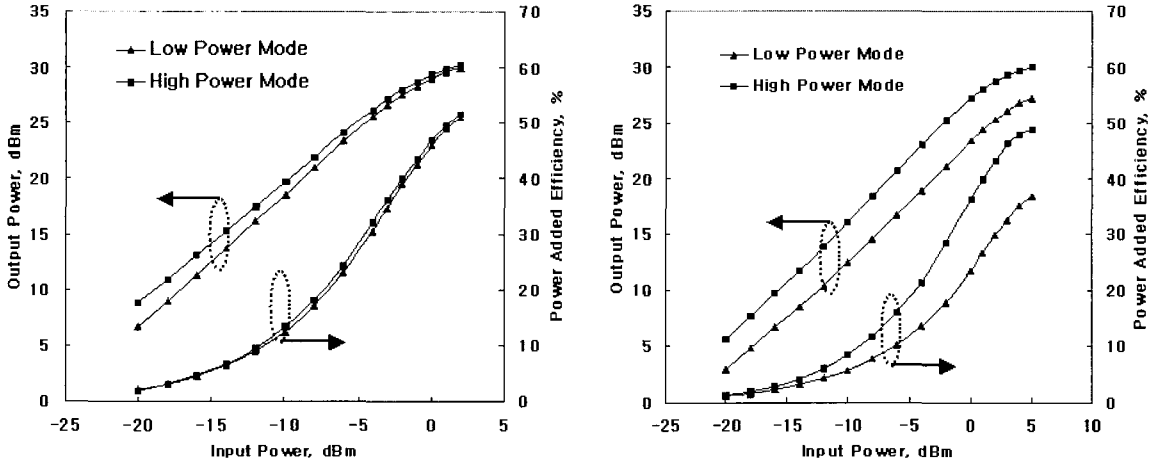



**Fig. 4** Measured output power and power added efficiency of the two-stage smart power amplifier MMICs with the bias current control circuits (a) of current bypass structure and (b) of current injection structure.

the circuit with current bypass bias circuits and 0.89x0.75 $mm^2$ for that with current injection bias circuit, both including input matching, interstage matching, bias circuits, and the bias current control circuits.

Figure 4 shows the measured output power and power added efficiency of the two-stage smart power amplifiers with each bias current control circuit. The MMIC with current bypass bias circuit operates with the total quiescent current of 44(94) mA for LPM(HPM) operation, and exhibits the output power of 29.65(29.92) dBm and PAE of 49.12(49.68) % for LPM(HPM) operation. Gain expansion up to 3dB was observed for

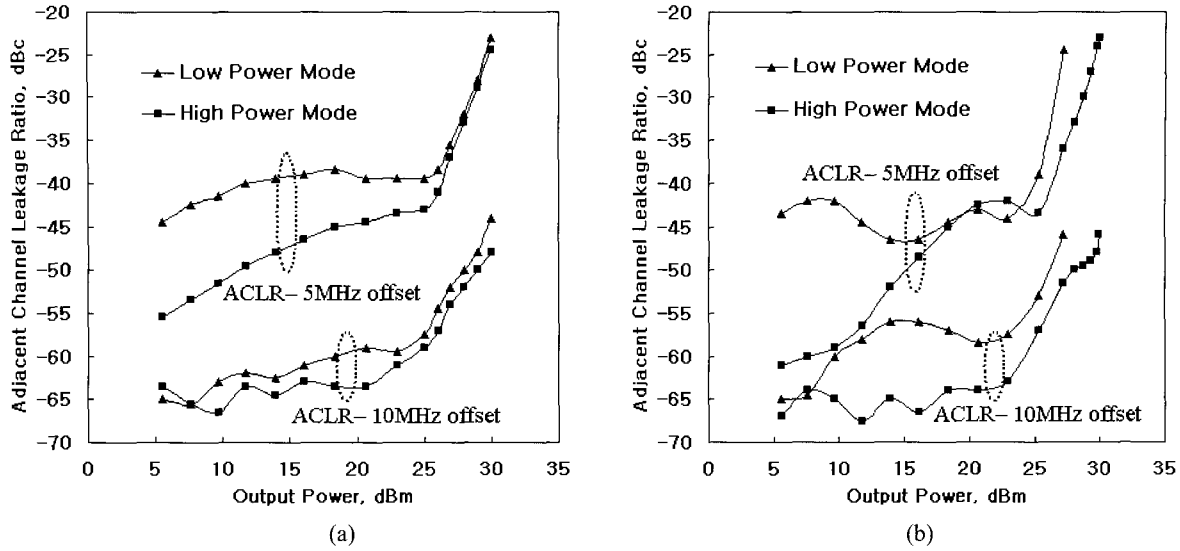



**Fig. 5** Measured ACLR of the two-stage smart power amplifier MMICs with the bias current control circuits (a) of current bypass structure and (b) of current injection structure.

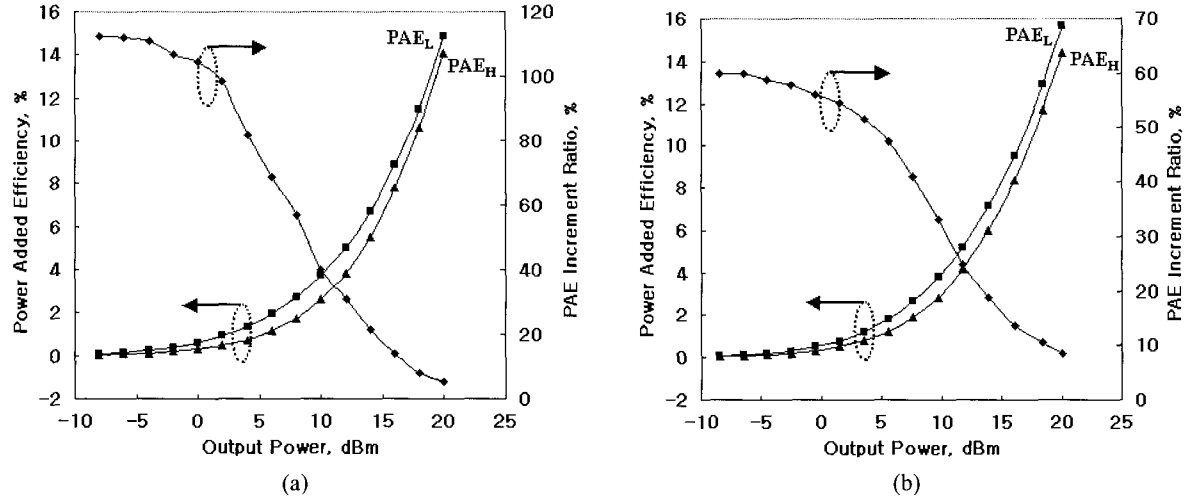



**Fig. 6** Measured PAE of the low and high power mode operation to the output power 20 dBm and PAE increment ratio of the two-stage smart power amplifier MMICs with the bias current control circuit (a) of current bypass structure and (b) of current injection structure.

the low power mode operation along with the input power, and that results in output power and power added efficiency values similar to that for the high power mode operation at the high output power region. The MMIC with current injection bias circuit operates with the total quiescent current of 50(80) mA for LPM(HPM) operation, and exhibits the output power of 26.83(29.75) dBm and PAE of 35.2(47.9) % for LPM (HPM) operation.

Figure 5 shows the measured ACLR using 3.84 Mcps HPSK modulated signal (DPCCH+1DPDCH). ACLR, at a 5(10) MHz offset frequency, of the MMIC with current bypass bias circuit exhibits –39(–59) dBc at the output power of 20dBm for the low power mode operation and –33(–52) dBc at the output power of 28dBm for the high power mode operation. ACLR, at a 5(10) MHz offset

frequency, of the MMIC with current injection bias circuit exhibits –44(–58) dBc at the output power of 20dBm for the low power mode operation and –33(–50) dBc at the output power of 28dBm for the high power mode operation. At the output power of 20 dBm, the MMIC with current bypass bias circuit shows 5 dB higher than the MMIC with current injection bias circuit. The 2.3 dB gain expansion of the MMIC with current bypass bias circuit at the output power of 20dBm in the Figure 4.(a) results in somewhat high value of ACLR.

Figure 6 shows the $PAE_L$ (PAE of Low Power Mode) and $PAE_H$ (PAE of High Power Mode) of the two-stage smart power amplifiers as a function of an output power up to 20 dBm. PAEIR(Power Added Efficiency Increment Ratio) is defined as follows;

$$PAEIR = \frac{PAE_L - PAE_H}{PAE_H} X\ 100 \quad [\%] \tag{1}$$

The PAEIR of the MMIC with current bypass bias circuit is 5.44 % at the output power of 20 dBm and increases to 112.5 % under the output power of –6 dBm. The PAEIR of the MMIC with current injection bias circuit is 8.6 % at the output power of 20 dBm and increases to 59.8 % under the output power of –6 dBm. This drastic improvement of each PAEIR is largely based on the reduced quiescent current of 44mA and 50mA, respectively. In the case of the MMIC with current bypass bias circuit, the quiescent current difference of 50 mA between high power mode and low power mode rather than 30 mA for the MMIC with current injection bias circuit makes higher PAEIR at the low output power region. But, at the output power of 20 dBm, the MMIC with current injection bias circuit shows higher PAE and PAEIR than the MMIC with current bypass bias circuit.

Figure 7 shows the gain, PAE, and ACLR of the two-stage smart power amplifier with the switching at the output power of 20 dBm. At the output power of 20dBm, phase difference of the $S_{21}$ between low and high power mode operation is lower than 2.2(0.36) degrees for the MMIC with current bypass bias circuit (the MMIC with current injection bias circuit) amplifier at the W-CDMA band.

Additionally, in order to evaluate the PAE effectiveness of the power amplifier with each bias control circuit, the work of Hanningtone et al. [8] is used

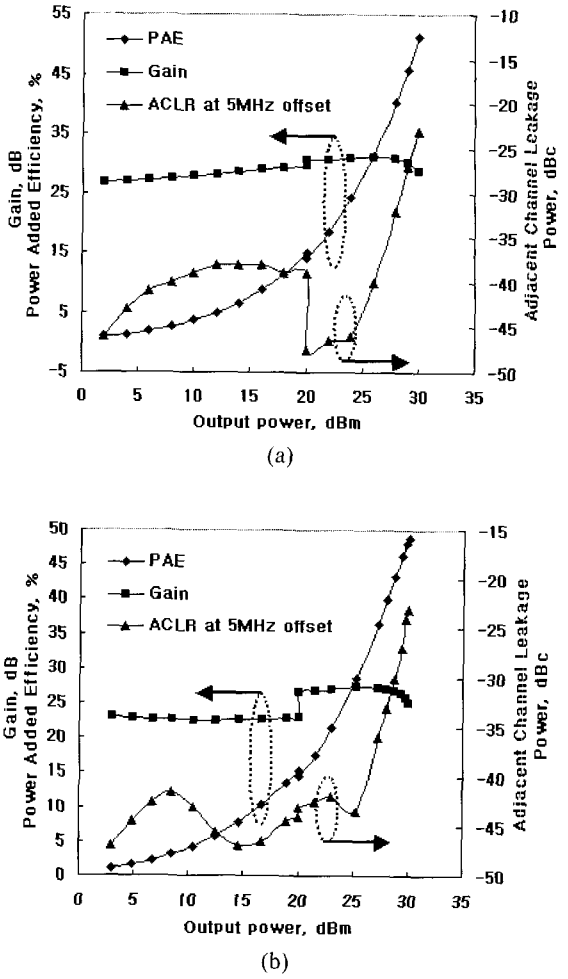



**Fig. 7** Measured gain, PAE, and ACLR with the switching at the output power of 20 dBm of the two-stage smart power amplifier MMICs with the bias current control circuits (a) of current bypass structure and (b) of current injection structure.

considering the power amplifier probability density function based on IS-95 CDMA urban environment [9]. From this work, the average RF output power from the power amplifier is defined as

$$\overline{P_{out}} = \int_{-\infty}^{+\infty} PDF(P_{out}) \cdot P_{out}\, dP_{out} \tag{2}$$

The average supplied DC input power is given by

$$\overline{P_{in}} = \int_{-\infty}^{+\infty} PDF(P_{out}) \cdot P_{in}(P_{out})\, dp_{out} \tag{3}$$

where the DC power is given by

$$P_{in} = I_{cc} \cdot V_{cc} \tag{4}$$

Then the average power usage efficiency is defined as

$$\eta_{usage} = \frac{\overline{P_{out}}}{\overline{P_{in}}} \tag{5}$$

This value is a measure of power amplifier efficiency for overall transmission power, and can be used for evaluation of the bias current control function on the efficiency. The average power usage efficiency defined in equation (5) is calculated as 5.94(5.8) % with switching at the output power of 20dBm. And, for only high power mode operation, the average power usage efficiency is 3.58(4.1) %. Consequently, the battery lifetime will be extended as much as 1.65(1.415) times by adopting the current bypass bias circuit (the current injection bias circuit). The measured performances of the two types W-CDMA MMIC smart power amplifier are summarized in Table 1.

**Table 1** Measured results of the W-CDMA MMIC smart power amplifiers.

| Amplifier Type | Operation | Vcon | Iq (mA) | Gain (dB) | PAE (%) | ACLR (dBc) |
|---|---|---|---|---|---|---|
| MMIC with current bypass bias circuit | LPM | High, 2.8~3.3V | 44 mA | 26 | Pout = 20 dBm | |
| | | | | | 14.8 | -39 |
| | HPM | Low, 0~0.5V | 94 mA | 29.6 | Pout = 28 dBm | |
| | | | | | 39.4 | -33 |
| MMIC with current injection bias circuits | LPM | Low, 0~0.5V | 50 mA | 22.9 | Pout = 20 dBm | |
| | | | | | 15.63 | -44 |
| | HPM | High, 2.8~3.3V | 80 mA | 26.6 | Pout = 28 dBm | |
| | | | | | 39.9 | -33 |

## V. CONCLUSION

The switching mode smart power amplifiers applying new bias current control circuits have been implemented for the high efficiency at the most probable output power regions as well as at the maximum output power. The low power mode operating the amplifier at the near Class B makes PAE increment ratio up to 112.5(59.8) % under -6 dBm output power for the MMIC with current bypass bias circuit (the MMIC with current injection bias circuit) amplifiers. With the switching to high power mode at the output power of 20 dBm, the switching mode MMIC power amplifiers with current bypass bias circuit (with current injection bias circuit) exhibits output power of 28(28) dBm, gain of 29.6(26.6) dB, PAE of 39.4(39.9)% with -33(-33)dBc ACLR at the a 5MHz frequency offset, extending the battery lifetime by 1.65(1.415) times.

## ACKNOWLEDGMENT

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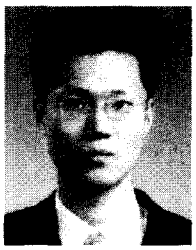

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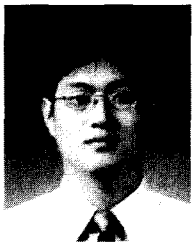

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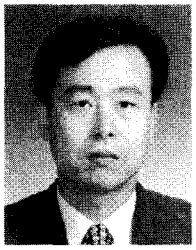

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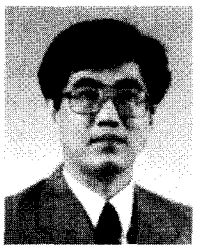

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