Design of Broad Band Amplifier Using Feedback Technique

Tae-Shin Kang and Jin-Koo Rhee

Abstract—**In this paper, an MMIC broadband amplifier for wireless communication systems has been developed by using an active feedback method. This active feedback operates at much higher frequencies than a method by a spiral inductor feedback and its size is independent of the inductance value. The MMIC broadband amplifier was designed using a 0.5 ㎛ MESFET library. The fabricated chip area was 1.4 mm × 1.4 mm. Measurement showed a gain of 18 dB with a gain flatness of ± 3 dB in a 1.5 GHz~3.5 GHz band. The maximum output power and the minimum noise figure were 14 dBm and 2.5 dB in the same band, respectively.**

Index Terms—**broad band amplifier, feedback, common-source FET, MMIC amplifier, active feedback**

I. INTRODUCTION

Recently, wireless communication market has shown explosive growth. Services in a 800 MHz~2.5 GHz band are especially important because PCS (Personal Communication Services), IMT-2000, and WLL (Wireless Local Loops) are all serviced in this band. A compact, low-priced and lightweight transceiver is one of the most important elements for in these services, and the MMIC (Monolithic Microwave Integrated Circuit) technology is the key to realize such a transceiver. A broadband amplifier is very attractive because it could replace narrowband amplifiers targeting each specific service frequency, for example, 1.8 GHz (PCS), 2 GHz (IMT-2000), and 2.4 GHz (WLL), and thus reduce development efforts and costs substantially [1]. In this work, an MMIC broadband amplifier for wireless communication systems was developed using an active feedback technique.

II. DESIGN AND FABRICATION OF THE AMPLIFIER

1. *Active Feedback Technique*

In an MMIC design, one of the major difficulties is to realize a high inductance with a small size spiral inductor. Due to the inter-segment fringing capacitance, however, realization of broadband spiral inductors is very difficult. And furthermore a serious problem is a shunt capacitance of the spiral inductor to ground [2-5]. In this work, the use of an active feedback technique instead of a spiral inductor feedback circuit improves the operating bandwidth while reducing the loss and the size of the amplifier [6-9]. Recently, a publication [8] has shown that its active feedback circuit is composed of a common-drain FET. In this paper an active feedback using a common-source FET is proposed. Specifically, the chip size is reduced by 75 % using an FET instead of a 6.5-turn spiral inductor with similar impedance. A basic configuration and a simplified equivalent circuit for the proposed common-source active feedback loop are illustrated in Figs. 1 and 2, respectively.

In order to calculate S_{21} gain and inductance, we used

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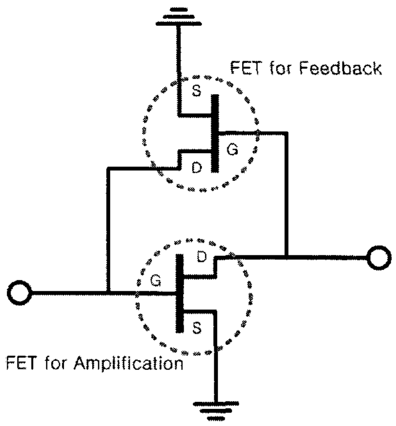

Fig 1 Proposed basic configuration of the Active Feedback with a common-source FET.

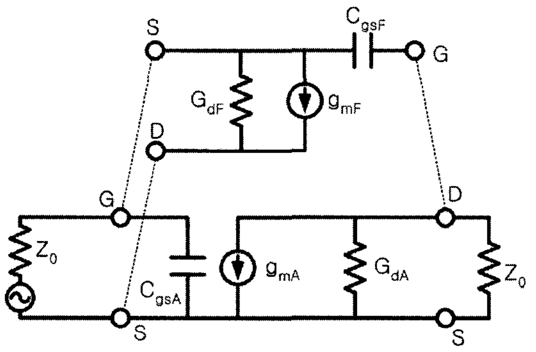

Fig 2 A simplified equivalent circuit of the Active Feedback loop.

FET's small signal parameters. The Y_A matrix of the FET for amplification is

$$[Y_A] = \begin{bmatrix} j\omega C_{gsA} & 0 \\ g_{mA} & G_{dA} \end{bmatrix} \tag{1}$$

The common-source FET in the feedback path is shown as Y_F

$$[Y_F] = \begin{bmatrix} j\omega C_{gsF} & 0 \\ g_{mF} & G_{dF} \end{bmatrix} \tag{2}$$

The total Y matrix of the equivalent circuit is

$$[Y] = \begin{bmatrix} j\omega C_{gsA} + j\omega C_{gsF} & 0 \\ g_{mA} + g_{mF} & G_{dA} + G_{dF} \end{bmatrix} \tag{3}$$

From the Y matrix of equation (3), the first stage S_{21} gain is obtained as following equation (4)

$$\begin{aligned} S_{21} &= \frac{-2Y_{21}Z_0}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)-(Y_{12}Z_0)(Y_{21}Z_0)} \\ &= \frac{-2Y_{21}Z_0}{(1+Y_{11}Z_0)(1+Y_{22}Z_0)} \\ &= \frac{-2(g_{mA}+g_{mF})Z_0}{\{1+(j\omega C_{gsA}+j\omega C_{gsF})Z_0\}\{1+(G_{dA}+G_{dF})Z_0\}} \end{aligned} \tag{4}$$

The above expressions show that the gain of the proposed active feedback stage can be changed by controlling of gate-source capacitance (C_{gsF}) and transconductance (g_{mF}) the feedback path FET. For example, if C_{gsF} and g_{mF} decrease and increase, respectively then S_{21} gain is increasing. However, the performance of this proposed method is seriously affected by increasing C_{gsF}. Because, C_{gsF} of the active feedback path FET is decided by inductance of the active feedback path and operation frequency of whole circuits. The inductance of active feedback path is calculated by equations (5), (6) and (7)

$$\begin{aligned} [Y] &= \left[j\omega C_{gsA} + g_{mA}\left(1+\frac{g_{mF}}{j\omega C_{gsF}}\right) \right] \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \\ &= \left[j\omega C_{gsA} + g_{mA} + \frac{g_{mA}\, g_{mF}}{j\omega C_{gsF}} \right] \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \end{aligned} \tag{5}$$

Equation (5) is rewritten as equation (6) by considering only the imaginary part,

$$[Y] = \left[j\omega C_{gsA} + \frac{1}{j\omega C_{gsF}} \right] \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \tag{6}$$

The maximum operation frequency is calculated by equation (7)

$$f_{\max} = \frac{1}{2\pi}\sqrt{\frac{g_{mA}\, g_{mF}}{C_{gsA}\, C_{gsF}}} = \sqrt{f_{TA} f_{TB}} \tag{7}$$

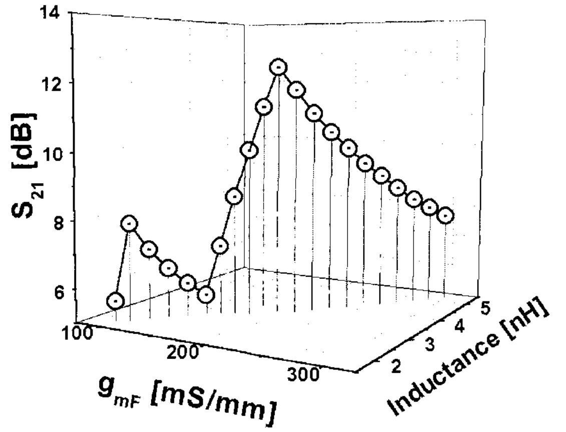

Fig 3 Calculated transconductance and inductance versus S_{21} gain of the active feedback stage.

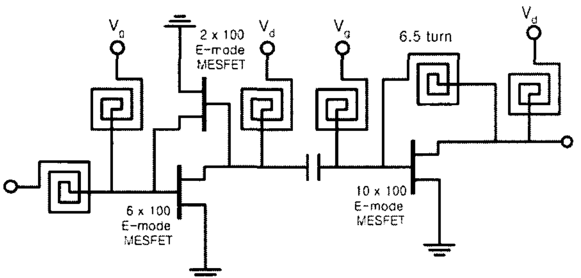

Fig 4 A schematic of the designed two-stage Feedback Amplifier.

The S_{21} gain and inductance of active feedback stage are plotted in Fig 3.

As a result, we selected the active feedback path FET with 200 ㎛ gate width with 200ms/mm transconductance to obtain maximum S_{21} gain and f_{max} by simulation.

2. *Topology of the Amplifier*

The amplifier was designed by using a 0.5 ㎛ MESFET library. The design of the two-stage MMIC amplifier included the input and the output matching networks to avoid the use of off-chip matching circuits. Enhancement-mode (E-mode) MESFETs were used in the first stage, the second stage, and the feedback circuit. For the best performance of our MMIC, we designed the second stage using conventional feedback method. To determine the gain, bandwidth and frequency of the second stage, we used resistor and spiral inductor in feedback path [10]. The gate widths for each stage were 6 × 100 ㎛, 10 × 100 ㎛, and 2 × 100 ㎛, respectively.

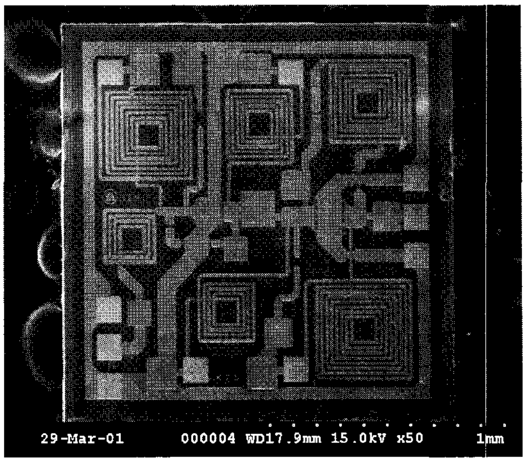

Fig 5 A photograph of the fabricated chip.

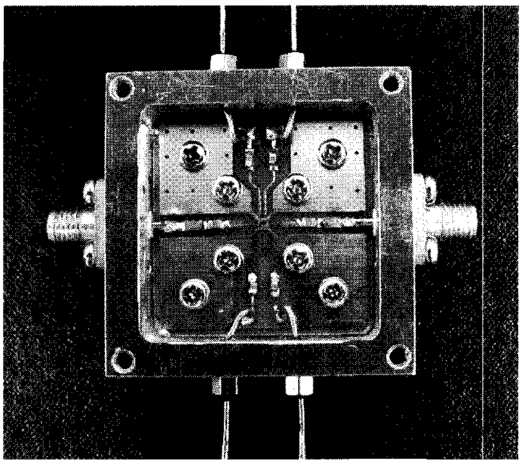

Fig 6 The MMIC amplifier module.

The bias conditions were I_{ds} = 50 % I_{dss}, V_{gs} = 0.6 V, and V_{ds} = 3 V, for optimum performance. Fig. 4 shows the schematic of the two-stage feedback amplifier. Simulation results showed a gain of 21 dB with a gain flatness of ± 1 dB. And the maximum output power was 17 dBm, and the noise figure was 2.5 dB in the 600 MHz to 3 GHz range.

3. *Fabrication*

To minimize coupling effects between signal lines, a minimum gap of 20 ㎛ was maintained. The use of a right-angle bend was avoided to reduce signal distortions. The widths of the signal and the ground lines were designed to be wider than estimated values by simulation in order to reduce parasitic inductances. The size of the fabricated chip is shown in Fig. 5 is 1.4 mm × 1.4 mm.

A gold-plated test PCB was specially designed and fabricated to match our measurement setup. The MMIC chip was mounted and then bonded to the test PCB. The module size is 40 mm × 40 mm × 18 mm. Fig. 6 shows the MMIC amplifier module.

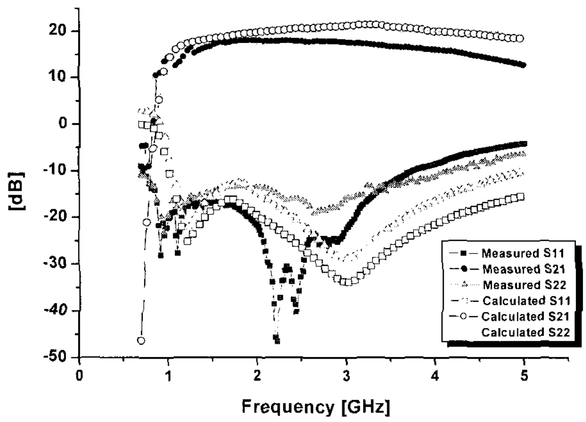

Fig 7 Measured S parameters of the amplifier.

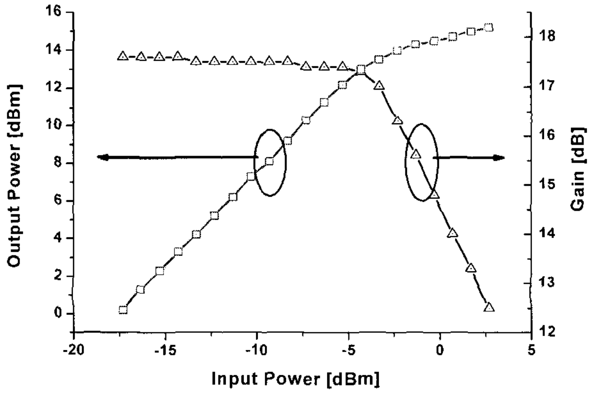

Fig 8 Power performance of the amplifier.

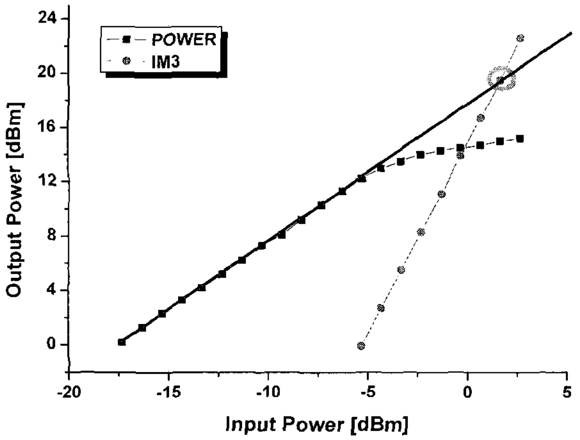

Fig 9 Results of the two-tone test.

III. MEASUREMENT OF THE AMPLIFIER MODULE

The module has the measured maximum gain of 18 dB at 2.5 GHz. Both the input and the output return losses are better than -10 dB in the 1.0 GHz~3.5 GHz range. The chip operates at the 3 V supply voltage, and the current consumption is 50 mA. Fig. 7 shows the S-parameter characteristics of the two-stage feedback amplifier. The measurement results show some discrepancy from the simulation. This is partially attributed to the fact that the effects of the bonding wires between the MMIC chip and the external bias circuits are not sufficiently considered in the simulation. The proposed MMIC chip used the common-source active feedback, and our proposed MMIC design showed high gain compared with a amplifier of the common-drain active feedback by Kenjiro et al. [8].

The power amplification performance of the amplifier is shown in Fig. 8. The 1 dB compression point ($P1_{dB}$) is 14 dBm of output power with an associated gain of 17 dB. The result of the two-tone test is shown in Fig. 9. The OIP_3 is about 20 dBm.

IV. CONCLUSION

In this paper, an MMIC broadband amplifier for wireless communication systems has been developed by using an active feedback method, which resulted in reduced chip size and broadband RF characteristics. The fabricated amplifier shows the gain of 18 dB with the gain flatness of ± 3 dB in 1.5 GHz~3.5 GHz band. $P1_{dB}$ is 14 dBm of output power with the associated gain of 17dB. This MMIC broadband amplifier could be an effective solution to various mobile communication systems.

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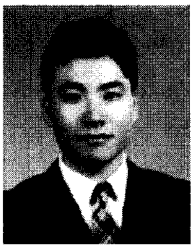

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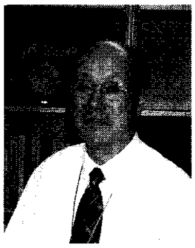

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