K-Time 슬롯당 한번의 스케줄을 갖는 독창적인 스위치 아키텍쳐에 관한 연구

손승일*

A Study on The Novel Switch Architecture with One Schedule at K-Time Slots

Seung-il Sonh*

이 논문은 2003년도 한신대학교 학술 연구비 지원에 의하여 연구되었음

요 약

본 논문에서는 k-타임 슬롯 당 한번의 스케줄을 갖는 새로운 스위치 아키텍쳐를 제안한다. 여기서 k는 각 스케줄에 대해 할당된 시간 슬롯을 의미한다. 기존의 스위치 스케줄러는 각각의 스케줄에 대해 하나의 타임 슬롯을 사용하지만, 제안된 스위치 시스템은 각 스케줄에 대해 다중 타임 슬롯을 사용한다. 기존의 스위치 시스템과 제안된 스위치 시스템은 동일한 쓰루풋을 갖지만 제안한 스위치 시스템은 각 스케줄당 다중 셀 타임 슬롯을 점유한다. 따라서 기존의 스위치 시스템과 비교하여 간단한 회로의 스케줄러로 구현되어 질 수 있다. 스위치 시스템에 대해 제안된 스케줄링 알고리즘은 고속의 데이터 링크율을 갖는 스위치 시스템에 적용될 수 있을 것으로 사료된다.

ABSTRACT

In this paper, we propose a new switch architecture with one schedule at k-time slots, which k means the allocated time slots for each schedule. A conventional switch system uses a single time slot per each schedule but the proposed switch system uses multiple time slots per each schedule. Both the conventional switch and the proposed switch have same throughput but our switch system occupies multiple cell time slots per each schedule and hence can be implemented in scheduler of simple circuitry compared to the conventional switch. The proposed scheduling method for switch system will be applicable in switch system with high-speed data link rate.

키워드

Scheduler, ATM Switch, Multiple-cell time slots, Throughput, VOQ(Virtual Output Queueing)

Ⅰ. Introduction

Input-queued switches are not proper for a high-performance switch due to poor performance. If FIFO queues are used to queue cells at each time, only the first cell in each queue is admitted to be forwarded. As a result, FIFO input queues suffer from head of line(HOL) blocking; if the cell at the front of the queue is blocked, other cells behind it in the queue cannot be forwarded to other

*한신대학교 정보통신학과

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unused outputs. It is well known that under certain conditions the maximum achievable throughput is limited to just 58.6%[1].

Hence, There have been many researches to enhance the performance of an input-queued switches by avoiding HOL blocking effect[2]-[4]. HOL blocking is entirely eliminated by using a separate FIFO queue for each output at each port, which is called Virtual Output Queueing(VOQ) scheme[5].

A cell scheduler must resolve output contention swiftly, provide high throughput, and meet QoS requirements. The scheduler algorithm like PIM, 2DRR, iSLIP, and MUCS has been developed-[3][4][6][7]. In order to process incoming cells in giga/tera bps of link rate, a cell time slot has been reduced and scheduling speed has to be increased. Especially, as port size of ATM switch becomes larger, the burden of a scheduler is higher. To cope with high link rate, a new investigation for existing cell scheduling methodology is needed. Due to breakthrough of memory process technology, memory access speed is improved and memory cost gradually goes on declining. We are mainly interested in ATM backbone switch with high traffic load. In this letter, we present ATM switch architecture with a novel multiple cell scheduling method which gets rid of the burden of a scheduler and can virtually achieve 100% throughput.

II. Proposed ATM Switch Architecture

Existing ATM switches just transmit one cell to corresponding destination port from an input port during one cell time slot. But as the transmission link rate abruptly increases in terabits per second, one cell time slot is very short. As a result, the scheduling time is substantially important. The complexity of scheduler is proportional to port size of ATM switch and the large port size of that may not satisfy the timing requirement of cell/packet scheduler.

To resolve the mentioned problem above, we propose a new switch system with multiple cells scheduling scheme. The proposed switch system is based on an advanced input-queued switch in which a separate queue called VOQ is maintained at each input port for each output port. The proposed switch system is shown in figure 1. Figure 1 is an example for transmission of 2 cells per schedule. Our switch system transmits 2 or more cells per schedule compare to one cell per schedule of the previous switch system.

We will explain the operation of the proposed switch below. Based on Figure 2, after we first explain the operation of a conventional switch system, that of our switch scheme will be described. Switch system is composed of 3-stage pipeline as shown in figure 2. The cell arrival stage is the stage of cell arrival in the buffer. The cell schedule stage performs the scheduling for the request cell.

The cell departure stage is the stage of cell departure in the buffer. VOQ memory of this paper uses dual-port memory.

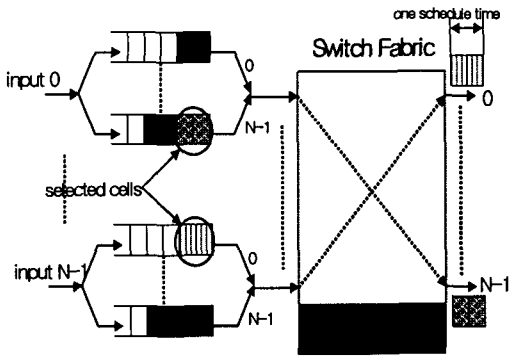

Fig. 1 Advanced input-buffered switch with multiple cells forwarding per schedule

Hence, the cell arrival and departure can simultaneously occur in the VOQ memory. As shown in (a) of figure 2, the conventional switch system can process the only one cell during unit schedule time. The schedule time is limited within one time slot and giga/tera bits per second of the link rate make difficult in finishing the schedule at one time slot for a large switch system. To solve the problem above, the switch system proposed in the paper allocates 2 or more cells time for schedule.

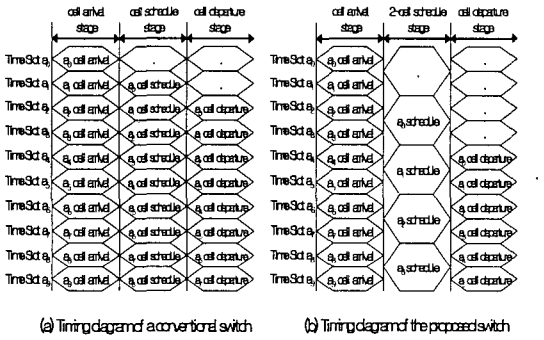

Fig. 2 Timing diagram for a conventional switch and the proposed one

As a result of the allocation of k time slots for schedule, the burden of the scheduler is reduced in 1/k of factor. During k time slots for schedule, k cell arrival and k cell departure are possible. The time diagram of the proposed switch scheme is shown in (b) of figure 2 and the schedule factor is k=2. The first cell departure arises at the third time slot a_2 in (a) of figure 2 and at the fifth time slot a_4 in (b) of figure 2.

III. Performance Analysis

The performance of the proposed switch is simulated using the most common scheduling algorithm, iSLIP, in a central arbiter for random uniform and burst traffic models. A two-state Markov chain model is used for the burst cell arrival process[8]. We use a switch with N=8. We suppose that Each VOQ can store up to 2,048 ATM cells for each destination port. Especially, it is focused on the performance evaluation for the offered load from 90% to 100%.

Figure 3 compares mean IQ(input Queue) length of the conventional switch and the proposed switch with iSLIP scheduling algorithm under random uniform traffic. Although the mean IQ length of the conventional switch spends small queue area below 97%, the difference of maximum queue length between the conventional switch and the proposed switch is trivial in offered load above 98%.

Figure 4 shows the delay characteristics of the conventional switch and the proposed switch under the equal condition with that of figure 3. As the offered load increases, the difference for mean waiting time between the conventional switch and the proposed switch decreases. But the performance for mean waiting time in the conventional switch is superior to that of the proposed switch.

The simulation for uniform bursty traffic which burst length is 8-cell is also performed with the same switch structure mentioned in figure 3 and figure 4.

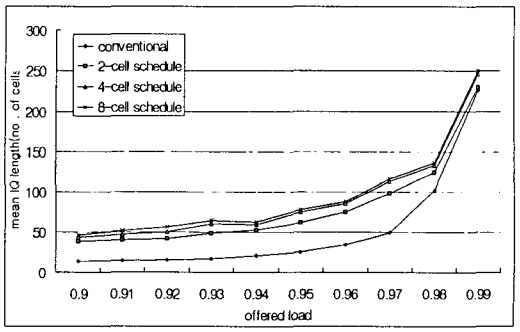

Fig. 3 Comparison of conventional switch with the proposed switch for mean IQ length in random uniform traffic

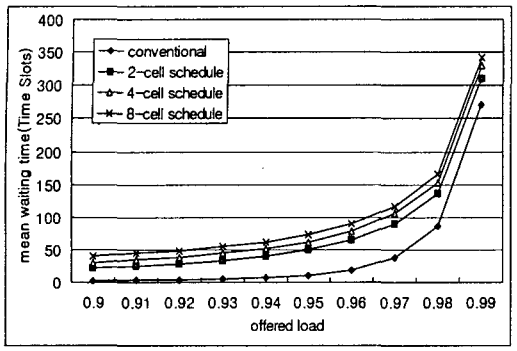

Fig. 4 Comparison of conventional switch with the proposed switch for mean waiting time in random uniform traffic

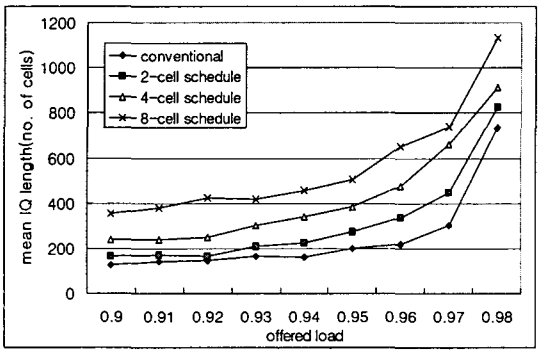

Fig. 5 Comparison of conventional switch with the proposed switch for mean IQ length in uniform bursty traffic

Figure 5 compares mean IQ length of the conventional switch and the proposed switch with iSLIP scheduling algorithm under uniform bursty traffic. Simulation result shows that queue size for 2-cell schedule method in 98% offered load has 12% overhead compared to that of the conventional switch. Queue size for 4-cell schedule method is 23% larger queue size than that of the conventional switch.

Figure 6 shows the delay characteristics of the conventional switch and the proposed switch under uniform bursty traffic. The simulation result shows that the switch adopting 2-cell schedule method experiences 14% longer mean waiting time than the conventional switch. As the granularity of cell schedule increases, mean waiting time for the proposed switch is linearly grown corresponding to increment of cell schedule granularity.

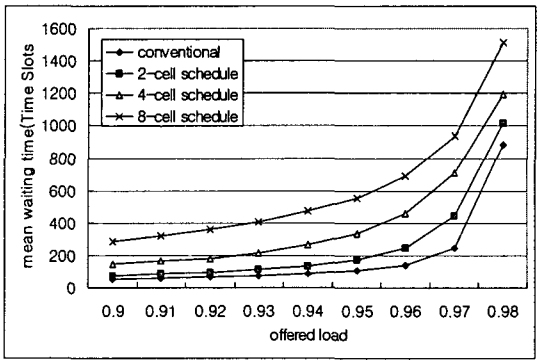

Fig. 6 Comparison of conventional switch with the proposed switch for mean waiting time in uniform bursty traffic

Until now, we analyzed the mean waiting time and mean IQ length for the conventional switch and the proposed switch system. As a result of analysis, the conventional switch has a benefit for the mean IQ length and waiting time compared to the proposed switch. But as mentioned earlier part of this paper, our interests are mainly the switch throughput and the simplicity of scheduler.

From now on, we will discuss the throughput and scheduler simplicity. The throughput for switch system is shown in figure 7. As shown in figure 7, both the conventional switch and the proposed switch have almost the same throughput. Therefore, the multiple-cell scheduling method proposed in this paper does not reduce the throughput compared to the conventional switch.

The complexity of Scheduler design for ATM switch is increased as the port size of ATM switch is extended.

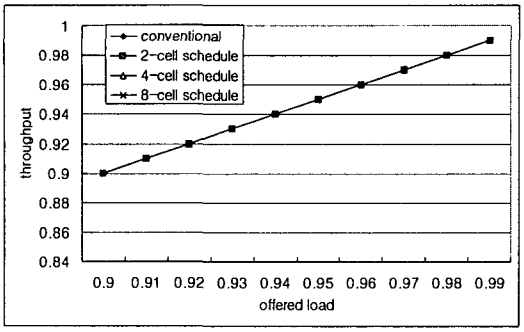

Fig. 7 Comparison of throughputs between the conventional switch and the proposed switch

But if the granularity of cell schedule increases, the burden of the scheduler is reduced and the implementation of simple scheduler is possible. That is to say, the conventional switch must complete scheduling within one cell time slot. The proposed switch using multiple-cell schedule can use multiple-cell time slots for scheduling. Let us suppose that a time slot of the conventional switch takes 12 clock cycles. The schedule for the conventional switch must be finished within 12 clock cycles. If we use 2-cell schedule method proposed in this paper, the schedule must be completed within 24 clock cycles which occupy two time slots. Hence the multiple-cell scheduler can implemented in small area circuit although total scheduling cycles are increased.

IV. Conclusions

In this paper, we focused on the novel multiple-cell schedule method for ATM switch system to cope with extremely high-speed link rate. The proposed switch system obtained the same throughput compared to the conventional switch and considerately reduced the burden of scheduler. If the granularity of cell schedule proposed in this paper increases in K, the design area of the scheduler may approximately reduce in 1/K. The multiple-cell scheduling method proposed in this paper is applicable as the scheduler of the high-speed ATM switch.

감사의 글

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저자 소개

손승일(Seung-il Sonh)

1989년 2월 연세대학교 전자공학과 (공학사)
1991년 8월 연세대학교 전자공학과 (공학석사)
1998년 2월 연세대학교 전자공학과 (공학박사)
1998년 3월~2002년 8월 호남대학교 컴퓨터공학과 교수
2002년 8월~현재 한신대학교 정보통신학과 교수
※ 관심분야 : ATM 통신, ASIC 설계