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A Novel Frequency-to-Digital Converter Using Pulse-Shrinking

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Abstract - In this paper, a new frequency-to-digital converter without an analog element is proposed. The proposed circuit consists of pulse-shrinking elements, latches and D flip-flops, and the operation is based on frequency comparison by the pulse-shrinking element. In the proposed circuit, the resolution of digital output can be easily improved by increasing the number of the pulse-shrinking elements. The FDC performance is improved in viewpoints of operating speed and chip area. In designed FDC, error of frequency-to-digital conversion is less than 0.1%.

Keywords: frequency-to-digital converter, pulse-shrinking element

1. Introduction

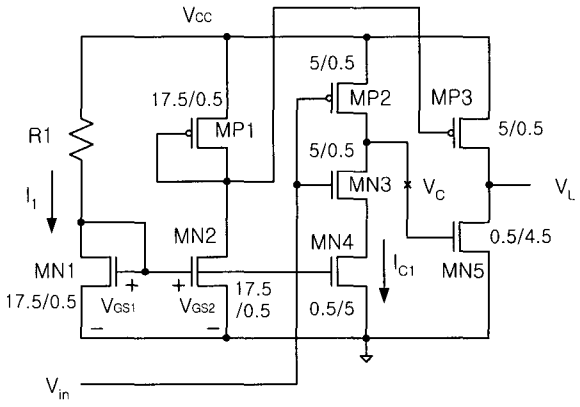
A frequency-to-digital converter (FDC) is an interesting electronics block widely used in systems involving automatic control of frequency such as communications, frequency synthesis, and instrumentation systems [1-2]. In general, the FDC contains analog and digital circuit blocks and the architecture is built on the capacitors charge redistribution principle [1]. To convert frequency into digital value, the frequency signal is converted to an analog voltage signal by way of a capacitor. The digital value is obtained by analog-to-digital conversion. In this paper, an FDC without ADC is proposed, allowing for a simplified structure and enhanced performance in the cases of operating speed and chip area.

2. Circuit implementation and simulation results

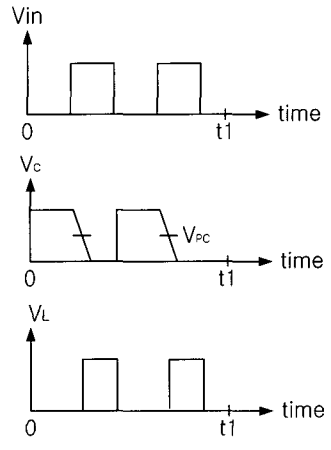
The frequency-to-digital converter consists of pulse-shrinking elements, latches, and D flip-flops. The pulse-shrinking element circuit is shown in Fig. 1(a). In Fig. 1(a) MN1 and MN2 are the constant current source and the drain currents of MN1 and MN2 are identical because V_{GS1} and V_{GS2} are the same and MN1 and MN2 have equivalent channel width and length. I_{C1} flows through MN4 is given by

$$\frac{I_{C1}}{I_1} = \frac{(W/L)_{MN4}}{(W/L)_{MN1}} \quad (1)$$

where W is the channel width and L is the channel length. Fig. 1(b) shows Vin, V_C and V_L signals. When the input pulse, Vin, is low MP2 is on and MN3 is off. Thereby V_C is high and the output signal, V_L, is low as shown in Fig. 1(b) and Fig. 1(c). When Vin is high MN3 is on and V_C voltage decreases linearly because MN4 is a constant current source. When V_C voltage drops below the critical voltage, V_{PC}, the output signal, V_L, is switched to a higher state. The critical voltage, V_{PC}, is 0.98 volts, which is obtained in HSPICE simulation.



(a)



(b)

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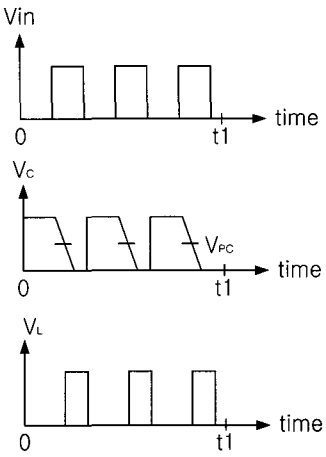


(c)

Fig. 1 The proposed circuit and waveforms (a) pulse-shrinking element circuitry (b) input and output waveforms (low frequency) (c) input and output waveforms (high frequency)

The width of Vin shrinks by the pulse-shrinking element and the degree of pulse shrinking is controlled by the constant current source I_{C1}. The output pulse width will vary with input frequency as shown in Fig. 1(b) and Fig. 1(c).

The pulse-shrinking element can be operated as the frequency comparator and a reference frequency for frequency comparison in the pulse-shrinking element depends on the I_{C1} current. When the input frequency is faster than a reference frequency the output of the pulse-shrinking element, V_L, is low. Conversely, when the input frequency is not faster than a reference frequency the output of the pulse-shrinking element is high and the width of V_L pulse shrinks compared to the input pulse width.

The relation between I_{C1} and the reference frequency f_1 is expressed as follows:

$$f_1 = I_{C1} / C\Delta V \tag{2}$$

with

$$\Delta V = V_{CC} - V_{PC} \tag{3}$$

where V_{CC} is the supply voltage, V_{PC} is the critical voltage and C is the sum of gate and drain capacitances. I_{C1} is about 10nA, which is decided to obtain the 25kHz reference frequency.

The circuit operation has been verified by HSPICE simulation and the supply voltage is 3.3 volts. The circuit has been designed and simulated using 0.35 ㎛ CMOS technology. The FDC circuit is shown in Fig. 2(a) and Fig. 2(b). The MN4, MN7_1, MN7_2, MN10_1, MN10_2 and MN10_3 transistors have the same width and length in Fig. 2(a). The reference frequencies f_2 and f_3 are expressed as follows:

$$f_2 = I_{C2} / C\Delta V = 2I_{C1} / C\Delta V = 50KHz \tag{4}$$

$$f_3 = I_{C3} / C\Delta V = 3I_{C1} / C\Delta V = 75KHz \tag{5}$$

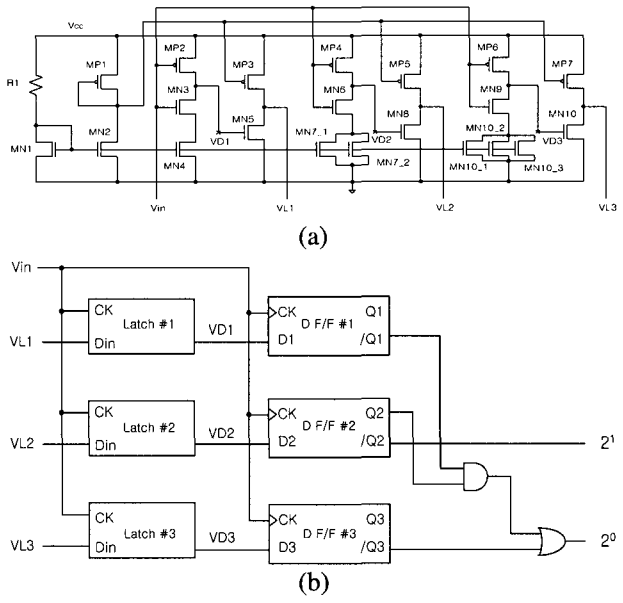
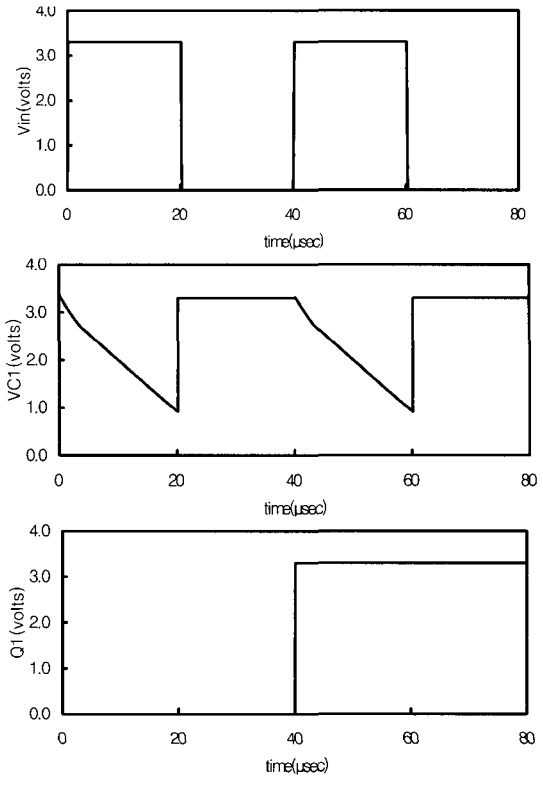
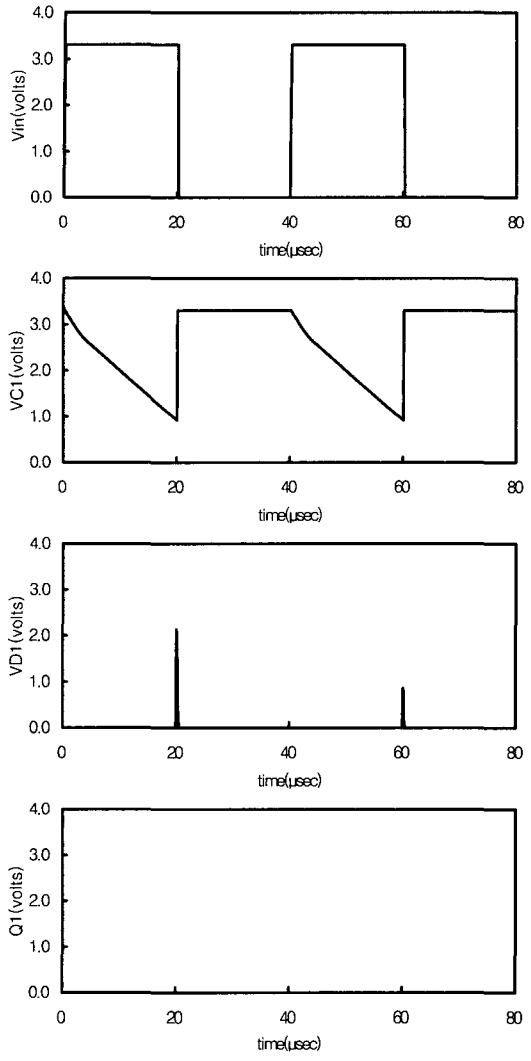


Fig. 2 The FDC circuit (a) pulse-shrinking elements circuit (b) the latch and D flip-flop circuit

Fig. 3 shows Vin, VC1, VD1 and Q1 signals. In Fig. 3(a) and (b) the input frequencies are 25kHz and 24.975kHz, respectively. The latch stores the high value when the VC1 voltage drops 0.98 volts and the D flip-flop stores the latch output signal, VD1, at the positive edge of the input pulse.



(a)



(b)

Fig. 3 The output signals of pulse-shrinking element Input frequency: (a) 24.975kHz (b) 25kHz

In Fig. 3(a) the Q1 signal is high when input frequency is 24.975KHz. Q1 signal is low when input frequency is 25KHz. The reference frequency of the VL1 signal is 25KHz for frequency comparison and the error is less than 0.1%. From equations (3) and (4), VL2 and VL3 signals are low when the input frequency is faster than 50kHz and 75kHz, respectively.

Table 1 shows the digital output with the input frequency. The digital outputs, 2^1 and 2^0, will be expressed by

$$\begin{aligned} 2^1 &= \overline{Q2} \\ 2^0 &= \overline{Q3} + Q2 \cdot \overline{Q1} \end{aligned} \tag{6}$$

where Q1, Q2 and Q3 are the outputs of D flip-flop #1, D flip-flop #2 and D flip-flop #3, respectively.

Table 1 The D flip-flop outputs and the digital outputs with input frequency

Input frequency f [kHz]	Q3	Q2	Q1	Digital output	
				2^1	2^0
$75 \le f < 100$	0	0	0	1	1
$50 \le f < 75$	1	0	0	1	0
$25 \le f < 50$	1	1	0	0	1
$0.0 \le f < 25$	1	1	1	0	0

The performance of the designed FDC is shown in Fig. 4 when the input frequency is 40kHz. Fig. 4(a) shows the Vin signal and Fig. 4(b) shows VD2 and VD3. Fig. 4(c) shows the final digital outputs. The proposed design scheme reveals that the digital output can be obtained without delay time.

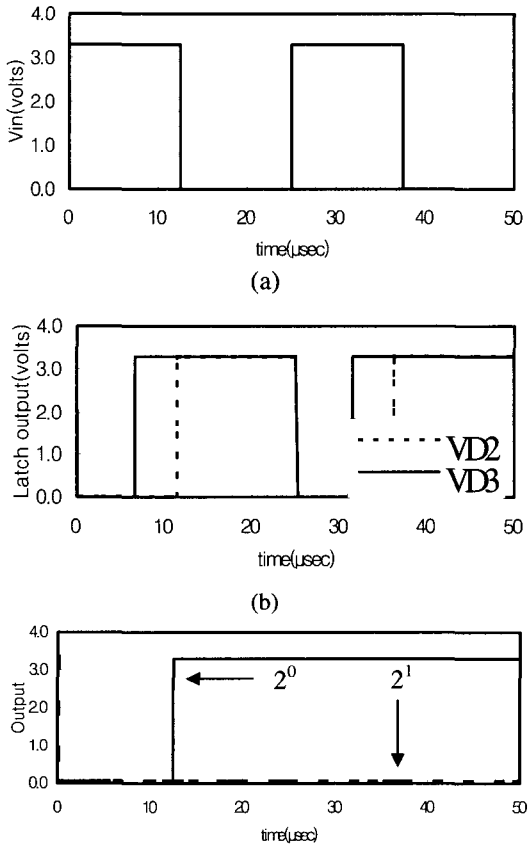


Fig. 4 The output signals in the designed FDC circuit (a) input signal (b) VD2 and VD3 signals (c) digital output

3. Conclusion

The frequency-to-digital converter for frequency detection is presented. The designed circuit is implemented only

in MOS transistors and the FDC performance is improved from the viewpoint of operating speed. As well, the resolution of the digital output can be improved by increasing the number of pulse-shrinking elements, latches and D flip-flops. The designed circuit shows good output characteristics to use in frequency-to-digital signal processing.

References

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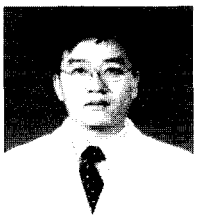

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