A Design of 5.8 GHz Oscillator using the Novel Defected Ground Structure

Myoung-Sub Joung · Jun-Seok Park · Jae-Bong Lim · Hong-Goo Cho

Abstract

This paper presents a 5.8-GHz oscillator that uses a novel defected ground structure(DGS), which is etched on the metallic ground plane. As the suggested defected ground structure is the structure for mounting an active device, it is the roles of a feedback loop inducing a negative resistance as well as a frequency-selective circuit. Applying the feedback loop between the drain and the gate of a FET device produces precise phase conversion in the feedback loop. The equivalent circuit parameters of the DGS are extracted by using a three-dimensional EM simulation and simple circuit analysis method. In order to demonstrate a new DGS oscillator, we designed the oscillator at 5.8-GHz. The experimental results show 4.17 dBm output power with over 22 % dc-to-RF power efficiency and − 85.8 dBc/Hz phase noise at 100 kHz offset from the fundamental carrier at 5.81 GHz.

Key words : Oscillator, Defected Ground Structure(DGS).

Ⅰ. Introduction

An oscillator represents the basic microwave energy source for all microwave systems, such as radars, communications, navigation, or electronic warfare. They can be termed as dc-to-RF converters or infinite-gain amplifiers. A typical microwave oscillator essentially consists of an active device(a diode or a transistor) and a passive frequency-determining resonant element, such as a microstrip, SAW, cavity resonator, or dielectric resonator for fixed tuned oscillator and a varactor or a YIG sphere for tunable oscillator. With the rapid advance of microwave technology, there has been an increasing need for better oscillator performance. The emphasis has been on low phase-noise, small size, low cost, high efficiency, high temperature stability and reliability for all oscillators[12]. Most transistor oscillators can be viewed as feedback circuits since they require a series or parallel feedback to induce a negative resistance. The feedback topology chosen for an oscillator circuit has a great influence on the frequency range of the negative resistance. Dielectric resonator(DR) is a commonly used device to create a feedback loop in microwave oscillators. By realizing one or multiple immittances, DR works as a high-quality frequency selective circuit as well as providing series or parallel feedback paths to the microwave oscillator. This approach, however, dose not permit full monolithic microwave integrated circuits (MMIC) oscillator as its volume. Therefore, in terms of cost, reliability, and integration, a DGS oscillator using microstrip structure is preferred. As a DGS is the structure etched on the metallic ground plane, it provides rejection band in some frequency range due to increasing the effective inductance of a transmission line. The structure has been reported in the recent publications in various applications such as filters, power dividers, and amplifiers due to its high-Q frequency characteristics, compactness, the precise extraction of equivalent circuit models and simple applications to any microstrip circuits[3]~[9].

In this paper, we report on the design, implementation, and performance of a 5.8 GHz self-resonant oscillator using a novel DGS, which is capable of mounting an active device. The main advantages of a DGS oscillator are that reduce size because a modified DGS induces a feedback loop as well as a frequency-selective circuit. Also this circuit was fabricated with hybrid technique, but can be fully compatible with the MMIC due to its entirely planar structure.

Ⅱ. A Novel DGS for Mounting an Active Device

Generally, the oscillator for microwave systems is

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composed of an active element and a resonant for the selective frequency.[3] In this paper, a new etched DGS which structure is planar type suitable microwave integrated circuit(MIC) has been used resonant-circuit as well as feedback circuit. Furthermore the presented DGS circuit in this paper is useful to mounting a transistor such as a BJT or FET. Fig. 1 show the proposed DGS configuration etched on the ground plane under the conventional microstrip line. In order to bias DC to a transistor, it is necessary to implement the DC isolated circuit in a practically realizable oscillator with DGS. The DGS structure presented Fig. 1 involves the consideration for the DC isolation, which correspond to gap d appeared in this figure, of bias circuit.

However, EM-simulation for finding the equivalent circuit parameters to implement an oscillator was performed with the DGS circuit shown in Fig. 2(a), which has the dimension of d=0. It should be noted that since the gap d shown in Fig. 1 introduces an open circuit to the ground conductor at low frequencies including DC, the patterns isolated by gap d on DGS must be electrically coupled to achieve identical performance with the case of Fig. 2(a) at high frequency region. The electrical coupling at the operating frequency region of an oscillator could be simply achieved by coupling capacitors shown in Fig. 2(b).

A ceramic substrate of 0.671 mm thickness, which has a dielectric constant of 9.2, was used for design and fabrication. The dimensions of rectangle were chosen to be a=7.5 mm and b=2.72 mm. The etched

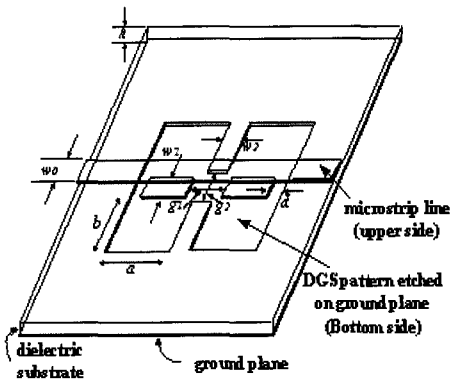


Fig. 1. The proposed defected ground structure useful to mounting the active device. The dimensions of rectangle were chosen to be a=7.5 mm and b= 2.72 mm. The etched gaps, g_1, g_2, and d are 1.0 mm, 2.0 mm, and 0.5 mm, respectively. The microstrip width, w_1, is 0.66 mm corresponding to a conventional 50 Ω line.

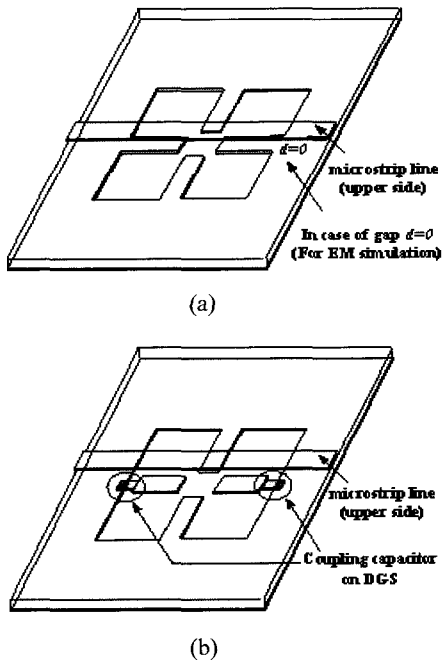


Fig. 2. The DGS models for (a) EM-simulation to find the equivalent circuit parameters and (b) practically implementation of a DGS oscillator. w_2 was chosen to be 0.5 mm.

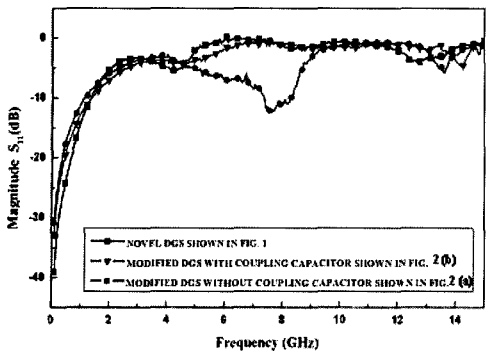
gaps, g_1, g_2, and d are 1 mm, 2 mm, and 0.5 mm, respectively. The micro-strip width, w_1, is 0.66 mm corresponding to a conventional 50 Ω line. Three kinds of DGS circuits are fabricated without coupling gap (d=0), with coupling gap(d=0.5 mm), and with coupling capacitor(2pF) on the coupling gap.

To confirm the validity of the proposed DGS, three kinds of DGS circuits are fabricated without coupling gap(d=0), with coupling gap(d=0.5 mm), and with coupling capacitor(2pF) on the coupling gap. Fig. 3 shows the comparisons of measurements on the fabricated DGS circuits. Measurements on the DGS circuit without coupling capacitors show the cutoff-frequency shift from that of DGS without the gaps for DC isolation as shown in Fig. 3. However, measured S-parameters on the DGS circuits without coupling gap and with coupling capacitors in gaps of DGS are well matched all frequencies until about 10 GHz.

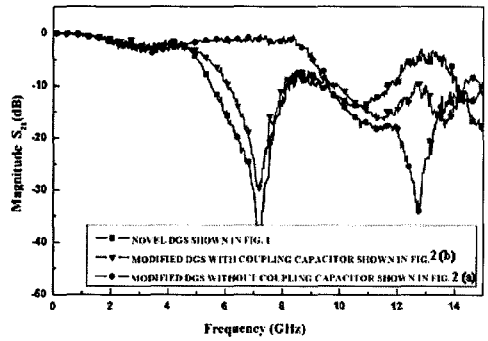
Ⅲ. Design of a DGS Oscillator at 5.8 GHz

3-1 The Design of a DGS for 5.8 GHz Oscillator

Fig. 4 shows The PCB layout of the proposed DGS oscillator. It was fabricated on a 0.671 mm-thick TMM-

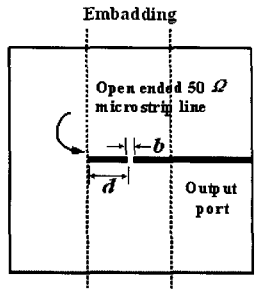


(a)

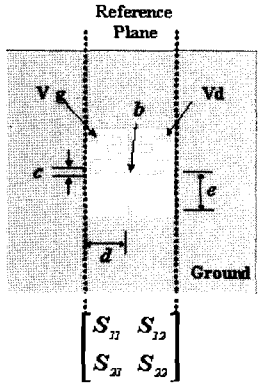


(b)

Fig. 3. Comparisons of measurements on three kinds of the fabricated DGS circuits.



(a) Top layout



(b) Bottom layout

Fig. 4. The PCB layout of the proposed DGS oscillator.

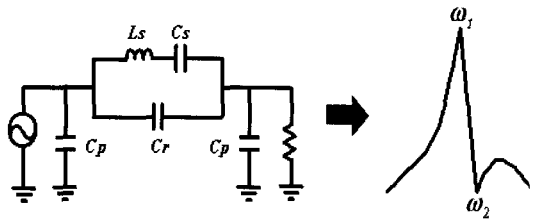


Fig. 5. Equivalent circuit of layout shown in Fig. 4 and the expected response.

10 substrate with a relative dielectric constant of 9.2. As Fig. 4(a) shows the top pattern of the proposed DGS, the left side was provided open ended 50 Ω microstrip line and middle gap is roles of tuning a oscillation frequency with implement lumped capacitor if there is needed. Fig. 4(b) shows the ground pattern, it is composed of a DGS lattice and bias lines. In this work, the length and gap of the DGS was set a=4.24 mm, b=0.4 mm, c=0.67 mm, d=4.18 mm, and e=4.1 mm respectively.

The simplified equivalent circuit of the PCB layout shown in Fig. 4 is depicted in Fig. 5. The equivalent circuit of the proposed DGS can be obtained by s-parameter values which can be extracted by performing an EM-simulation with the DGS unit as the reference plane. The equivalent circuit of the proposed DGS can be expressed by π-type circuit model. Thus, the ABCD-parameters can be found from the 2-port parameter transportation using the extracted S-parameters. Next step, admittance values can be found the ABCD. Finally, the susceptance of the admittance is calculated by (1), (2), and (3). The inductance L_s and the Capacitance C_s determine the resonant frequency (ω_1) of the DGS and the inductance L_s and parallel capacitance C_r is a ant-resonant part (ω_2) respectively. All these values are determined from the structure of the DGS, such as line length, line width, and gap of the DGS. Parameter L_s, C_s and C_r is dependant on lengths b, d, and e.

The whole size of this DGS, which can be used to integrate all elements, such as active device, resonant circuit, feedback circuit and lumped elements in the area, is within 9×9 mm. Therefore the oscillator using a DGS is much smaller than a conventional microstrip-type oscillator. Fig. 6 is showed the comparison mea-

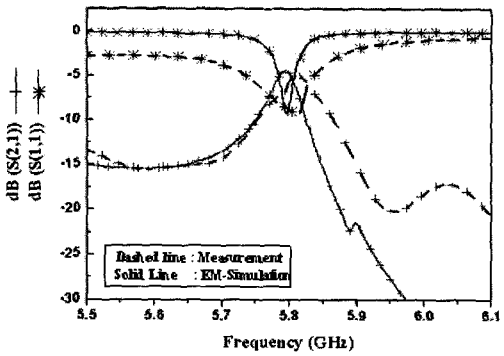


Fig. 6. Measured(solid line) and simulated(dashed line) response of the DGS layout shown in Fig. 4.

sured result with EM-simulation one. It shows 70 MHz of 3-dB bandwidth at 5.82 GHz center frequency. The measured loaded quality factor of the DGS is 87.

There are some disagreements between simulated and measured one, such resonant frequency, return and insertion loss, and quality factor. It is believed that this is because the whole size of the proposed DGS is so small that there are some errors in the fabrication process. However, these problems would be overcome if the proposed DGS is designed and fabricated in an MMIC technology. Also, further optimization for this structure would lead to the improvement of the quality factor.

3-2 The Design of 5.8 GHz Oscillator

Fig. 7 shows the photograph of a practically implemented oscillator, which was designed at 5.8 GHz and incorporated with the proposed DGS. The total dimensions of the assembled circuit are 12 mm×10 mm and 0.671 mm thickness. We adopted a parallel feedback topology which is composed of a active device, DGS pattern, and some lumped elements. Presented oscillator uses a DGS for section as a feedback loop for inducing the negative resistance and a passive frequency-selective circuit, simultaneously. External lumped elements or device mounted on DGS are figured as parallel-connected elements or device with the equivalent circuit of unit DGS section. Thus, DGS circuit having an active device provides a parallel feedback path to the mounted device on DGS. The equivalent circuit and the modeling method for a DGS circuit are detailed in [5].

Since the effect of an external lumped element on DGS circuit can be explained by parallel connection

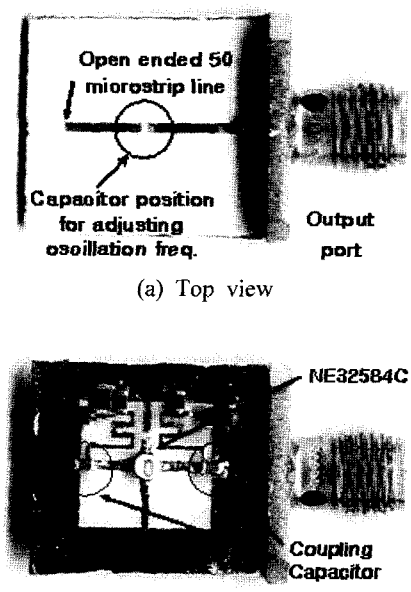


Fig. 7. The photograph of the DGS oscillator.

with the equivalent circuit of a DGS circuit, the prototype circuit for simulation of the DGS oscillator presented in this paper is shown in Fig. 8[6]. The DGS oscillator was designed with a NE32584C GaAs hetero-junction FET in common source configuration for achieving the Gate-to-Drain feedback. Finally designed DGS circuit for implementing the oscillator involves the DC chokes, for the purpose that DC bias can be applied to the device with minimal influence on the oscillator's RF performance, by using quarter wavelength transformer as shown in Fig. 8.

The oscillation conditions are analyzed by the con-

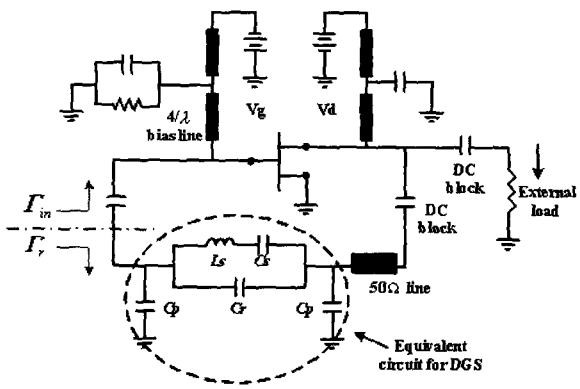


Fig. 8. The corresponding prototype circuit having the equivalent circuit of DGS.

dition of loop feedback and that of negative resistance. Firstly, to have a loop gain of the oscillation signal, the feedback transfer function should be 0 degree. Secondary, to eliminate the parasitic resistance of the resonator, negative resistance is produced with the active device. Negative resistor represents when the reflection coefficient toward the active device is greater than 1. So the condition where the magnitude of S11 is greater than 1 can be described as the initial requirement for oscillation.

Fig. 9 shows the oscillation analysis for the equivalent DGS circuit in commercial computer-aided design.

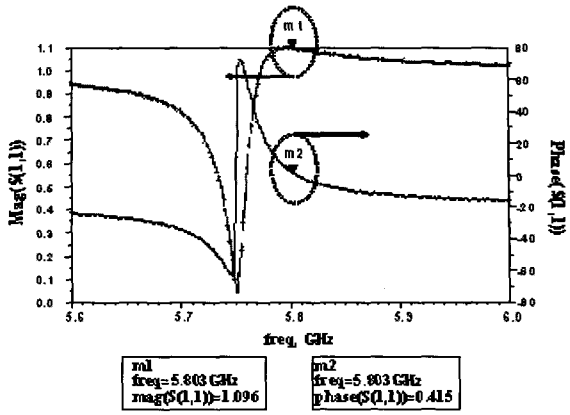
As shown in Fig. 9, we meet the oscillation condition, such as negative resistance and loop-phase for achieving loop-gain, at 5.8 GHz.

Ⅳ. Measurements and Results

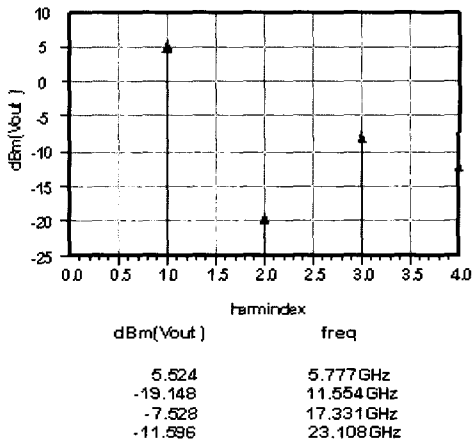
Fig. 10 shows the dependence of the output power and DC-RF efficiency on the transistor drain bias V_d measured with fixed $V_g = -0.87$ V. For a drain voltage of 2 V, the output power was increased to 5 dBm while DC-RF efficiency was decreased at the over 1.7 V drain voltage. Inspecting the equation of the DC-RF efficiency in (7), [10] the highest DC-RF efficiency is 22 % with output power 4.17 dBm, the bias condition of V_d = 1.7 V and $V_g = -0.87$ V, and I_d =8 mA at the oscillation frequency of 5.809 GHz.

Fig. 11 depicts the variations of output power, and oscillation frequency at drain voltage, V_d=1.7 V, as a function of gate voltage, V_g. According to increasing V_g from −1.6 V to −0.6 V, oscillation output power of 3.8 ± 0.5 dBm was observed at around 5.8 GHz and oscillation frequency varied from 5.68 GHz to 5.86 GHz. Thus, we knew the fact that the propose oscillator is stable, as the result that the oscillator pushing figure was about 180 MHz/V about various bias condition. Fig. 12 shows the measured dependence of the phase noise on the drain bias voltage with $V_g = -0.87$ V at a 100 kHz offset. The minimum phase noise value, −86 dBc/Hz, was achieved at a drain bias V_d = 1.7 V. This result suggests that the phase-noise characteristic is minimized if the oscillating transistor is biased so as to yield the optimum transconductance characteristic (via the drain voltage)[11].

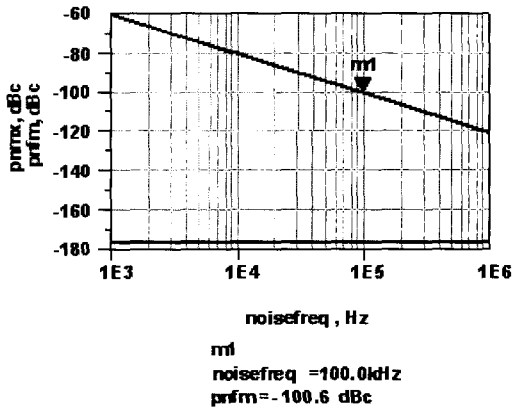
Fig. 13(a) shows the measured output spectrum of the fabricated DGS oscillator. The oscillation frequency, ω_{or} of the DGS oscillator is 5.81 GHz. The output power of the oscillator is 4.17 dBm with applied voltage



(a)



(b)



(c)

Fig. 9. The oscillating condition of 5.8 GHz DGS oscillator using computer-aided design.

of V_d=1.7 V and $V_g = -0.87$ V. As the result that this circuit dissipates 8 mW from a 1.7 V supply, efficiency of the presented oscillator is near 22 %. Fig. 13(b) shows harmonics for fundamental frequency. The

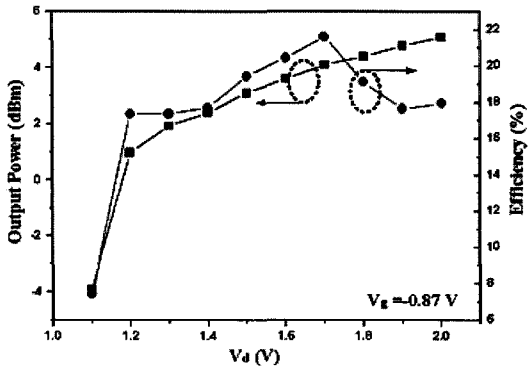


Fig. 10. The variations of output power, and DC-RF efficiency as a function of drain voltage (V_g= – 0.87 V).

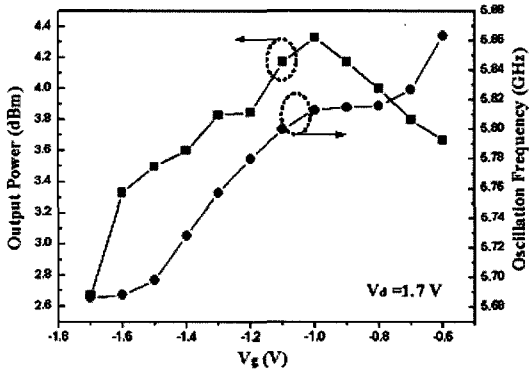


Fig. 11. The variations of output power, and oscillation frequency as a function of gate voltage(V_d= 1.7 V).

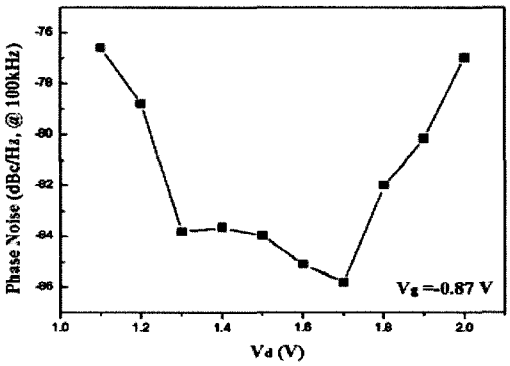
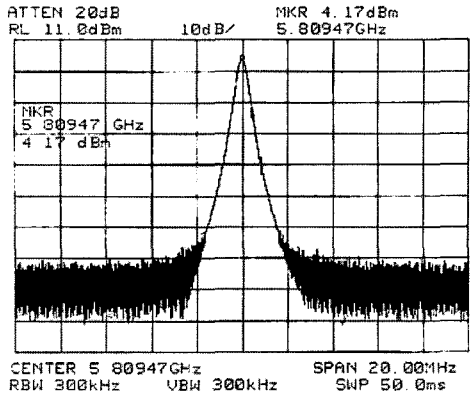


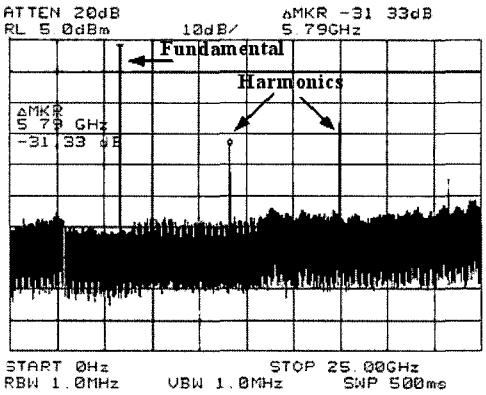
Fig. 12. The variation of phase noise as a function of drain voltage(V_g= – 0.87 V)

second harmonic of the oscillator is 31.33 dB down from fundamental oscillation frequency.

A phase noise at 100 kHz offset form the carrier (f_o=5.81 GHz) is measured to be – 85.83 dBc/Hz as shown in Fig. 14. Employing the stabilized techniques



(a) Fundamental output power spectrum



(b) The output power spectrum including harmonics

Fig. 13. Measured output spectrums.

Table. 1. The characteristics for the implemented 5.8 GHz DGS oscillator.

Characteristics	Measurement
Oscillation frequency	5.81 GHz
Output power level	4.17 dBm
1st harmonic suppression	31.33 dBc
Phase Noise @ offset freq. 100 kHz	– 85.83 dBc/Hz
Power supply	V_d=1.7 V, V_g= – 0.87 V
Current consumption	8 mA
DC to RF conversion efficiency	22 %
Dimension fabricated size	12×10 mm

such as injection-locked oscillator can improve the performance of the presented oscillator. Furthermore,

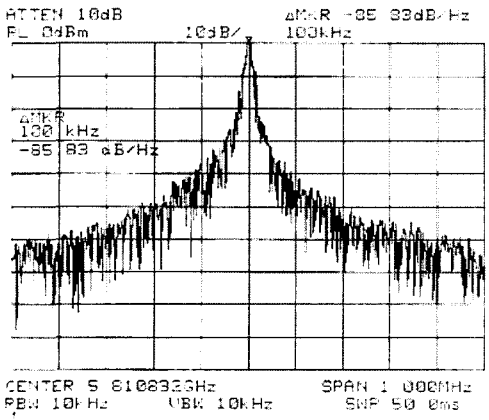


Fig. 14. Measured phase noise performance for the fabricated oscillator.

the phase noise performance can be improved by increasing the quality factor of DGS at resonant frequency. Table 1 shows the characteristics for the implemented 5.8 GHz DGS oscillator.

V. Conclusion

A new configuration for the self-resonant parallel feedback oscillator is presented using the DGS circuit, which is useful to mounting an active device such as BJT or FET. The output power of the oscillator is about 4.17 dBm with the DC-to-RF conversion efficiency of 22 % at a 5.81 GHz oscillation frequency. And it exhibits phase noise performance of −85.8 dBc/Hz at 100 kHz offset. We expect the basic configuration of this paper can be further exploited to various oscillator techniques such as injection-locking oscillator or self-oscillating mixer techniques for both MIC and MMIC applications. These will be the topic for our future works.

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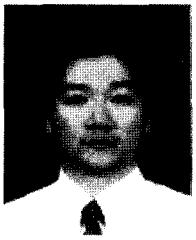

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He received the B.S., M.S. and Ph.D degrees in electronics engineering in 1972, 1979 and 1987, respectively, from Seoul National University, Korea. In September 1980, he joined the Kookmin University, Korea, and is currently a Professor in the School of Electrical Engineering. He was also a Visiting Professor at Colorado University and Syracuse University in 1988 and 2001, respectively. His areas of research include electromagnetic numerical analysis, antenna analysis and design. His current research involves RF and microwave hybrid module design using low-temperature co-fired ceramic techniques and RF integrated circuit(RFIC) design.