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A Japanese National Project for Superconductor Network Devices

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Abstract

A five-year project for Nb-based single flux quantum (SFQ) circuits supported by Japan's Ministry of Economy Trade and Industry (METI) in Japan was started in September 2002. Since April 2003, the New Energy and Industrial Technology Development Organization (NEDO) has supported this Superconductor Network Device Project. The aim of the project is to improve the integration level of Nb-based SFQ circuits to several ten thousand Josephson junctions, in comparison with their starting integration level of only a few thousand junctions. Actual targets are a 20 GHz dual processor module for the servers and a 0.96 Tbps switch module for the routers. Starting in April 2003, the Nb project was merged with SFQ circuit research using a high-T_c superconductor (HTS). The HTS research targets are a wide-band AD converter for mobile-phone base stations and a sampling oscilloscope for wide-band waveform measurements.

Keywords : national project, single-flux-quantum, Nb integrated circuit, router, processor, switch circuit, Josephson junction

I. Introduction

Two crises concerning network devices have been predicted in the developing information technology (IT) society. One is an electric power crisis due to the rapid increase in power consumption by network devices, especially by servers. The Fuji Research Institute anticipated that by 2010 the increasing power consumption will demand more than thirty one- million kW class atomic power plants supplying electric power. The other crisis is congestion due to rapid increases in communication traffic. They predicted that by 2010, 20 Tbps (10^{12} bit per second) throughput routers will be necessary, although the maximum throughput of semiconductor routers will be restricted to around 1 Tbps.

A possible solution to this problem is the use of superconducting single flux quantum (SFQ) circuits [1], which are unique devices that can realize large-scale integrated circuit (LSI) operation having higher clock-speed than semiconductor circuits [2]. This is due to their ultra-high (picosecond) speed and low-power (micro W per gate at 100 GHz) nature. These features enable the devices to be integrated with high density without considering heat generation.

The high-speed nature of these circuits makes it possible to reduce their complexity, thus reducing the number of their elements and their power consumption. An example of this is the USA's SFQ PFLOPS computer project, which planned to develop a 1 PFLOPS computer made up of 256 GFLOPS processors comprising 4000 SFQ chips, the power consumption of which would be 300 W for the chips and 100 kW for a cryo-cooler. This would stand in sharp contrast to a CMOS 1 PFLOPS computer made up of 10 GFLOPS processors comprising 100,000 chips and having power consumption of 15 MW.

SFQ circuits are particularly advantageous for network router switches, because SFQ switches can

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directly process 40 Gbps input data by means of a 40 GHz clock. This contrasts with semiconductor switches, even the fastest ones, which process 10 Gbps data by divided 64 parallel using 156 MHz-clock switches. This remarkable reduction in circuit size results in a breakthrough on packaging and power consumption limits, and increases data throughput.

For the purpose of developing SFQ servers and routers, Japan's Ministry of Economy, Trade and Industry (METI) has launched a national "Superconductors Network Device Project" as an advanced program IT infrastructure. The project period is from September 2002 to March 2007. This article describes the project's organization and research targets.

II. Organization

Fig. 1 shows the organization that was set up to execute this project. Since April 2003, the project has been supported by the New Energy and Industrial Technology Development Organization (NEDO). The project leader is Prof. H. Hayakawa of Nagoya University, one of the world leaders in the field of superconductor digital technology. NEDO has entrusted the project to the International Superconductivity Technology Center (ISTEC). The Superconductivity Research Laboratory (SRL) which is under the ISTEC umbrella has hired floor and facilities from NEC Fundamental Research Laboratories for the project and organized the Low Temperature Superconducting Device Laboratory (SRL Tsukuba). NEC had constructed an Nb process line, measurement facilities and design tools.

In the area of SFQ design, ISTEC collaborates closely with Nagoya University (Prof. A. Fujimaki) and Yokohama National University (Prof. N. Yoshikawa). They also collaborate with Communication Research Laboratory, Hokkaido University (Prof. M. Takai), and Nagoya University (Prof. N. Takagi) on circuit design, micro architecture and device architecture, respectively.

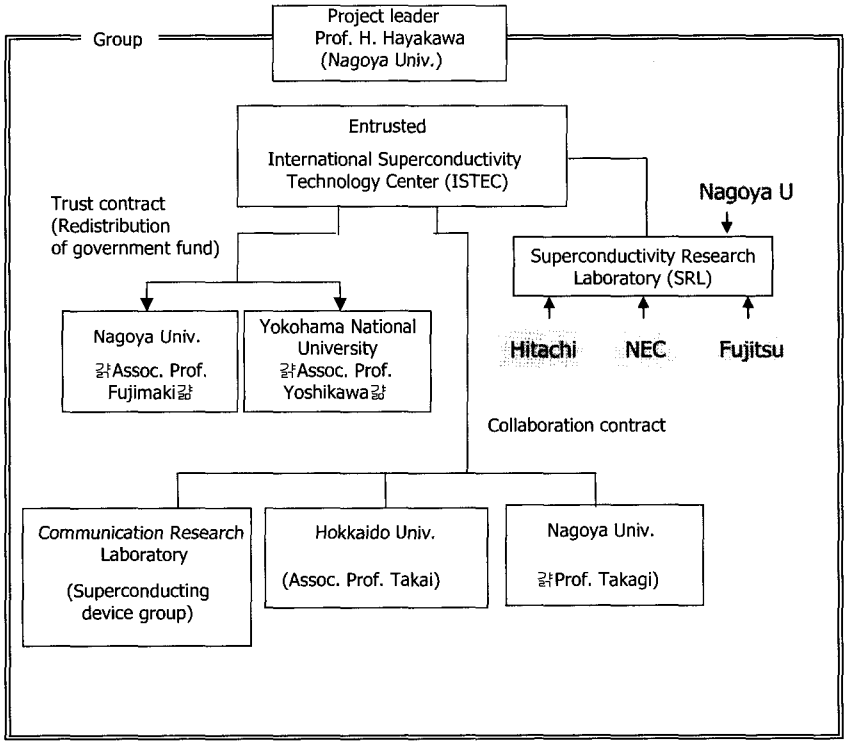

Fig. 1. Organization of the Superconductor Network Device Project

Researchers from NEC, Hitachi, Fujitsu and Nagoya University have joined SRL Tsukuba to develop both fabrication processes and circuit designs. SRL Tsukuba fabricates Nb-based SFQ chips for design researchers. About 20 researchers and 15 students are engaged in the project.

III. Research targets

One of the aims of the project is to raise the Nb-based SFQ circuit integration level to several ten thousand Josephson junctions, in contrast to their starting level of a few thousand junctions. Process and design technology will be developed as a means to fabricate such SFQ circuits. The ultimate targets are a 0.96 Tbps switch module for the routers and a 20 GHz dual processor module for the servers.

Fabrication process

Our current Nb fabrication process is called "NEC standard process [3]". Fig. 2(a) shows a schematic cross section of a device by the process. There are three Nb layers and the minimum Josephson junction size is 4 μm^2. Fig. 2(b) is an image of our advanced process. All layers, except contact holes, will be planarized to increase the number of Nb layers. The original plan called for the number of Nb layers to be four by 2004 and five by 2006, and for the minimum junction size to be reduced to 2.0 μm^2 by 2004 and 1.0 μm^2 by 2006. The one-fourth junction size corresponds to twice the operation clock frequency, namely 80 GHz.

Circuit design

We are developing a top-down cell base design methodology [4] for designing SFQ LSIs using 100,000 Josephson junctions. The plan is to develop an automatic placing and routing tool that converts circuit diagrams to layout schematics, and a logic synthesis tool that generates circuit diagrams from logic operation descriptions, in addition to an advanced cell library and high-speed circuit design methodology.

Switch module for SFQ routers

A 32×32 switch module for SFQ routers will be demonstrated at the end of this project. Fig. 3 shows

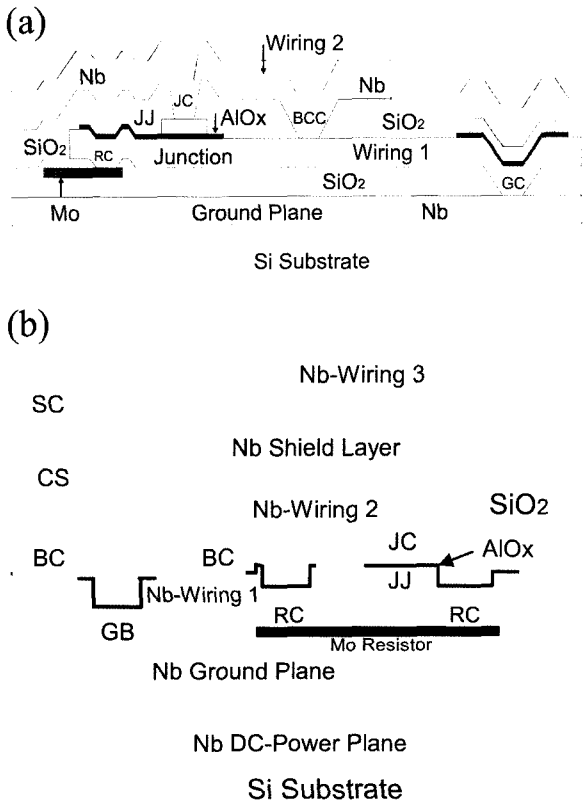

Fig. 2. Schematic cross sections of (a) the NEC standard process and (b) an advanced process image.

an image of the switch module. Several SFQ switch chips, for example four 16×16 chips, will be arranged on a multi-chip-module (MCM). Each switch chip will operates at a 30 GHz clock. This will achieve a total module throughput of 0.96 Tbps, which is 12 times larger than that of the fastest semiconductor switch module.

Processor module for SFQ servers

One of the project targets is the dual processor module shown in Fig. 4. The module consists of two identical processors, a switch network and a clock generator. Each processor includes an ALU, a resistor, a controller and a cache memory, and semiconductor main memories are placed at room temperature. The dual processor module will be operated at a 20 GHz clock. High-speed data transmission between SFQ processors will be verified using the module.

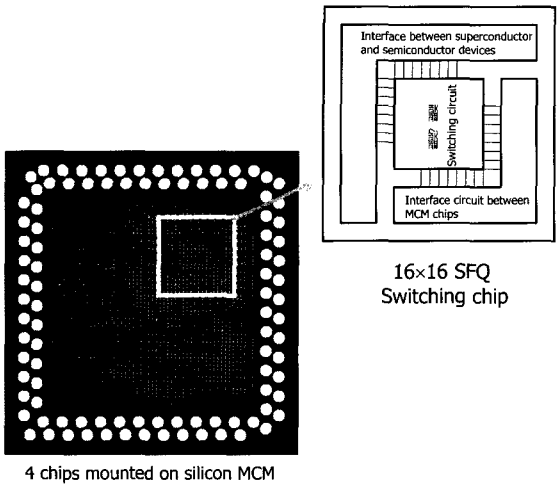

Fig. 3. Schematic image of the 32×32 switch module. Approximate size is 10 cm × 10 cm.

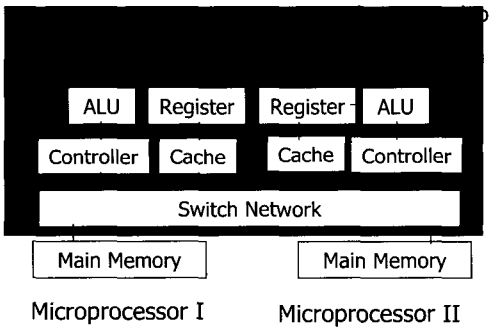

Fig. 4. Schematic image of the dual processor module for servers.

IV. High-T_c superconductor project

In April 2003, SFQ circuit research using high-T_c superconductor (HTS) was merged with the Nb project. The HTS research targets are a wide-band AD converter for mobile-phone base stations [5] and a sampling oscilloscope for wide-band waveform measurements [6]. Process, design and assembly technologies for implementing these devices are being developed at SRL Tokyo.

V. Summary

A national project for superconducting network devices in Japan started in September 2002. The final project targets are an SFQ router and server. SRL hired a floor and facilities from NEC and is executing the Nb-based project there. About 20 researchers and 15 students are engaged in this project. SFQ LSIs comprising several ten thousand Josephson junctions will be operated at 40 GHz by 2005. Demonstrations of a 0.96 Tbps switch module and a 20 GHz dual processor module are planned at the end of the project. The development of HTS SFQ circuits for a sampling oscilloscope and an AD converter were merged with the Nb-based project in April 2003.

Acknowledgments

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