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A Simple Control Strategy for Balancing the DC-link Voltage of Neutral-Point-Clamped Inverter at Low Modulation Index

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ABSTRACT

This paper proposes a simple control strategy based on the discontinuous PWM (DPWM) to balance the DC-link voltage of three-level neutral-point-clamped (NPC) inverter at low modulation index. It introduces new DPWM methods in multi-level inverter and one of them is used for balancing the DC-link voltage. The current flowing in the neutral point of the DC-link causes the fluctuation of the DC-link voltage of the NPC inverter. The proposed DPWM method changes the path and duration time of the neutral point current, which makes the overall fluctuation of the DC-link voltage zero during a sampling time of the reference voltage vector. Therefore, by using the proposed strategy, the voltage of the DC-link can be balanced fairly well and the voltage ripple of the DC-link is also reduced significantly. Moreover, comparing with conventional methods which have to perform the complicated calculation, the proposed strategy is very simple. The validity of the proposed DPWM method is verified by the experiment.

Keywords: Neutral-Point-Clamped (NPC) inverter, DC-link voltage balancing, the neutral point current, discontinuous PWM (DPWM)

1. Introduction

Nowadays, multi-level inverters are being widely used in high voltage/high power application and multi-level inverter technology has been receiving great interest. The multi-level inverter has many advantages over the conventional two-level inverters as follows. The multi-level inverter reduces not only the voltage stress on switches by connecting the switches in series, but also EMI problems by decreasing the dv/dt stress. Furthermore, when comparing with the same switching frequency, the multi-level inverter can achieve lower harmonic distortion due to more level of the output waveform in comparison to the conventional two-level inverter.

Many multi-level inverter topologies have been proposed and classified into three categories: diode-clamped-inverter, cascaded inverter and flying capacitor inverter[1-3]. Among the multi-level inverters, the most popular topology is the diode-clamped-inverter, which is called as a neutral-point-clamped (NPC) inverter in three-level[1]. The structural feature of the diode-clamped-inverter is that all DC-link voltage can be charged with only one common voltage source although clamping diodes need to obtain the phase voltage of N-level. Especially, in the field of the high power speed application like traction and steel mill system, the NPC inverter has been widely used.

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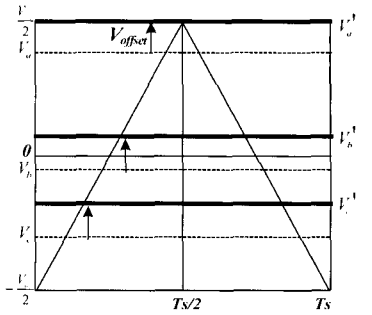
However, in NPC inverters, the DC-link voltage is divided by capacitors and each capacitor is composed of series connection construction. Therefore, if voltage unbalancing occurs between each capacitor, the line-to-line output voltage waveform has many harmonic components and the power devices in the NPC inverter can not guarantee safe operation. Therefore, for the safety and the good performance of the NPC inverter, the DC-link voltage balancing should be kept. Many methods have been presented to solve the DC-link voltage balancing problem[4-7]. However, many of them contain complicated calculation to select the switching sequence and to control the duration time of switching, or need to add the balancing circuit.

In this paper, a simple control strategy based on discontinuous PWM method is proposed and new DPWM methods in multi-level inverters are presented. The proposed method uses one of the DPWM methods in three-level inverter for balancing the DC-link voltage. By using this strategy, the DC-link voltage can be effectively balanced without the complicated calculation or the additional balancing circuit. The current flowing in the neutral point of the DC-link causes the fluctuation of the DC-link voltage in the NPC inverter. Therefore, the proposed DPWM changes the path and duration time of the neutral point current, which makes the overall fluctuation of the DC-link voltage zero during a sampling time of the reference voltage vector. Consequently, the DC-link voltage balancing is realized by the proposed method. The effectiveness of the proposed DPWM is verified through a number of experiments.

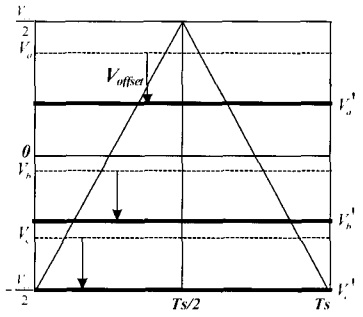
2. Discontinuous PWM Method

2.1 The conventional DPWM method in two-level inverter

As a technique to control the inverter, PWM (Pulse Width Modulation) method is stabilized and is the standard these days Many PWM methods have been researched and presented such as sinusoidal PWM (SPWM)[8], space-vector PWM (SVPWM)[9], third harmonic injection PWM (THIPWM)[10][11], carrier-redistribution PWM (CRPWM)[12][13] and discontinuous PWM (DPWM)[14][15].



(a)



(b)

Fig. 1. DPWM method in two-level inverter.

Among them, various discontinuous PWM methods have been developed in order to minimize the switching loss in two-level PWM inverter[15][16]. Fig. 1 shows the DPWM method in two-level inverter. The DPWM means that each output voltage of the inverter legs (V_a, V_b, V_c) is clamped to the positive rail (Fig. 1(a)) or negative rail (Fig. 1(b)) of the DC-link for total one third of the fundamental period. This is the reason why they are called a "discontinuous PWM". To clamp each output voltage, it is necessary to add the specified voltage to each output voltage. The specified voltage is named the offset voltage (V_{offset}). The V_{offset} can be selected in condition as follows.

$$-\frac{V_{dc}}{2}-V_{\min}\le V_{offset}\le\frac{V_{dc}}{2}-V_{\max} \tag{1}$$

where $V_{max}=\max(V_a, V_b, V_c)$

$V_{mid}=\mathrm{mid}(V_a, V_b, V_c)$

$V_{min}=\min(V_a, V_b, V_c)$

In Fig. 1, $V_a^{'}$, $V_b^{'}$ and $V_c^{'}$ are new output voltages and are given by (2) written as follows

Table 1. V_{offset} according to clamping rail in two-level inverter.

Clamping rail	V_{offset}	Condition
Positive rail	$V_{offset} = \frac{V_{dc}}{2} - V_{\max}$	No condition
Negative rail	$V_{offset} = -\frac{V_{dc}}{2} - V_{\min}$	No condition

$$\begin{aligned} V_a^{'} &= V_a + V_{offect} \\ V_b^{'} &= V_b + V_{offect} \\ V_c^{'} &= V_c + V_{offect} \end{aligned} \tag{2}$$

Table 1 shows the V_{offset} according to the clamping rail in two-level inverter.

The DPWM methods are of a special interest because they reduce the average switching frequency by 33% and cause less switching loss. Hence, the DPWM methods are applied to the two-level inverter to minimize switching loss with the absence of switching in the region of the peak phase current. In particular, under the identical average switching frequency, the discontinuous PWM is superior to the other PWMs in high modulation range regarding the waveform quality[15].

2.2 New DPWM method in multi-level inverter

The discontinuous PWM method in two-level inverter can be extended to multi-level inverter. However, the DPWM in multi-level inverter is different from one in two-level inverter. The reason is that the number of rails of the DC-link, to which output voltage of the inverter legs can be clamped, increases according to modulation index. For example, in case of three-level, there are three rails such as a positive, middle and negative rail. Fig. 2 shows the DPWM method in three-level inverter. For high modulation index, each output voltage of the inverter legs can be clamped to the positive rail (Fig. 2(a)) or negative rail (Fig. 2(b)) of the DC-link like the two-level inverter. However, for low modulation index, the middle voltage of the three phases can be clamped to middle rail (Fig. 2(c)) and the maximum voltage can be clamped to middle rail (Fig. 2(d)) or the minimum voltage can be clamped to

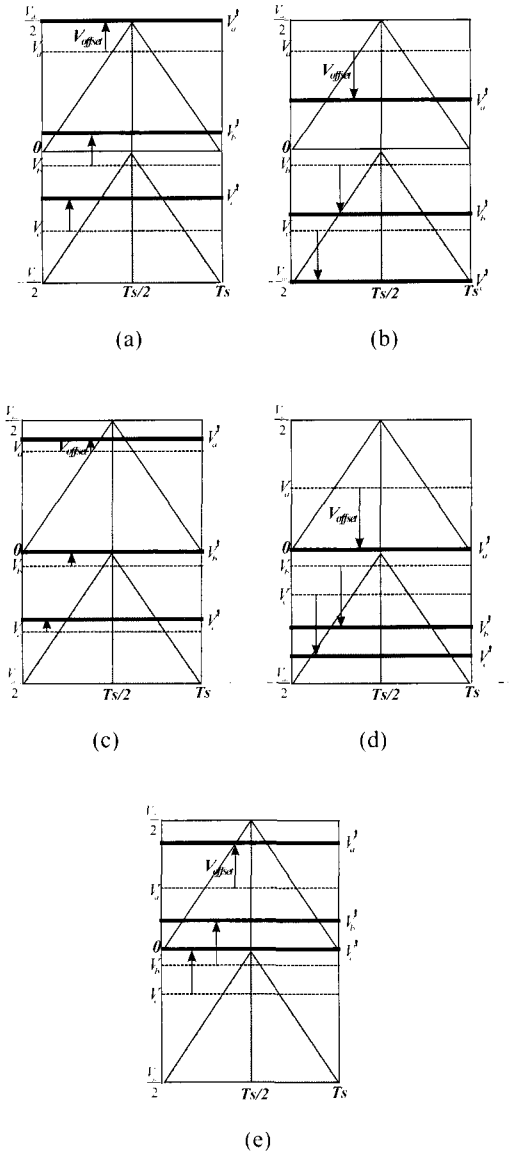


Fig. 2. DPWM method in three-level inverter.

middle rail (Fig. 2(e)). Therefore, the only two cases exist independent of modulation index for two-level inverter, while the maximum five cases exist in low modulation index and the minimum two cases exist in high modulation index for the three-level inverter. Table 2 shows the V_{offset} according to clamping rails in three-level inverter.

Consequently, in case of N-level, the number of rails is N and the number of cases that can clamp the output voltages to rails increases as a N+2 according to modulation index.

Table 2. V_{offset} according to clamping rail in three-level inverter.

Clamping rail	V_{offset}	Condition
Positive rail	$V_{offset} = \frac{V_{dc}}{2} - V_{\max}$	No condition
Negative rail	$V_{offset} = -\frac{V_{dc}}{2} - V_{\min}$	No condition
Middle rail	$V_{offset} = -V_{mid}$	only if $V_{\max} - V_{mid} \le V_{dc}/2$ and $V_{mid} - V_{\min} \le V_{dc}/2$
	$V_{offset} = -V_{\max}$	only if $V_{\max} - V_{\min} \le V_{dc}/2$
	$V_{offset} = -V_{\min}$	only if $V_{\max} - V_{\min} \le V_{dc}/2$

However, these DPWM methods cause the serious variation of the DC-link voltage in NPC inverter because capacitors of the DC-link are not used equally. The NPC inverter has such a problem that an excessive voltage may be added to switching devices when the DC-link voltage unbalancing occurs between each capacitor. Therefore, the DPWM methods cannot be applied to the NPC inverter directly. In order to be applied to the NPC inverter, these discontinuous PWM methods have to be modified.

The proposed DPWM method, which can be applied to the NPC inverter, will be explained in the next section.

3. DC-Link Voltage Control Strategy

3.1 Principle of the DC-link voltage balancing

Fig. 3 shows a schematic of a three-level NPC inverter. The switching states and output leg voltage of three-level inverter are listed in Table 3. There are three kinds of switching states ***P***, ***O*** and ***N*** in each phase, so there exist 27 switching states in three phase three-level inverter.

Fig. 4 shows 27 switch states and 19 voltage space vectors for the three-level inverter. These 19 available vectors can be divided into four different vectors: large, medium, small and zero vectors. The zero vectors are the ones that have all three switches connected at the same point: *ppp*, *ooo* and *nnn*. The large vectors are the ones

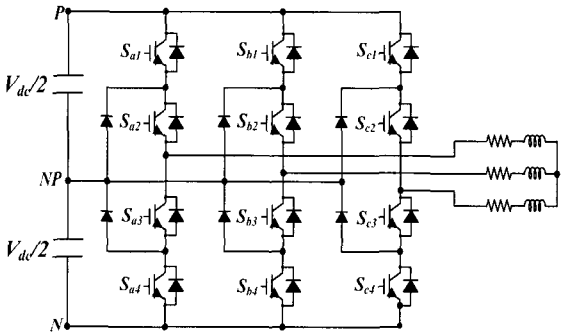


Fig. 3. Three-level NPC inverter.

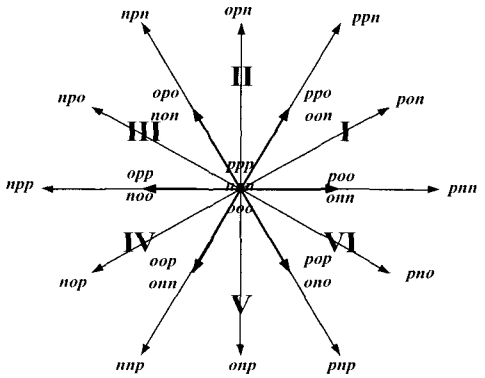


Fig. 4. Switching state vectors.

Table 3. Switching states in three-level inverter.

Switching Symbols	Switching States				Output leg Voltage
	S_{x1}	S_{x2}	S_{x3}	S_{x4}	
P	ON	ON	OFF	OFF	*Vdc/2*
O	OFF	ON	ON	OFF	*0*
N	OFF	OFF	ON	ON	*-Vdc/2*

that have all of the three switches connected to positive(P) and negative(N) point except for the case of all three being connected at the same point: *pnn*, *ppn*, *npn*, *nnp* and *pnp*. The zero vectors and the large vectors are free from the fluctuation of the neutral point potential since the neutral point(NP) current doesn't flow through the neutral point. The medium vectors are the ones that have only one switch connected to neutral point and other two switches connected to positive(P) and negative(N) point each other: *pon*, *opn*, *npo*, *nop*, *onp* and *pno*. For the medium vectors, one of the three output lines is always connected to neutral

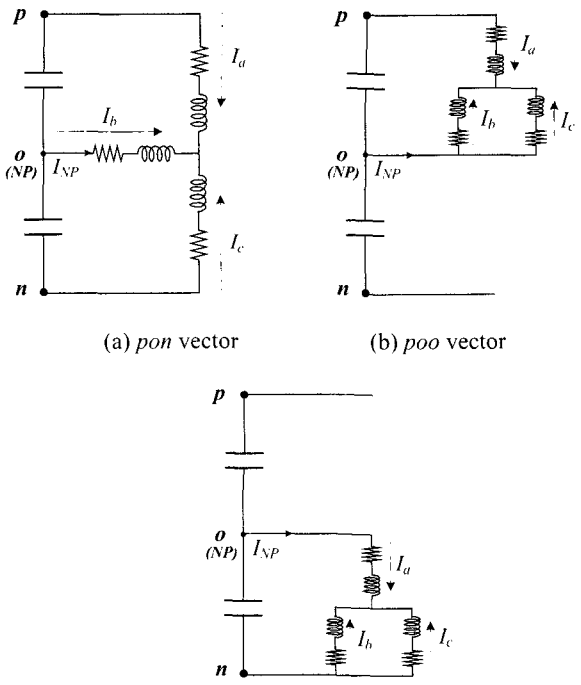
point, so that the *NP* current flows through the neutral point during the time when the vector is used to synthesize the reference vector. The *NP* current direction is decided according to load condition and the *NP* current cause the fluctuation of the neutral point potential. As a result, the unbalancing of the DC-link voltage occurs. The small vectors are the ones that have two switches connected at the same point and the remaining one connected at another adjacent point: *ppo*, *oon*, *opo*, *non*, *opp*, *noo*, *oop*, *nno*, *pop*, *non*, *poo* and *onn*. The small vectors can be divided into six sets of two small vectors. For example, *poo* and *onn* are one set. The two small vectors have the same direction and magnitude but these two small vectors make the *NP* currents with the opposite direction. Therefore, using small vectors, the *NP* current can be controlled. In other words, by selecting appropriate small vectors during each sampling time and by controlling the *NP* current that cause the DC-link unbalancing, the DC-link balancing can be achieved.

Considering the relationship between the voltage vector and the neutral point, the *NP* current can be presented by the load current. Fig. 5 shows some examples. I_b is the current flowing though the neutral point during *pon* vector. $-I_a$ is for *poo* and I_a is for *onn*. Therefore, the relationship between the voltage vectors and the neutral point current can be displayed as Table 4.

The reference vector may be synthesized by the combination of the three switching state vectors that are nearest to it during every sampling time in order to minimize the harmonic component of the output line-to-line voltage. Therefore, the different switching state vectors are decided, depending on where the reference vector is located. The nearest three vectors (V_{s1}, V_{s2}, V_z) are selected by locating the reference vector in one of the four small triangles illustrated in Fig. 6. Due to the circular symmetry of the three-phase system, it is sufficient to consider only the case of sector I, as shown in Fig. 6.

For the inner small triangle shaded in Fig. 6, the reference vector is synthesized as follows.

$$V_{ref} = (d_{s1}V_{s1} + d_{s2}V_{s2} + d_zV_z)/T_s$$
$$d_{s1} + d_{s2} + d_z = T_s \quad (3)$$



(a) *pon* vector (b) *poo* vector

(c) *onn* vector

Fig. 5. Relationship between the *NP* current and the load current.

Table 4. Neutral point current for space vectors.

Small vector	I_{NP}	Small vector	I_{NP}	Medium vector	I_{NP}
onn	I_a	***poo***	$-I_a$	***pon***	I_b
ppo	I_c	***oon***	$-I_c$	***opn***	I_a
non	I_b	***opo***	$-I_b$	***npo***	I_c
opp	I_a	***noo***	$-I_a$	***nop***	I_b
nno	I_c	***oop***	$-I_c$	***onp***	I_a
pop	I_b	***ono***	$-I_b$	***pno***	I_c

d_{s1}, d_{s2} : duration time of the small vectors

d_z : duration time of the zero vector

T_s : sampling time

The sum of these three vectors multiplied by their duration time reproduces the reference vector. At that time, the *NP* current can be found from Table 4.

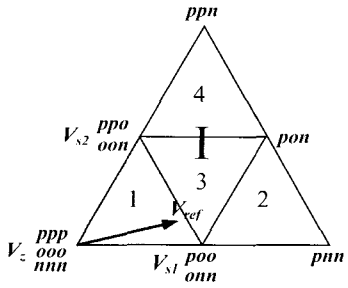


Fig. 6. Reference vector in the inner small triangle.

According to the selected small vectors, the *NP* current can be expressed as follows

$$I_{NP} = d_{s1} I_a + d_{s2}(-I_c) \quad \text{for } onn, oon \qquad (4)$$
$$I_{NP} = d_{s1}(-I_a) + d_{s2} I_c \quad \text{for } poo, ppo$$

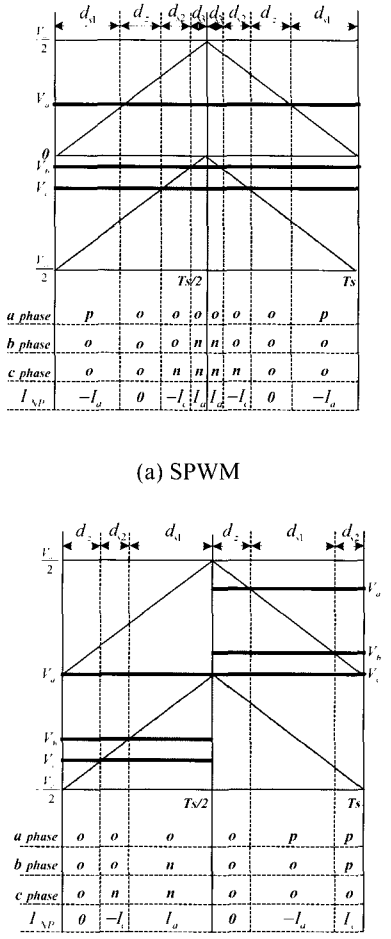
As shown in (4), the actual current of the neutral point is the product of the *NP* current and the duration time of their vectors. This *NP* current causes the fluctuation of the neutral point potential of the DC-link and the unbalancing of DC-link voltage occurs.

Consequently, the desirable output voltage is obtained by synthesizing three switching state vectors that are nearest to the reference vector during every sampling time and at the same time, the *NP* current that causes the DC-link unbalancing flows in the neutral point. Therefore, the DC-link voltage can be balanced by making the *NP* current zero for a sampling time, which is obtained by the combination of the selected vectors and the control of their duration time.

3.2 The proposed DPWM method for balancing DC-link

As explained in the previous section, it is important to note that there are six sets of two small vectors associated with the different switching states and the value of the *NP* currents has the opposite sign for the two small vectors. This property plays an important role in the DC-link balancing of three-level NPC inverter.

To balance the DC-link voltage, the technique of alternative small vector selection is adapted. This means that in shaded regions of Fig. 6, the switching states of *oon* and *onn* are selected for the first half sampling time, while *poo* and *ppo* are selected for the next half sampling time.



(a) SPWM

(b) the proposed DPWM

Fig. 7. Reference vector and Neutral point current.

By this technique, the average of the *NP* current becomes zero for a sampling time, which makes the DC-link voltage balancing.

This technique is simply realized by the proposed DPWM method.

Fig. 7 shows the correlation between the reference vector and the *NP* current in three-level inverter. Fig. 7(a) and 7(b) show the SPWM method and the proposed DPWM method respectively. As shown in Fig. 7(b), the fluctuation of the DC-link voltage can be controlled by using the proposed DPWM method. This DPWM method means that for the first half of the sampling time, the maximum voltage of the three phases is clamped to middle rail and for the next half sampling time, the minimum voltage of the three phases is clamped to middle rail. The

proposed DPWM method is one of the DPWM methods in three-level inverter, which was already explained in section II. To clamp the maximum and minimum voltage to middle rail, it is necessary to add the V_{offset} to each output voltage of the inverter leg. The V_{offset} can be found from Table 2. For the first half sampling time, the V_{offset} of $-V_{\max}$ is added to each output voltage and for the next half sampling time, the V_{offset} of $-V_{\min}$ is added to each output voltage. The proposed DPWM method makes the *NP* currents with the opposite sign flow in the neutral point and it also makes the duration time of the *NP* currents with the opposite sign equal for a sampling time. For example, in Fig. 7(b) the duration time of $-I_c$ for the first half sampling time is equal to the duration time of I_c for the next half sampling time and the duration time of I_a is equal to the duration time of $-I_a$. Therefore, the proposed DPWM method makes the average of the *NP* current, which is the product of the *NP* current and the duration time of their vectors, zero for a sampling time. In Fig. 7(b), when the maximum voltage of the three phases is clamped to middle rail for the first half sampling time, the switching states of *oon* and *onn* result in the *NP* current of $-I_c$ and I_a. When the minimum voltage is clamped to middle rail for the next half sampling time, the switching states of *poo* and *ppo* result in the *NP* current of $-I_a$ and I_c.

The neutral point current for a sampling time is calculated as follows

$$I_{NP1} = d_{s2}(-I_c) + d_{s1}I_a$$
for the first half sampling time

$$I_{NP2} = d_{s1}(-I_a) + d_{s2}I_c$$
for the next half sampling time (5)

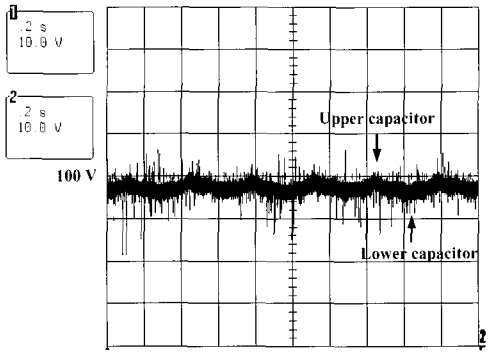
$$I_{NPT} = I_{NP1} + I_{NP2} = 0$$
for a sampling time

Consequently, the proposed DPWM method changes the path and duration time of the *NP* current and makes the overall fluctuation of the DC-link voltage zero during a sampling time. Therefore, the voltage of the DC-link is effectively balanced.

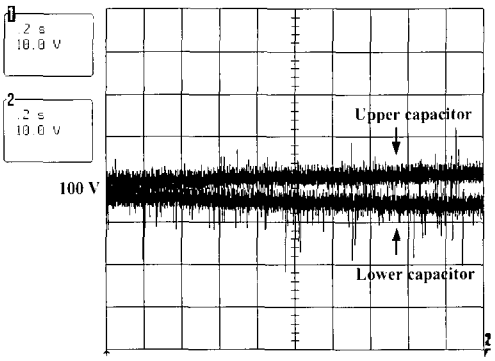
4. Experiment Result

In order to verify the validity of the proposed DPWM and control strategy of the DC-link voltage, the experiment was carried out.

The proposed DPWM method is programmed with the TMS320C31 DSP board and the Mitsubishi CM100DY-6H is used as power devices. 2[hp]-induction motor is used as a load of NPC inverter. The *V/f* control is used to drive the motor and output frequency is 20[Hz]. The capacitance of the DC-link capacitors is 1000[μF] respectively and switching frequency is 8[kHz]. Total DC-link voltage is 200[V] and modulation index is 0.45. Fig. 8 shows two capacitor voltages. In this figure, the DC-link voltage keeps balancing well by the proposed method, while the unbalancing of the DC-link voltage occurs in SPWM method. The proposed method makes the

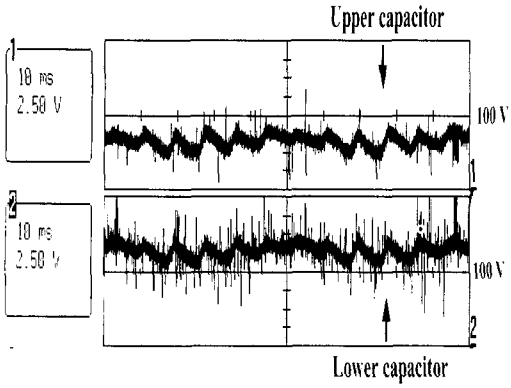


(a) the proposed method

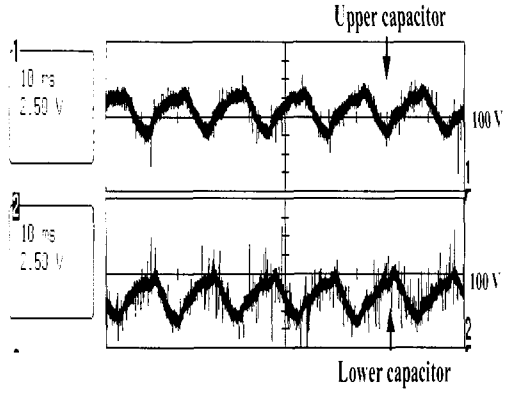


(b) SPWM

Fig. 8. Two capacitor voltages.

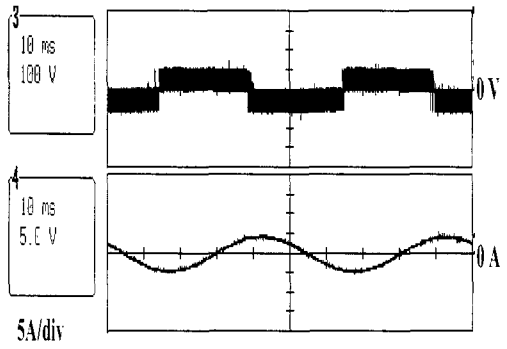


(a) the proposed method

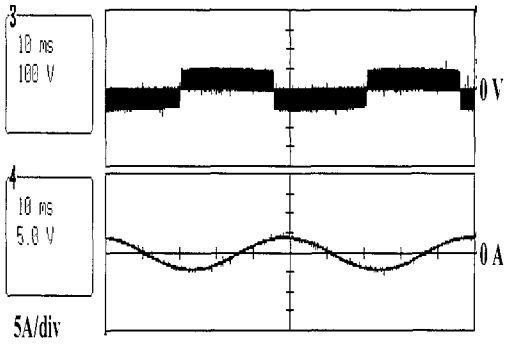


(b) SPWM

Fig. 9. The ripple of DC-link voltage.



(a) the proposed method



(b) SPWM

Fig. 10. Line-to-line voltage and load current.

average of the *NP* current zero for a sampling time, so that the DC-link voltage is balanced. On the other hand, due to the effect of the *NP* current that flows through the neutral point, the DC-link voltage of SPWM method is unbalanced. Fig. 9 is the experiment result of the DC-link voltage ripple. It displays that the DC-link voltage ripple of the proposed DPWM is reduced significantly than one of the SPWM. Fig. 10 shows line-to-line voltage and load current respectively.

Experiment results confirm that the proposed DPWM has good performance for solving the fluctuation of the DC-link voltage at the low modulation index of three-level inverter.

5. Conclusion

This paper proposes a simple control strategy for balancing the DC-link voltage of neutral-point-clamped inverter at low modulation index and presents new DPWM methods in multi-level inverter. The proposed control strategy is based on the DPWM method in three-level inverter. The proposed DPWM method changes the path and duration time of the neutral point currents, which makes the overall fluctuation of the DC-link voltage zero during a sampling time. Therefore, the natural point potential of the DC-link is balanced well. Moreover, the voltage ripple of the DC-link is reduced significantly. In comparison with conventional methods which have to perform the complicated calculation for the DC-link voltage balancing, the proposed method obtains the DC-link voltage balancing simply. The proposed method was verified and illuminated through experiments. The results show that the voltage balance of the DC-link is controlled well by the proposed DPWM and the proposed method is one of the methods to solve the problem that is the fluctuation of the DC-link voltage. Consequently, the proposed method is significantly effective to control the DC-link voltage balancing at low modulation index.

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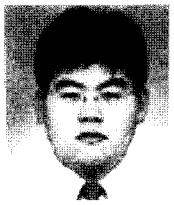

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