

◦ 논문제목

Dielectric property and conduction mechanism of ultrathin zirconium oxide films

◦ 저자

J.P. Chang., Y.S. Lin

◦ 소속

Dept. of chemical Engineering, University of California, Los Angeles, California 90095

◦ 초록

Stoichiometric, uniform, amorphous  $ZrO_2$  films with an equivalent oxide thickness of  $\sim 1.5\text{nm}$  and a dielectric constant of  $\sim 18$  were deposited by an atomic layer controlled deposition process on silicon for potential application in metal-oxide-semiconductor (MOS) devices. The conduction mechanism is identified as Schottky emission at low electric fields and as Poole-Frenkel emission at high electric fields. The MOS devices showed low leakage current, small hysteresis ( $< 50\text{mV}$ ), and low interface state density ( $\sim 2 \times 10^{11} / \text{cm}^2\text{eV}$ ). Microdiffraction and high-resolution transmission electron microscopy showed a localized monoclinic phase of  $\alpha\text{-}ZrO_2$  and an amorphous interfacial  $ZrSi_2O_7$  layer which has a corresponding dielectric constant of 11

◦ 출처

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◦ 논문제목

Metal-dielectric band alignment and its implications for metal gate complementary metal-oxide semiconductor technology

◦ 저자

Tee-Chia Yeo, Tsu-Jae King, and Chenming Hu

◦ 소속

Dept. of Electr. Eng & Comput. Sci., University of California,

Berkeley, California 94720

◦ 초록

The dependence of the metal gate work function on the underlying gate dielectric in advanced metal-oxide-semiconductor (MOS) gate stacks was explored. Metal work function on high-k dielectrics are observed to differ appreciably from their values on  $SiO_2$  of in vacuum. We applied the interface dipole theory to the nterface between the gate and the gate dielectric of a MOS transistor and obtained excellent agreement with experimental data. Important parameters such as the slope parameters for gate dielectrics like  $SiO_2$ ,  $Al_2O_3$ ,  $Si_3N_4$ ,  $ZrO_2$ , and  $HfO_2$  were extracted. In addition, we also explain the weaker dependence of  $n^+$  and  $p^+$  polysilicon gate work functions on the gate dielectric material. Challenges for gate work function engineering are highlighted. This work provides *additional guidelines on the choice of gate materials for future MOS technology incorporating high-k gate dielectrics.*

◦ 출처

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◦ 논문제목

High-k dielectrics by UV photo-assisted chemical vapour deposition

◦ 저자

Q. Fang; J.Y. Zhang; Z.M. Wang; G. He; J. Yu; Ian W. Boyd

◦ 소속

Dept. Electronic & Electrical Engineering, University College London, Torrington Place, London UK

◦ 초록

An overview of our recent work on thin films of metal oxides deposited on silicon by a novel excimer lamp-assisted ultraviolet injection liquid source CVD (UVILS-CVD) process for advanced high-k gate dielectrics applications will be presented. Recent results on  $TiO_2$ ,  $Ta_2O_5$ ,  $ZrO_2$ ,  $HfO_2$ , and  $TiO_2$ -doped  $Ta_2O_5$  will be demonstrated. The physical, structural, interfacial

properties and electrical characterization of the as-deposited and UV-annealed new high dielectric constant (high-k) materials, determined using ellipsometry, Fourier transform infrared spectroscopy, X-ray photoelectron spectroscopy, UV spectrophotometry, SEM, TEM, and C-V, I-V measurements, showed that good quality layers could be produced. The investigation of high-k dielectrics grown by the UVILS-CVD process clearly demonstrates that low cost, high power density excimer lamp systems can provide an interesting alternative to conventional UV lamps and excimer lasers for industrial large-scale low temperature materials processing. UVILS-CVD is a promising technique for the controlled deposition of ultra thin high-k metal-oxide dielectrics for deep sub-micron CMOS devices at temperatures as low as 350°C.

출처

Microelectric Engineering, Volume:1 2002 000-000



논문제목

Annealing Effects On Ultra thin MOS Capacitors

저자

Alvin Chi-hai Ng, Jun Xu, J. B. Xu, W. Y. Cheung

소속

Dept. of Electronic Engineering, Chinese university of Hong Kong, Shatin, the New Territories, Hong Kong

초록

Silicon oxide with thickness less than 9 nm is fabricated by tube furnace oxidation. Nitrogen is added to dilute the oxidation rate. Aluminum dots with radius of 0.05 μm are deposited on the oxide. High frequency capacitance-voltage (HF C-V), conductance-voltage (G-V) and current-voltage (I-V) characteristics are measured. Annealing under nitrogen atmosphere is carried out with different time and at different temperature. Densities of the interface states before and after annealing are compared. After annealing, a decrease in density of the interface states is found. Experiments show that 450°C annealing for 30 minutes has the lowest density of the interface states.

출처

Electron Device Meeting, IEEE Hong-Kong (2001) Page(s): 101-104



논문제목

Material characteristics of electrically tunable zirconium oxide thin films

저자

Byeong-Ok Cho and Jane P. Chang

소속

Dept. of Chemical Engineering, University of California, Los Angeles, California 90095

초록

Material characteristics of zirconium oxide thin films obtained by plasma enhanced chemical vapor deposition on p-type Si (100) substrates were investigated to explain their tunable electrical properties. The films obtained without heating had polycrystalline nanograins that are mostly of a tetragonal phase under oxygen-deficient plasma conditions but transformed into a monoclinic phase with increasing O<sub>2</sub> addition in the plasma. Mostly amorphous bulk ZrO<sub>2</sub> with a relatively thicker and smoother interfacial layer was obtained from oxygen-rich plasmas, resulting in a decrease in both the overall dielectric constant and the leakage current density. The interfacial layer formed between the bulk ZrO<sub>2</sub> and Si substrate was analyzed to be zirconium silicate, which approached SiO<sub>2</sub> as its zirconium content decreased with the increasing gas phase O<sub>2</sub> content.

출처

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논문제목

Effective electron mobility in Si inversion in metal-oxide-semiconductor systems

with a high-k insulator: The role of remote phonon scattering

· 저자

Massimo V. Fischetti, Deborah A. Neumayers, and Eduard A. Caritier

· 소속

IBM Research Division, Thomas J. Watson Research Center, P.O. Box218 Yorktown Heights, New York 10598

· 초록

The high dielectric constant of insulators currently investigated as alternatives to SiO<sub>2</sub> in metal-oxide-semiconductor structures is due to their large ionic polarizability. This is usually accompanied by the presence of soft optical phonons. We show that the long-range dipole field associated with the interface excitations resulting from these modes and from their coupling with surface plasmons, while small in the case of SiO<sub>2</sub>, for most high-k materials causes a reduction of the effective electron mobility in the inversion layer of the Si substrate. We study the dispersion of the interfacial coupled phonon-plasmon modes, their electron-scattering strength, and their effect on the electron mobility for Si-gate structures employing films of SiO<sub>2</sub>, Al<sub>2</sub>O<sub>3</sub>, AlN, ZrO<sub>2</sub>, HfO<sub>2</sub>, and ZrSiO<sub>4</sub> for "SiO<sub>2</sub>-equivalent" thickness ranging from 5 to 0.5 nm

· 출처

Journal of Applied Physics, Volume:90 Issue:9 Nov. 2001 Page(s): 4587-4608

· 논문제목

Al<sub>2</sub>O<sub>3</sub> formation on Si by catalytic chemical vapour deposition

· 저자

Yoh-Ichiro Ogita, Shinshi Iehara, Toshiyuki Tomita

· 소속

Dept. of Electrical and Electronic Engineering, Kanagawa Institute of Technology, 1030 Shimo-ogino, Atsugi 243-0292, Japan

· 초록

Catalytic chemical vapor deposition (Cat-CVD) has been developed to deposit alumina (Al<sub>2</sub>O<sub>3</sub>) thin films on silicon (Si)

crystal using N<sub>2</sub> bubbled tri-methyl aluminium [Al(CH<sub>3</sub>)<sub>3</sub>, TMA] and molecular oxygen (O<sub>2</sub>) as source species and tungsten wires as a catalyzer. The catalyzer dissociated TMA at approximately 600°C. The maximum deposition rate was 18 nm/min at a catalyzer temperature of 1000 and substrate temperature of 800°C. Metal oxide semiconductor (MOS) diodes were fabricated using gates composed of 32.5-nm-thick alumina film deposited at a substrate temperature of 400°C. The capacitance measurements resulted in a relatively dielectric constant of 7.4, fixed charge density of 1.74\*10<sup>12</sup>/cm<sup>2</sup>, small hysteresis voltage of 0.12V, and very few interface trapping charge. The leakage current was 5.01\*10<sup>-7</sup> A/cm<sup>2</sup> at a gate bias of 1V.

· 출처

Thin Solid Films, Volume:430 Issues:1-2 Apl. 2003 Page(s): 161-164

· 논문제목

Epitaxial growth of yttrium-stabilized HfO<sub>2</sub> high-k gate dielectric thin films on Si

· 저자

J. Y. Dai, P. F. Lee, K. H. Wong, H. L. W. Chan, and C. L. Choy

· 소속

Dept. of Applied Physics, The Hong Kong Polytechnic University, Hong Kong, China

· 초록

Epitaxial yttrium-stabilized HfO<sub>2</sub> thin films were deposited on p-type (100) Si substrates by pulsed laser deposition at a relatively lower substrate temperature of 550°C. Transmission electron microscopy observation revealed a fixed orientation relationship between the epitaxial film and Si; that is, (100)Si//[100]HfO<sub>2</sub> and [001]Si//[001]HfO<sub>2</sub>. The film/Si interface is not atomically flat, suggesting possible interfacial reaction and diffusion. X-ray photoelectron spectrum analysis also revealed the interfacial reaction and diffusion evidenced by Hf silicate and Hf-Si bond formation at the interface. The epitaxial growth of the yttrium stabilized HfO<sub>2</sub> thin film on bare Si is via a direct growth

mechanism without involving the reaction between Hf atoms and SiO<sub>2</sub> layer. High-frequency capacitance-voltage measurement on an as-grown 40-Å yttrium-stabilized HfO<sub>2</sub> epitaxial film yielded an effective dielectric constant of about 14 and equivalent oxide thickness to SiO<sub>2</sub> of 12 Å. The leakage current density is  $7.0 \times 10^{-2}$  A/cm<sup>2</sup> at 1 V gate bias voltage.

◦ 출처

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Page(s): 912-915

◦ 논문제목

Basic characteristics of metal-ferroelectric-insulator-semiconductor structure using a high-k PrOx insulator layer

◦ 저자

Minoru Noda, Kazushi Kodama, Satoshi Kitai, Mitsue Takahashi, Takeshi Kanashima, and Masanori Okuyama

◦ 소속

Area of Materials and Device Physics, Department of Physical Science, Graduate School of Engineering Science, Osaka University, 1-3 Machikaneyama-Cho, Toyonaka, Osaka, 560-8531, Japan

◦ 초록

A metal-ferroelectric [SrBi<sub>2</sub>Ta<sub>2</sub>O<sub>9</sub> (SBT)]-high-k-insulator(PrOx)-semiconductor(Si) structure has been fabricated and evaluated as a key part of metal-ferroelectric-insulator-semiconductor-field-effect-transistor MFIS-FET memory, aiming to improve the memory retention characteristics by increasing the dielectric constant in the insulator layer and suppressing the depolarization field in the SBT layer. A 20-nm PrOx film grown on Si(100) showed both a high of about 12 and a low leakage current density of less than  $1 \times 10^{-8}$  A/cm<sup>2</sup> at 1.5 MV/cm. A 400-nm SBT film prepared on PrOx/Si shows a preferentially oriented (105) crystalline structure, grain size of about 130 nm and surface roughness of 3.2 nm. A capacitance-voltage hysteresis is confirmed on the Pt/SBT/PrOx/Si diode with a memory window of 0.3 V at a sweep voltage width of 12 V. The memory retention time was about 1 104 s, comparable to

the conventional Pt/SBT/SiO<sub>2</sub>N<sub>x</sub>(SiO<sub>2</sub>)<sub>x</sub>/Si. The gradual change of the capacitance indicates that some memory degradation mechanism is different from that in the Pt/SBT/SiON/Si structure.

◦ 출처

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◦ 논문제목

Atomic layer chemical vapor deposition of ZrO<sub>2</sub>-based dielectric films: Nanostructure and nanochemistry

◦ 저자

S. K. Dey

◦ 소속

Chemical and Materials Engineering, and Electrical Engineering, Arizona State University, Tempe, Arizona 85287-6006

◦ 초록

A 4 nm layer of ZrOx (targeted x~2) was deposited on an interfacial layer (IL) of native oxide (SiO<sub>2</sub>, t~1.2 nm) surface on 200 mm Si wafers by a manufacturable atomic layer chemical vapor deposition technique at 300°C. Some as-deposited layers were subjected to a post-deposition, rapid thermal annealing at 700°C for 5 min in flowing oxygen at atmospheric pressure. The experimental x-ray diffraction, x-ray photoelectron spectroscopy, high-resolution transmission electron microscopy, and high-resolution parallel electron energy loss spectroscopy results showed that a multiphase and heterogeneous structure evolved, which we call the Zr-O/IL/Si stack. The as-deposited Zr-O layer was amorphous ZrO<sub>2</sub>-rich Zr silicate containing about 15% by volume of embedded ZrO<sub>2</sub> nanocrystals, which transformed to a glass nanoceramic (with over 90% by volume of predominantly tetragonal-ZrO<sub>2</sub> (t-ZrO<sub>2</sub>) and monoclinic-ZrO<sub>2</sub> (m-ZrO<sub>2</sub>) nanocrystals) upon annealing. The formation of disordered amorphous regions within some of the nanocrystals, as well as crystalline regions with defects, probably gave rise to lattice strains and deformations. The interfacial layer (IL) was

partitioned into an upper SiO<sub>2</sub>-rich Zr silicate and the lower SiO<sub>x</sub>. The latter was sub-stoichiometric and the average oxidation state increased from Si<sup>0.86+</sup> in SiO<sub>0.43</sub> (as-deposited) to Si<sup>1.32+</sup> in SiO<sub>0.66</sub> (annealed). This high oxygen deficiency in SiO<sub>x</sub> was indicative of the low mobility of oxidizing specie in the Zr-O layer. The stacks were characterized for their dielectric properties in the Pt/(Zr-O/IL)/Si metal oxide-semiconductor capacitor (MOSCAP) configuration. The measured equivalent oxide thickness (EOT) was not consistent with the calculated EOT using a bilayer model of ZrO<sub>2</sub> and SiO<sub>2</sub>, and the capacitance in accumulation (and therefore, EOT and kZr-O) was frequency dispersive, trends well documented in literature. This behavior is qualitatively explained in terms of the multi-layer nanostructure and nanochemistry that evolves.

◦ 출처

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◦ 논문제목

Interfacial properties of ZrO<sub>2</sub> on silicon

◦ 저자

Y.-S. Lin, R. Puthenkovilakam, and J. P. Chang

◦ 소속

Dept. of Chem. Engineering, University of California, Los Angeles, California

◦ 초록

The interface of zirconium oxide thin films on silicon is analyzed in detail for their potential applications in the microelectronics. The formation of an interfacial layer of ZrSi<sub>2</sub>O<sub>7</sub> with graded Zr concentration is observed by the x-ray photoelectron spectroscopy and secondary ion mass spectrometry analysis. The as-deposited ZrO<sub>2</sub>/ZrSi<sub>2</sub>O<sub>7</sub>/Si sample is thermally stable up to 880°C, but is less stable compared to the ZrO<sub>2</sub>/SiO<sub>2</sub>/Si samples. Post-deposition annealing in oxygen or ammonia improved the thermal stability of as-deposited ZrO<sub>2</sub>/ZrSi<sub>2</sub>O<sub>7</sub>/Si to 925°C, likely due to the oxidation/nitridation of the interface. The as-deposited film had an equivalent oxide

thickness of ~1.3 nm with a dielectric constant of ~21 and a leakage current of 3.2 × 10<sup>-3</sup> A/cm<sup>2</sup> at 1.5 V. Upon oxygen or ammonia annealing, the formation of SiO<sub>x</sub> and SiH<sub>3</sub>N<sub>2</sub>O<sub>x</sub> at the interface reduced the overall dielectric constants.

◦ 출처

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◦ 논문제목

Dielectric properties of Pr<sub>2</sub>O<sub>3</sub> high-k films grown by metalorganic chemical vapor deposition on silicon

◦ 저자

Raffaella Lo Nigro, Vito Raineri, and Corrado Bongiorno

◦ 소속

IMM, sezione di Catania, CNR, Stradale Primosole n 50, 95121 Catania, Italy

◦ 초록

Praseodymium oxide (Pr<sub>2</sub>O<sub>3</sub>) thin films have been deposited on Si(100) substrates by metalorganic chemical vapor deposition using praseodymium tris-2,2,6,6-tetramethyl-3,5-heptandionate as source material. Film structural, morphological, and compositional characterizations have been carried out. Dielectric properties have been studied as well by capacitance-voltage and current-voltage measurements on metal-oxide-semiconductor capacitors of several areas. The Pr<sub>2</sub>O<sub>3</sub> films have shown a dielectric constant =23-25 and a leakage current density of 8.8 × 10<sup>-8</sup> A/cm<sup>2</sup> at +1 V.

◦ 출처

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담당위원 : 윤일구 교수(연세대)