Electrical Characteristics of Thin SiO_2 Layer

Nung-Pyo Hong* and Jin-Woong Hong**

Abstract - This paper examines the electrical characteristic of single oxide layer due to various diffusion conditions, substrate orientations, substrate resistivity and gas atmosphere in a diffusion furnace. The oxide quality was examined through the capacitance-voltage characteristic due to the annealing time after oxidation process, and the capacitance-voltage characteristics of the single oxide layer by will be described via semiconductor device simulation.

Keywords: MOS, Breakdown strength, Oxide(SiO_2), C-V Plot

1. Introduction

Since the invention of the first integrated circuit in 1960, there has been an ever-increasing density of devices manufacturable on semiconductor substrate. Today, the thickness of the insulation layer of semiconductor devices increases with integrated technology, but the size of memory decreases, which complicates the process[1,2].

So it is more important to acquire efficiency of progress and reliability. For a metal oxide semiconductor(MOS) structure device and bipolar junction transistor, the potential level of the oxide layer increases as the electric field focuses on the very thin layer[3,4], and it brings out the dielectric breakdown of oxide layer and decreases the life of devices.

When applied to low electric fields, this breakdown is insignificant, but in typical electric fields, the breakdown is serious if the oxide layer contains micro defects. The thickness traps and the various kinds of ions on the layer interface greatly influence the characteristic of device[5,6].

The purpose of this paper is to describe the electrical characteristics of a single oxide layer, such as breakdown strength and capacitance-voltage characteristics, due to different diffusion process.

2. Experimental

2.1 Composition of Samples

We started with a 100[mm] silicon wafer (manufactured by Shinetsu Co.), and <111> and <100> oriented and N-doped materials (substrate resistivity 15-20 Ω [cm]) were chosen as a substrate.

These wafers are thermally oxidized in quartz furnaces. To obtain higher density thermal oxide, they are made with two additional dry oxidation steps and are thus called dry-wet-dry structures [3].

The desired oxide layer thickness could be extracted from a Nanometrics 210(Film Thickness System). The first sample group was used for the measurement of oxide breakdown strength. The polished wafers were thermally oxidized under some conditions. A MOS is made with the thickness of 600[Å], 800[Å], and 1000[Å] under thermal oxidation in quartz furnaces. The highly doped poly-silicon was deposited on the thin oxide. The silicon wafer was made from front-side with an evaporated aluminum electrode of 40k[Å] thickness on the poly-silicon.

The second sample group was used for the measurement of capacitance-voltage plot. The polished wafers were cleaned at the condition of SCI and 2000:1 HF etching and then oxidized in quartz furnaces. After the oxidation, the sample was annealed. The unwanted oxide layer on the backside of the substrate wafer was removed by chemical etching using the SEG102(Spin Processor Co.). 10[kÅ] of aluminium was deposited on the oxide. The mask for C-V measurement was used.

2.2 Breakdown Strength

The breakdown strength was measured by the current voltage tester for each MOS capacitor. To measure the DC breakdown test, the TO-220 package was molded. The increasing rate of voltage was about 1.67[V/sec] and the measurements were taken at temperatures of 30-100[℃]. The SEM photograph of the vertical structure of the measured sample for breakdown strength is shown in Fig. 1.

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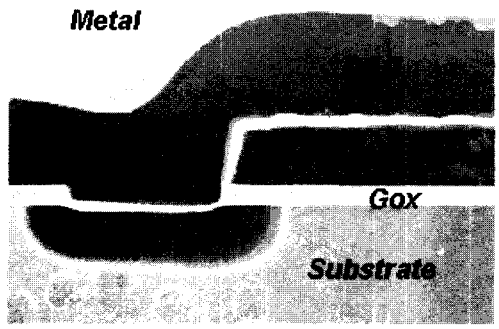

Fig. 1 Vertical structure of measured sample for break down strength by SEM

3. Results and Discussion

3.1 Breakdown Strength

The samples were made with the several process conditions, which are O2/TLC, dry(O2) and wet(H2O2) conditions. They have different oxide thicknesses.

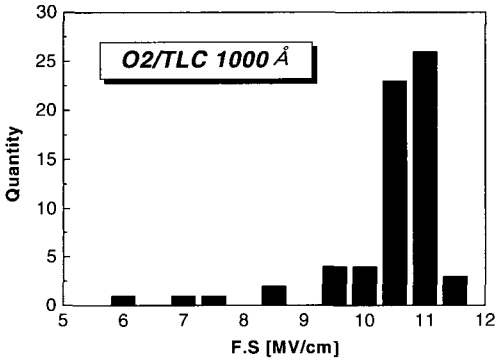

Fig. 2 Breakdown strength in <111> orientation

Figs. 2 and 3 show the actual result of the breakdown strength of <111> and <100> oriented wafers, respectively.

Field strength(FS) was calculated from Equation (1).

$$F.S[MV/cm] = \frac{BreakdownVoltage[V]}{OxideThickness} \quad (1)$$

The <111> oriented wafer has a higher breakdown strength than the <100> oriented wafer. Better results were obtained with the wet (H2,O2) condition than with the O_2/TLC and dry (O2) conditions as shown in Figs. 4 and 5.

$$Wet(H_2O_2) \geq O_2/TLC \geq Dry(O_2)$$

We can know that the radicals related to OH- or water on the wet oxidation condition, fill micro pores or voids and avoid generating them, while there are micro pore or void on the dry oxidation condition. Field strengths are believes to be higher with greater thickness but lower with less thickness because an attack occurs at the metal deposition.

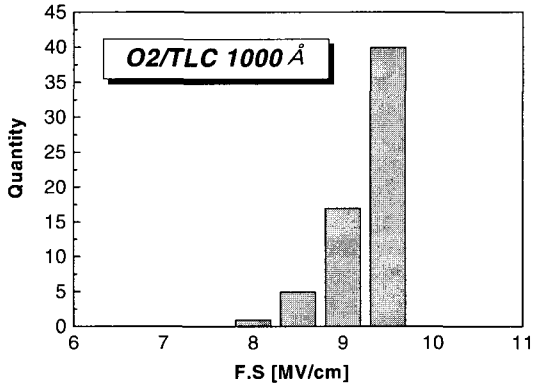

Fig. 3 Breakdown strength in <100> orientation

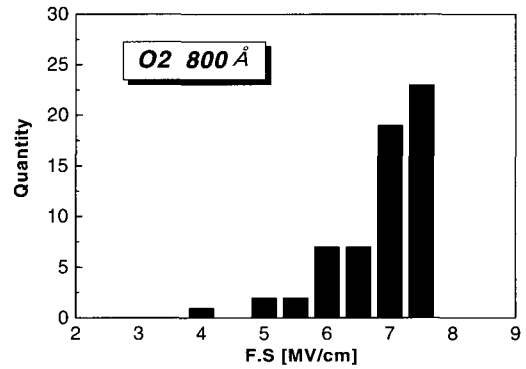

Fig. 4 Breakdown strength in <100> orientation

The substrate orientation and thickness of the oxide layer prepared with different process conditions are compared in Table.1.

The FS value dependence due to temperature and substrate resistivity is shown in Fig. 6. The thickness of the gate oxide layer is 600[Å]. It is confirmed that dielectric strength increases with relative temperature. F.S is inversely proportional with temperature, but positively proportional with resistivity.

Table 1 The average F.S actual value of sample.

Condition	Orientation	Thickness[Å]	F.S
O2/TLC	<111>	1000	10.8
	<100>	1000	9.2
	<100>	600	9.3
Dry(O2)	<100>	900	9.0
	<100>	800	8.3
Wet(H2O2)	<100>	1200	9.7

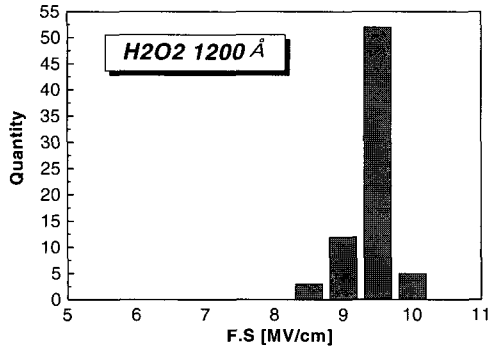

Fig. 5 Breakdown strength in <100> orientation

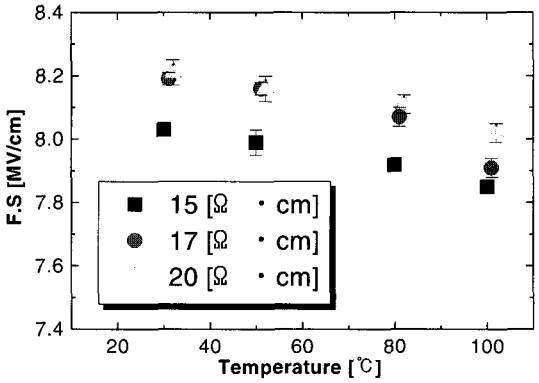

Fig. 6 F.S value dependence vs. temperature and resistivity

3.2 C-V Characteristics.

3.2.1 Simulation Result

Figs. 7 and 8 show the simulated capacitance-voltage characteristics at several oxide thicknesses. The reduction of capacitance observed in the accumulation mode at gate negative bias is due to current flow. Fig. 9 shows the simulated potential and electric field profile at single layers of oxide by Athena, a semiconductor device simulation tool made by Silvaco Co..

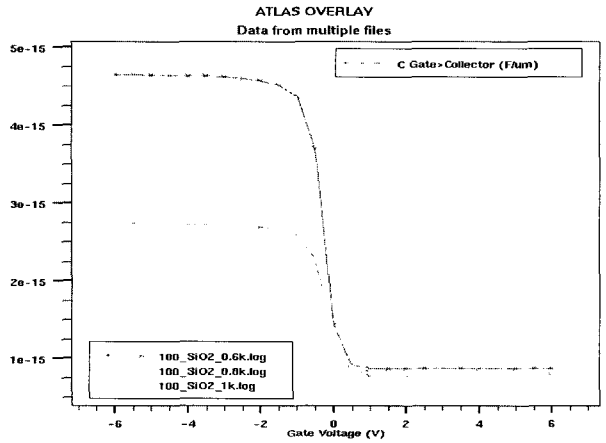

Fig. 7 Capacitance of the sample at different thickness

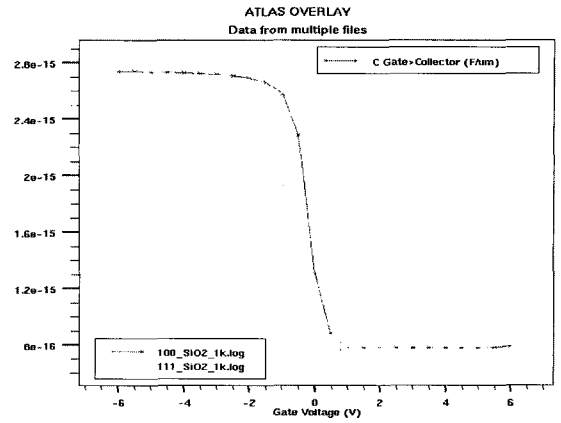

Fig. 8 Capacitance of the sample at different orientation.

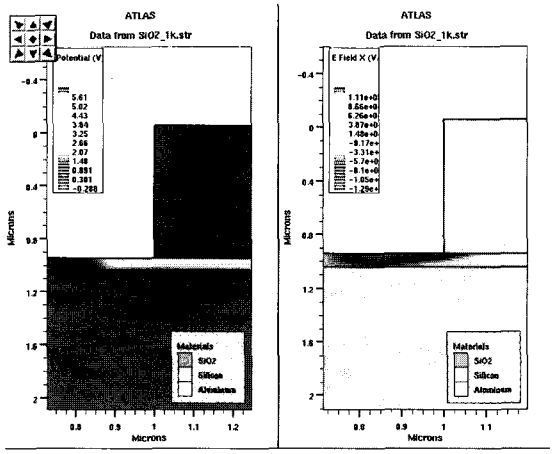

Fig. 9 Potential profile and electric field by capacitance-voltage bias of the 1k Å (SiO_2) sample.

3.2.2 Experimental Result

The substrate orientation and thickness of the oxide layer prepared with different process conditions are compared in Table 2.

Table 2 C-V plot of actual data due to process condition.

Condition	△Fb	Qmi [e10/cm^2]	Qf [e10/cm^2]
<100> 1000 Å N_2(0')	-0.297	0.167	14.2
<100> 1000 Å N_2(10')	-0.319	0.117	14.9
<100> 1000 Å N_2(30')	-0.338	0.220	17.7
<100> 1000 Å N_2(30')+ann.	-0.018	0.109	2.90
<100> 600 Å N_2(30')+ann.	-0.032	0.298	1.54
<111> 1000 Å N_2(30')+ann.	-0.171	0.344	15.3

We have a good result with the 600[Å] thick sample. But the <111> oriented wafer has a large shift of $\triangle F_B$. We confirmed that the fixed oxide charge (Qf) was more with the <111> oriented wafer than with the <100> oriented wafer, because of the excessive silicon atoms.

The surface fixed charge is known to be dependent on the oxidation condition and the high temperature annealing process in the N_2 condition after the oxidation

While there were no differences in the N_2 annealing condition 0 minute, 10 minute and 30 minute after the oxidation.

4. Conclusion

The field strength of oxidation at silicon substrate with the interface <111> of wafer <111>'s orientation has an order wet (H_2,O_2) > O_2/TLC > dry (O_2)

Through the capacitance-voltage measurement, the fixed oxide charge(Q_f) was more with the <111> oriented wafer than with the <100> oriented wafer, because of excessive silicon atoms.

The surface fixed charge is dependent on the oxidation condition and the high temperature annealing process in the N_2 condition after the oxidation. The fixed oxide charge (Qf) was much more with the <111> oriented wafer than with the <100> oriented wafer.

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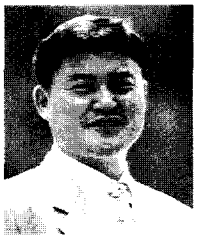

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