Determination of End Point for Direct Chemical Mechanical Polishing of Shallow Trench Isolation Structure

Yong-Jin Seo*, Kyoung-Jin Lee*, Sang-Yong Kim, and Woo-Sun Lee*****

Abstract - In this paper, we have studied the in-situ end point detection (EPD) for direct chemical mechanical polishing (CMP) of shallow trench isolation (STI) structures without the reverse moat etch process. In this case, we applied a high selectivity slurry (HSS) that improves the silicon oxide removal rate and maximizes oxide to nitride selectivity. Quite reproducible EPD results were obtained, and the wafer-to-wafer thickness variation was significantly reduced compared with the conventional predetermined polishing time method without EPD. Therefore, it is possible to achieve a global planarization without the complicated reverse moat etch process. As a result, the STI-CMP process can be simplified and improved using the new EPD method.

Keywords: Shallow trench isolation (STI), chemical mechanical polishing (CMP), end point detection (EPD), high selectivity slurry (HSS), reverse moat etch process

1. Introduction

Recently, the shallow trench isolation (STI) method has attracted attention as an indispensable technology for the integration of semiconductor devices [1, 2]. The method consists of three steps: making a shallow trench on a silicon wafer, depositing SiO_2 in the trench, and then planarizing with the chemical mechanical polishing (CMP) process. The method can separate devices with much narrower area and shows much better performance than the conventional local oxidation of silicon (LOCOS) method, which causes bird's beak structures [3]. However, using a complicated reverse moat etch process is still unavoidable since the sufficient polishing selectivity of SiO_2 to Si_3N_4 cannot be obtained from conventional low polishing slurries. By the etch process, the high density moat regions can be reduced to an acceptable level, and, therefore, the chip or wafer level polishing uniformity can be greatly enhanced. If the direct CMP without the reverse moat etch process were applied with conventional low selectivity slurries, damage might occur on the active regions in case of excessive CMP, whereas in the case of insufficient CMP, some nitride residues might remain in the active regions after nitride strip process due to the oxide residues [4, 5]. As a solution to these problems, the development of a high selectivity slurry (HSS) with high polishing selectivity of silicon oxide and silicon nitride has been widely studied [6, 7].

In this paper, we have studied the factors affecting the end point detection (EPD) method based on motor current (MC) [8, 9] and tested the EPD method for the CMP process of STI structures without the reverse moat etch pattern. We have also applied the HSS to the direct STI-CMP process without reverse moat etch step and evaluated the EPD method for the application of the STI-CMP process.

2. Experiments

Fig. 1 shows schematically the direct STI-CMP process

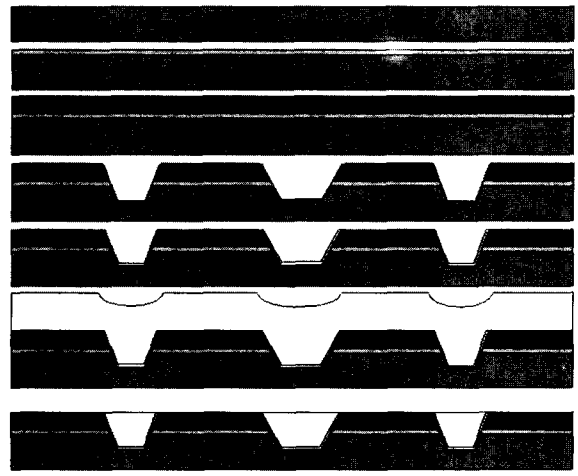

Fig. 1 Sequence of steps in the direct STI-CMP process without reverse moat etch.

* Department of Electrical Engineering, DAEBUL University, Chonnam, Korea (syj@mail.daebul.ac.kr, leekj@mail.daebul.ac.kr).
** ANAM Semiconductor Inc., Bucheon, Korea.
*** Chosun University, Gwangju, Korea (wslee@mail.chosun.ac.kr).
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without the reverse moat etch step. First, 150 Å of thermally grown pad oxide and 2000 Å of silicon nitride were deposited. Silicon trenches of 3500 Å were etched using the moat pattern and dry etching. After the removal of the photo resist, the wafers were cleaned. A sidewall oxide layer of 270 Å was grown by dry oxidation followed by an atmosphere pressure chemical vapor deposition (APCVD) of 8000 Å thick oxide to refill the shallow trenches. The sample wafers were then polished through the direct STI-CMP process without the reverse moat etch step. In this case, we used the HSS instead of the conventional oxide slurry. The HSS is composed of 25 % (by weight) fumed silica slurry with self-developed additives to improve the silicon oxide removal rate and maximize the oxide-to-nitride selectivity by forming a selective passivation layer on the silicon nitride and etching silicon oxide selectively. Before the EPD test, we optimized the CMP process to get a better polishing result. The polishing procedure and conditions for the optimized CMP process are shown in Table 1. The process is composed of five successive phases. In phases 1, 3, and 5, the polishing actions last for 30 sec, whereas no applied down force and back-pressure occur during the 5 sec of polishing in phases 2 and 4.

Rodel's IC 1000/Suba IV pad was used, and the mode of pad conditioning was just-while, where intersweep delay time was 19 sec and conditioning time per segment was 1.3 sec with a total of 10 segments. Luxtron's 2350 system was also used to obtain the motor current (MC) signal from both the polishing platen and carrier head. Table 2 shows the detailed polishing conditions used in this experiment.

Table 1 Polishing procedure and conditions for the optimized CMP process.

Items	Polish time (sec)	Down force (psi)	Back pressure (psi)	Speed (rpm)	
				Platen	Carrier
Phase 1	30	7	4.5	95	50
Phase 2	5	0	0	95	50
Phase 3	30	7	4.5	95	50
Phase 4	5	0	0	95	50
Phase 5	30	7	4.5	95	50

Table 2 Detailed polishing conditions.

Process conditions	
Platen speed	95 rpm
Carrier speed	50 rpm
Down force	7 psi
Back pressure	4.5 psi
Arm oscillation range	126 - 131 mm
Oscillation speed	5 mm/sec
Conditioning mode	Just-While
Intersweep delay	19 sec
Conditioning time	1.3 sec/segments

3. Results and discussion

Figs. 2 and 3 show the MC signals from the polishing platen and carrier head with phase separation, as shown in Table 1. The first and second sudden decreasing / increasing regions indicate phases 2 and 4, respectively, where no polishing action occurs, and the final sudden changes indicate the end points (EPs).

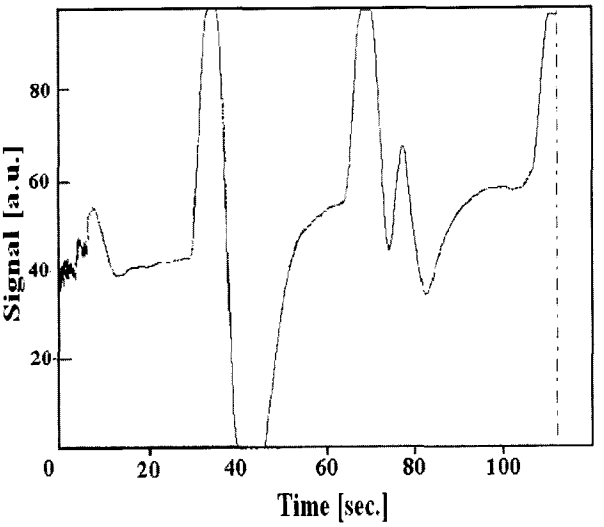


Fig. 2 Extraction of the signal from the platen state with phase separation.

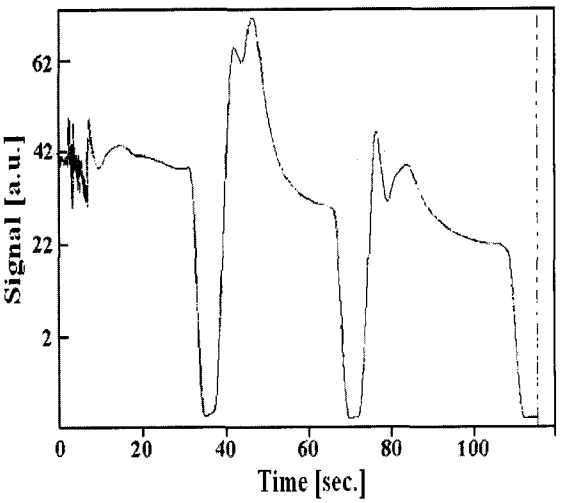
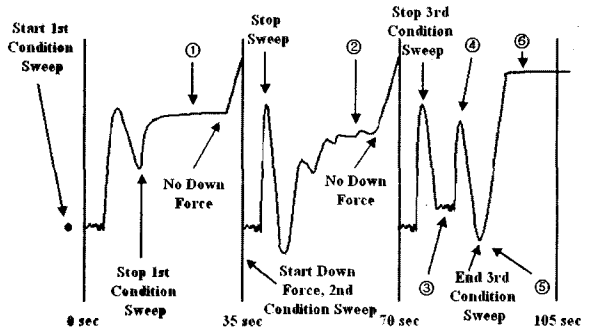


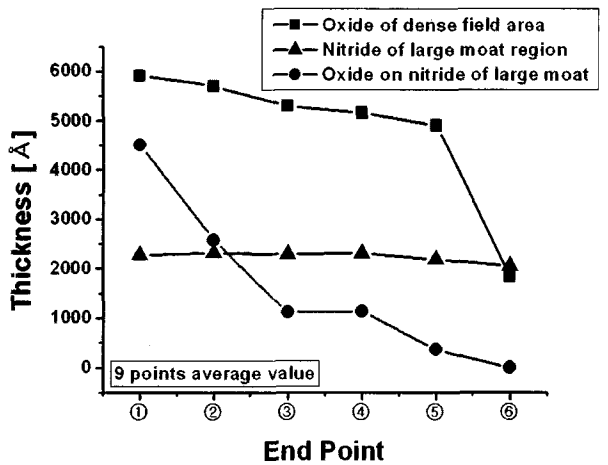
Fig. 3 Extraction of the signal from the carrier head state with phase separation.

More details about the signal from the carrier head and the thickness of each layer at each part of the signal are given in Fig. 4(a). The test wafer has an initial oxide thickness of 7600 Å with a trench depth of 3500 Å, and the target oxide thickness after the CMP process is 4500 Å. Here, point ① is the polishing time, 27 sec, in phase 1; point ②

is the polishing time, 18 sec, in phase 3; point ③ is the polishing time, 14 sec, in phase 5; the nitride layer starts to be polished partially; point ④ is the polishing time, 18 sec, in phase 5; point ⑤ is the polishing time, 24 sec, in phase 5, where the topology of oxide layer is almost eliminated; and point ⑥ denotes the EP, where over 95 % of silicon oxide on the silicon nitride layer is removed. As shown in Fig. 4(b), the nitride film of the large moat region was not removed due to high selectivity between the SiO_2 and Si_3N_4 film. However, as the polishing continuously proceeds, the oxide film on the nitride layer of the large moat region was completely polished, indicating that acceptable EPD results can be obtained.



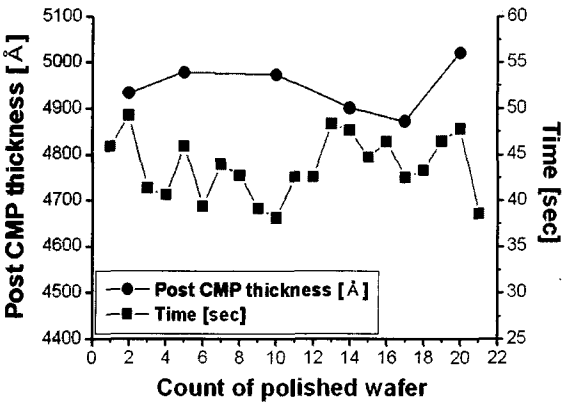
(a) Variation of carrier head signal as a function of polishing time in HSS STI-CMP processing.



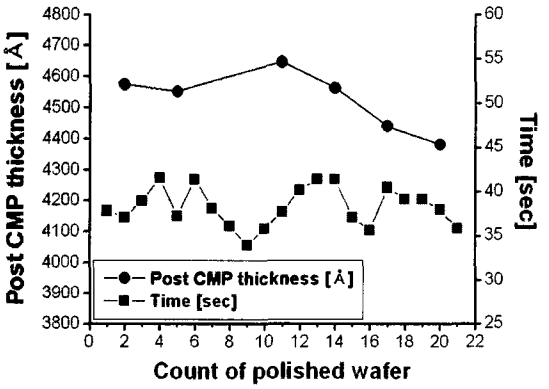
(b) Wafer thickness variations as a function of polishing time in HSS STI-CMP processing.

Fig. 4 Detailed analysis of the MC signal from the carrier head.

In order to verify the effectiveness of the EPD method, we compared the wafer-to-wafer thickness variation with the new EPD method and that of conventional predetermined polishing time without EPD method. Fig. 5(a) shows the thickness variation for the first, twenty-one polished wafers when the EPD method was applied, the thickness variation was about 85 Å. The new EPD times were controlled within a range from 37 sec to 50 sec, respectively. When the test was repeated for another twenty-one wafers, a quite reproducible result could be obtained as shown in Fig. 5(b), where the thickness variation is about 110 Å. The EPD time was varied from 33 sec to 42 sec. The reproducibility is an essential factor for adapting the EPD system to the actual manufacturing process.



(a) Thickness variation for first twenty-one wafers.



(b) Thickness variation for next twenty-one wafers.

Fig. 5 Wafer-to-wafer thickness variation when the new EPD method is applied.

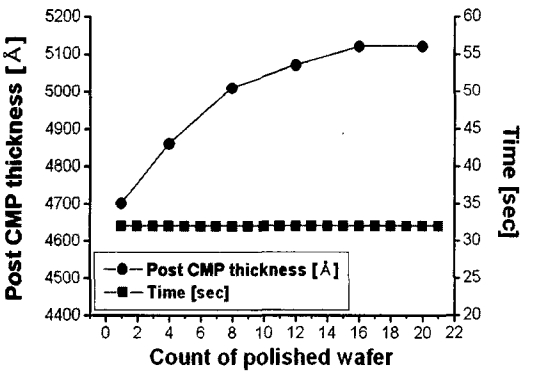


Fig. 6 Wafer-to-wafer thickness variation for the conventional predetermined polishing time method without EPD.

Fig. 6 shows the thickness variation for twenty-one wafers polished for the same predetermined polishing time of 32 sec. The thickness variation measured was within about 420 Å, which implies that the process significantly suffers from wafer-to-wafer thickness variation because the asing of the polishing pad causes a decline in the polishing rate.

4. Conclusions

We have investigated the EPD for the direct CMP of STI structures without the reverse moat pattern step in 0.18 ㎛ semiconductor device fabrication. We have applied a HSS that improves the silicon oxide removal rate and maximizes the oxide-to-nitride selectivity. Quite acceptable and reproducible EPD results were obtained, and the wafer-to-wafer thickness variation was significantly reduced compared with the conventional predetermined polishing time without the EPD method. Therefore, achieving an optimal global planarization was possible without the complicated reverse moat etch process. Furthermore, the problems caused by the nitride residue in the active regions could be reduced by overpolishing SiO_2 since Si_3N_4 was hardly removed. The experiment results, show that the STI-CMP process could be simplified and the defect level could be reduced. Therefore, the throughput, the yield, and the stability in semiconductor device fabrication could be greatly improved.

Acknowledgement

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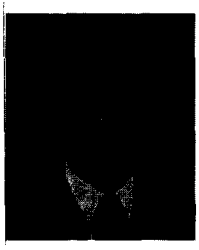
Yong-Jin Seo
He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from Chung-Ang University in 1987, 1989, and 1994, respectively. In 1995, he joined the Department of Electrical Engineering at DAEBUL University, Chonnam-do, Korea. From 1999 to 2000, he was a Post-Doctoral Fellow in the Electrical Engineering Department at the University of North Carolina at Charlotte. He was engaged in the development of a multi-layer nanocrystalline Si-O superlattice diode. Since 2002, he has been an associate professor in the Electrical Engineering Department of DAEBUL University. His research interests are Si-based optoelectronics and optimization of the chemical mechanical polishing (CMP) process for ULSI applications. Tel: +82-61-469-1260, Fax: +82-61-469-1260

Kyoung-Jin Lee
He received his B.S. degree in Electronic Engineering in 2001 and is currently working toward his M.S. degree in Electrical Engineering at DAEBUL University, Chonnam, Korea. His research interests are Si-based optoelectronics and optimization of chemical mechanical polishing (CMP) process for ULSI applications.
Tel: +82-61-469-1260, Fax: +82-61-469-1260

Sang-Yong Kim
He was born in Gwang-ju, Korea, in 1961. He received his Ph.D. degree in Electronic Engineering from Chung-Ang University in 1999. He joined the Hyundai Electronic Semiconductor R&D Center, Icheon Korea, in 1990. From 1990 to 1994, he was involved in CVD and PVD processing. In 1994, he joined the non-memory system I.C. R&D Center. From 1994 to 1996, he worked for Chemical Mechanical Planarization (CMP). He moved to ANAM Semiconductor Co., Buchen, Korea. From 1996 to 2002, he managed several generations of advanced non-memory I.C., 0.25 ㎛, 0.18 ㎛, 0.15 ㎛. His interests in CMP process during this time focused on new process architectures such as APC, CLC, next generation device design rule technologies, and development of new CMP consumable parts. He was engaged in the development of CMP processing of 0.13 ㎛ non-memory I.C. From 1998 to 2001, he became chairman for the Korea CMP user group meeting. Now, he is a technical director in CMP processing and lectures on semiconductors at Chang-Ang University.



Woo-Sun Lee
He received his Ph.D. degree in Electrical Engineering from Chungang University in 1984. From 1989 to 1990, he was a post-doctoral fellow in the Electrical Engineering Department at the University of Purdue. Currently, he is a professor in the Department of Electrical Engineering at Chosun University, Gwangju, Korea. His research interests focus on the chemical mechanical polishing (CMP) process.
Tel: +82-62-230-7024, Fax: +82-62-232-9218