

Accelerated Soft Error Rate Study with Well Structures

Do-Woo Kim*, Myeong-Kook Gong*, and Jin-Suk Wang**

Abstract - The characteristics of accelerated soft error rate (ASER) for fabricated 8M SRAM are evaluated for various well structures. The application of the Buried NWell (BNW) and the variations of each well structure, well dose in process conditions are checked by ASER failure in time (FIT) in terms of reliability. The application of only the BNW shows the lowest ASER FIT value. The BNW added to the Buried PWell (BPW) shows a 200% increase and the BNW plus the Striped BPW (SBPW) shows a 100% increase compared to applying the BNW. The cases of applying SBPW show very high ASER FIT.

Keywords: Soft error rate, FIT, Well, Buried NWell, Buried Pwell

1. Introduction

Recently, as the technology and the density of memory cells advance and require less voltage for operation, accelerated soft error rate (ASER) becomes a topic of interest [1, 2]. As memory densities have increased, cell capacitance has naturally decreased due to the decreasing size of the capacitive elements. Static random access memory (SRAM) cells have tended to allow cell capacitance to drop as the density has increased. ASER measurements have been correlated in the storage node capacitance of cells and various well structures [3, 4, 7].

Soft error, i.e., memory cell failure when the cell is written or read without the physical defects, shows the random bit failure mode in the memory fail bit map. The cause of soft error is α -particle radiated from uranium, thorium, americium, and so forth. This α -particle induces charge up-set by penetrating the cell storage region, and the memory data is lost.

The energy of the α -particle is partly lost passing through the passivation layer of the chip, and it moves on the storage area with 4MeV of energy for a distance of about 25 μ m, generating 10^6 electron hole pair (EHP), which is enough to induce soft error. The α -particle in the epoxy molding compound (EMC) forms an energetic silicon nucleus when it collides with silicon nucleus. With this energy, the EHP that is banded to the silicon nucleus is released as free carriers. The holes disappear due to the recombination in the PWell. Drift and diffusion move the electrons to the cell storage node, which changes the distribution of node charge and voltage and causes the soft error.

Methods for preventing ASER include raising the cell capacitance, making the diffusion, or using the funneling barrier to introduce the third well [5, 6, 9].

2. Experiment

Am-241 is used as a radiation source to measure the ASER of the fabricated 8M SRAM, which has 1.3×10^5 particles/cm²·min. The measurement system is MS3480 and the operation voltage is 2.3V. The write or read data pattern is normal checkerboard and inverse. It is first written to the device under test, and the memory is then read sequentially for a period of time sufficient to reflect the soft error bit fail [2]. The source is placed 7mm above the die surface. The α -particle flux of the EMC is presumed to be 0.005 particles/cm²·hrs. Thus the ASER failure in time (FIT) is calculated as follows.

$$FIT = \frac{0.005 \text{ particles/cm}^2 \cdot \text{hrs} * \text{errors/min} * 10^9 \text{ hrs}}{1.3 * 10^5 \text{ particles/cm}^2 \cdot \text{min}}$$

The schematic diagram of the electrical tester is shown in Fig. 1. Fig. 2 shows each well structure of the memory product applied in this experiment with simple layout. Buried NWell (BNW) is shown in Fig. 2(a), BNW plus Buried PWell (BPW) is shown in Fig. 2(b), BNW plus Striped BPW (SBPW) is shown in Fig. 2(c), and the Striped BNW (SBNW) plus the SBPW is shown in Fig. 2(d).

The BNW and BPW are applied as a junction barrier for free carriers from the substrate, and the memory cell is in the BNW and BPW. The application of the SBNW is used to reduce the PWell resistance relative to the box type BNW. The SBPW is applied to prevent pinch-off by depletion between

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NWell and PWell. Pinch-off can cut off the connection between PWell and the p-substrate. The schematic diagram of the ASER failure mechanism is shown in Fig. 3.

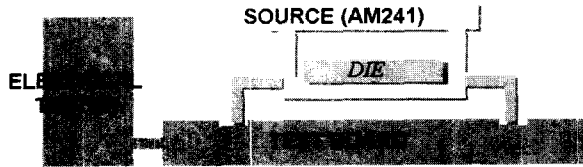


Fig. 1 Schematic diagram of the electrical tester.

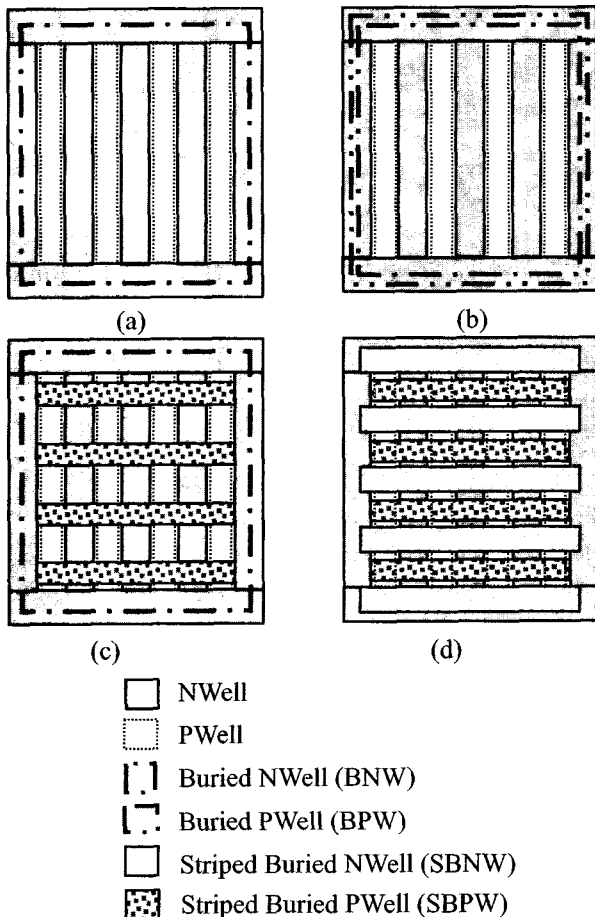


Fig. 2 Layout of Well structures: (a) BNW, (b) BNW + BPW, (c) BNW + SBPW, and (d) SBNW + SBPW.

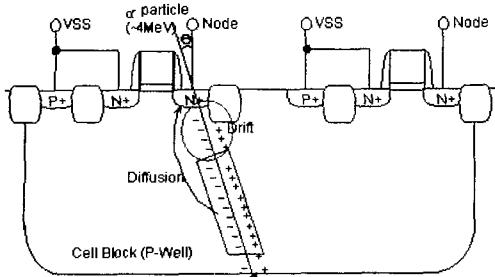
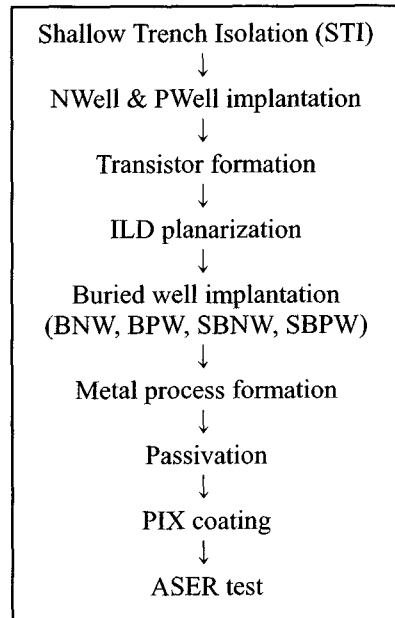


Fig. 3 ASER fail mechanism by energetic α -particle.

3. Results

Figs 4, 5, and 6 show the ASER FIT according to various well structures. The buried well implant processes are applied after the inter-layer dielectric (ILD) process that the transistors are already formed. The process flow sequence of the 8M SRAM is shown in Table 1.

Table 1 Process flow sequence.



In Fig. 4, the ASER FIT values are plotted with the BNW, the BNW plus the BPW, and no buried well [6, 8] in case the plot with no buried well shows the largest ASER FIT value. For the BNW (P, 3E13, 1.8MeV) plus the BPW (B, 3E13, 70KeV), the BPW is blocking the BNW in connection with Vcc power. So ASER FIT shows a small decrease because the generated charges are incompletely extracted from the BNW. In the pure BNW case, the generated charges are completely pulled out to Vcc, so it shows the smallest FIT. The ASER in this pure BNW case occurs due to the generated electron charges in the normal PWell and the holes in the BNW [5, 6].

In Fig. 5, the ASER FIT value of the BNW (P, 3E12, 1.8MeV) plus the SBPW (B, 8E12, 750KeV) well scheme has increased 100% compared to the BNW (P, 3E13, 1.8MeV), and the increase of the SBPW dose (B, 1E13, 750KeV) causes a 10% increase of the ASER. Thus, the SBPW makes the BNW compensate and, hence, degrades the role of the BNW as the barrier for diffused electrons [3]. The decrease of the BNW dose (P, 1.5E12, 1.8MeV) yields a 50% increase of ASER.

Fig. 6 shows the case in which the SBNW (P, 3E12, 1.8MeV) plus the SBPW (B, 3E12, 750KeV) is applied. The ASER is 100% larger than the BNW (P, 3E12,

1.8MeV) plus the SBPW (B, 8E12, 750KeV) case and 300% larger than the BNW (P, 3E13, 1.8MeV) case. This means the NWell area in the SBNW area is three times smaller than the application of the BNW. In addition, applying the SBPW causes a slight increase of the ASER.

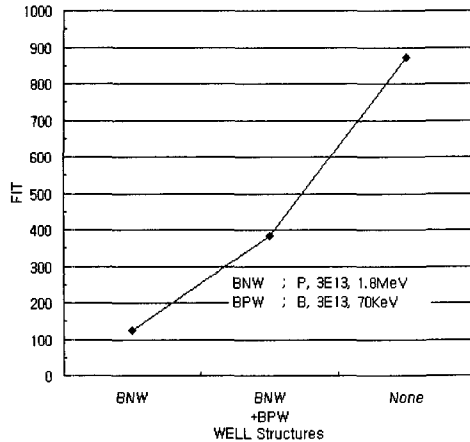


Fig. 4 ASER results comparing the BNW to the BPW.

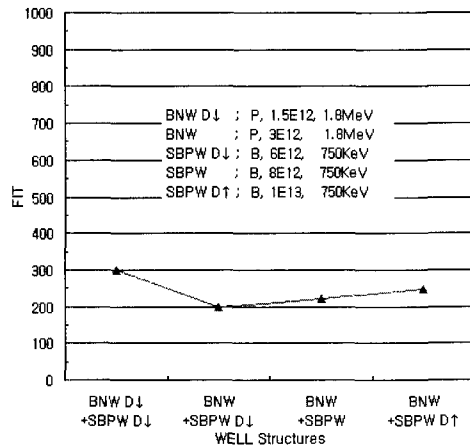


Fig. 5 ASER results comparing the BNW and the SBPW.

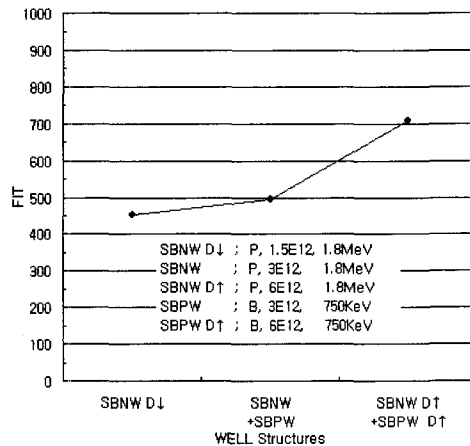


Fig. 6 ASER results comparing the SBNW to the SBPW.

4. Conclusion

We compared and analyzed the ASER for various well structures in the fabricated 8M SRAM. For each well structure applied to this experiment, the application of only the BNW (P, 3E13, 1.8MeV) shows the lowest ASER FIT value. BNW plus BPW shows a 200% increase and BNW plus SBPW shows a 100% increase compared to applying the BNW. The cases in which the SBPW (BNW plus SBPW, SBNW plus SBPW) is applied show very high ASER FIT values.

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