A Study on a Single-Phase Module UPS using a Three-Arm Converter/Inverter

Tae-Geun Koo*, Young-Bok Byun*, Ki-Yeon Joe*, Dong-Hee Kim** and Chul-U Kim***

Abstract - The module UPS can flexibly implement expansion of power system capacities. Furthermore, it can be used to build up the parallel redundant system to improve the reliability of power system operation. To realize the module UPS, load sharing without interconnection among parallel connecting modules as well as a small scale and lightweight topology is necessary. In this paper, the three-arm converter/inverter is compared with the general full-bridge and half-bridge topology from a practical point of view and chosen as the module UPS topology. The switching control approaches based on a pulse width modulation of the converter and inverter of the system are presented independently. The frequency and voltage droop method is applied to parallel operation control to achieve load sharing. Two prototype 3kVA modules are designed and implemented to confirm the effectiveness of the proposed approaches. Experimental results show that the three-arm UPS system has a high power factor, a low distortion of output voltage and input current, and good load sharing characteristics.

Keywords: module UPS, three-arm converter/inverter, droop method, load sharing

1. Introduction

Generally, UPS systems are being widely applied to a variety of critical loads including computers, financial transaction handlers, and life support equipment. Increased dependency of businesses and industry on computers has seen a tremendous increase in the use of UPS systems. However, these UPS systems are inflexible. As the system load grows, the UPS must be replaced with a new, higher capacity one and if the UPS fails, the entire system is affected [1].

The reliability as well as the power capability of the UPS system can be increased by replacing a single UPS unit with multiple small UPS units in parallel, resulting in a so-called module UPS. This module UPS system allows a new module to be added or replaced while maintaining power to a load, i.e. a hot-swappable operation. In addition, it has many desirable features such as ease of output power expandability, convenience of maintenance and repair, and high reliability [2-3].

The technical aspect of the module UPS is a proper load sharing among the parallel connecting modules. The load sharing is very sensitive to discrepancies between compo-

nents of each module, line impedance imbalance, errors of detection, and so on. If no suitable control action is taken, large circulating current among the modules will result. Although many control methods of operating UPS systems in parallel can be found in the literature [3-4], these methods are mainly divided into three categories: the master/slave control, the active current sharing control, and the droop method. All of the control methods have good characteristics of parallel operation and load sharing. The methods of the master/slave control and the active current sharing control need some form of control interconnection among parallel connecting modules. These interconnection wires not only act as a source of noise and failure, but also make it impossible to achieve hot-swappable operation. The droop method based on the frequency and voltage droop concept does not need any interconnection wires. Therefore, this droop method is suitable for the module UPS system.

In our previous work [5], we presented a parallel operation with two prototype three-phase 20kVA UPS systems using the frequency and voltage droop method and showed a balanced load sharing, a fast transient response, and hot-swappable operation. However, to improve the performance of the module UPS system, we must consider its physical size, weight, loss, and cost.

This paper presents a single-phase three-arm converter/inverter that is suitable for a small scale and lightweight module. This system effectiveness is compared with the general full-bridge and half-bridge converter/inverters from a practical point of view. In addition, the switching control approaches based on pulse width modulation of the
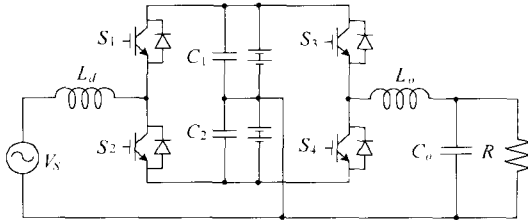
converter and inverter of the three-arm converter/inverter are presented independently. To realize full digital control of the entire control system, we have chosen a single-chip DSP (TMS320LF2407A) from Texas Instruments after a thorough consideration of performance, simplicity in hardware design, and software support. To verify the proposed approach, two prototype 3kVA modules have been designed and implemented and experimental results confirm the effectiveness of the proposed approaches.

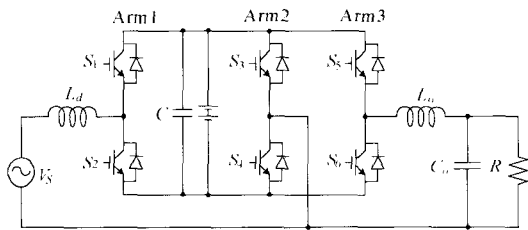## 2. Comparative UPS Topologies

A single-phase UPS system is mainly divided into three topologies [6]: full-bridge converter/inverter, half-bridge converter/inverter, and three-arm converter/inverter. Each circuit is shown in Fig.1.
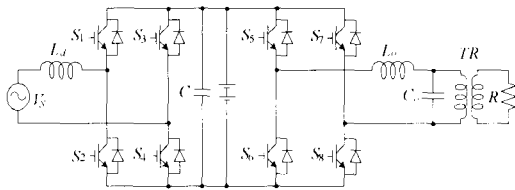
(a) Configuration of a full-bridge converter/inverter.

(b) Configuration of a half-bridge converter/inverter.

(c) Configuration of a three-arm converter/inverter.

Fig. 1 Single-phase UPS topologies.

The purpose of each UPS topology's converter/inverter operation is similar. The input AC source V_s is converted into a stable DC voltage by the converter with a unity power factor and the input current tracks a sinusoidal waveform. The inverter converts the DC voltage into a constant frequency single-phase sinusoidal waveform to supply a stable power to the loads. If an input ac source failure occurs, the DC power delivered from the energy storage battery is converted into high-quality single-phase

AC power by using the inverter to supply continuous AC power into the loads.

Fig. 1(a) shows a full-bridge converter/inverter configuration with a low frequency transformer. This topology is widely used in single-phase AC power supplies. Schemes using a diode bridge in cascade with a full-bridge inverter are simple and inexpensive. However, to correct the input current waveform, a full-bridge transistor can be used to replace the diode bridge. The isolation transformer TR is equipped at the output power side. If no isolation transformer exists, a short circuit through the commercial bypass line will occurs, resulting in significant damage to the UPS system. The volumetric size and weight of this topology are extremely large because the transformer operates at the commercial power frequency.

Fig. 1(b) shows a half-bridge converter/inverter configuration. Compared with the full-bridge topology with an isolation transformer, the half-bridge UPS offers several advantages, including no isolation transformer and a simple power conversion circuit with possibly the lowest switching device count of all such cirduits. However, it must be noted that the DC link voltage is twice that of the other topologies. Consequently, this half-bridge topology necessitates connecting a great number of the battery cells in series. This requirement of a high voltage storage battery leads to increased cost and reduced reliability since, for a given storage capacity, the cost rises but the reliability decreases as the number of storage batteries increases [7].

Fig. 1(c) shows a three-arm converter/inverter. Arms 1 and 2 operate as a PWM converter, and Arms 2 and 3 operate as a PWM inverter. This topology has a common bus line between input and output ports like the half-bridge topology. So this topology makes it possible to remove the isolation transformer and to reduce the physical size and weight of the system. In addition, although this topology can save one converter arm, the converter can process the same power capacity as the full-bridge topology. That is to say, the DC link voltage level requirement is the same as with the full-bridge topology. Thus, switching and conduction losses are reduced by approximately one quarter. In comparison with the half-bridge and the full-bridge topologies, the three-arm converter/inverter is suitable for the module UPS because it is small, compact, lightweight, and high efficiency.

3. Operation Analysis

3.1 Converter Operation Modes with Power-Factor Correction (PFC) Control

The operation of the converter of the three-arm converter/inverter is the same as a single-phase boost converter.

A PFC control block diagram of the converter is shown in Fig. 2 where v_s is the input voltage, i_s is the input current, i_s^* is the input current reference, V_{dc} is the DC link voltage, V_{dc}^* is the DC link voltage reference, P_o is output active power, L_d is the boost reactor, and C is the DC link capacitor.

In this paper, a multi-loop control scheme for the PFC is adopted because of its constant switching frequency and easy implementation. The control scheme consists of two parts: the inner current loop and the outer dc voltage loop.

As shown in Fig. 2, the operation of the outer loop controller is described as follows. The DC output voltage V_{dc} is compared with the reference voltage V_{dc}^*. $P_o \cdot k_p$, which is the instantaneous output power term, is added to the error signal V_{err}, and the result is multiplied by the absolute value $|v_{pll}|$, synchronized to the input voltage to produce the reference value i_s^* for the inner current loop. The operation of the inner loop controller is as follows.
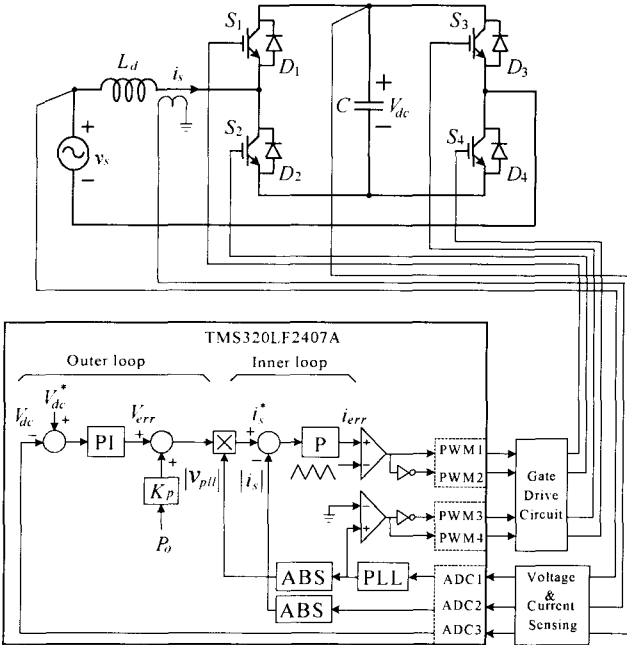

Fig. 2 PFC control block diagram of the converter.

The signal i_s^* is compared with the absolute value $|i_s|$ of the input current. Its error signal i_{err} is processed by a triangular wave of 20kHz to obtain PWMs 1 and 2 of the switches S_1 and S_2, respectively.

Since the transient response of the PFC is determined by the inner current loop, its response time has to be fast enough to closely follow the current reference. However, the response time of the DC voltage loop is slower than the current loop response. The outer loop controller commonly employs a proportional-integral (PI) control since it con-

tributes to zero steady state error for the DC voltage, and the inner loop controller is a proportional (P) controller. The current tracking response is improved by selecting a large proportional gain. If the gain is too small, then the input current i_s will stray from the current reference i_s^*.

When the input voltage v_s is positive, only the PWM 4 is high, and when v_s is negative, only the PWM 3 is high. In such a control implementation, the current in the boost inductor L_d is regulated by the PWM control of the boost converter to obtain a sinusoidal input current while maintaining a constant voltage across the DC link capacitor.

The circuit operation of the converter is divided into four states. For positive input voltage v_s and if switch S_2 is turned on, the input current flows along a path of v_s, L_d, S_2, D_4, and back to v_s, and energy is stored in the boost inductor L_d. The differential equation of the input current i_s is defined as

$$\frac{di_s}{dt} = \frac{v_s}{L_d}. \tag{1}$$

Then turning off switch S_2 changes the current path, and the energy of AC line and the stored energy of the boost inductor L_d transfer to the DC link line. The input current flows along a path of v_s, L_d, D_1, V_{dc}, D_4, and back to v_s. The differential equation of input current i_s is defined as

$$\frac{di_s}{dt} = \frac{V_s - V_{dc}}{L_d}. \tag{2}$$

Similarly, for negative v_s, two other operational modes can be established by the control of switch S_1.

3.2 Inverter Control and Operational Modes

The inverter is composed of arms 2 and 3. The basic function of the inverter is to convert the DC voltage to a pure sinusoidal waveform at its output port. A control block diagram of the inverter is shown in Fig. 3 where V_{dc} is the DC link voltage, i_f is the input current of the output filters, i_c is the capacitor current, i_L is the load current, V_o is the output voltage, V_o^* is the output voltage reference, C is the DC link capacitor, and L_o and C_o are the output filters.

In the circuit shown in Fig.3, the output voltage V_o is compared with the reference voltage V_o^* and its error signal V_{err} is multiplied by the signal v_{pll}, synchronized to the input voltage to produce the instantaneous fundamental signal v_{s1}. The signal v_{s1} is added to a square-wave to easily design the switching pattern of arm 3 [8]. The signal V_{s2} is processed by the triangular wave of 20 kHz to obtain PWMs 5 and 6 of the switching devices S_5 and S_6, respectively.
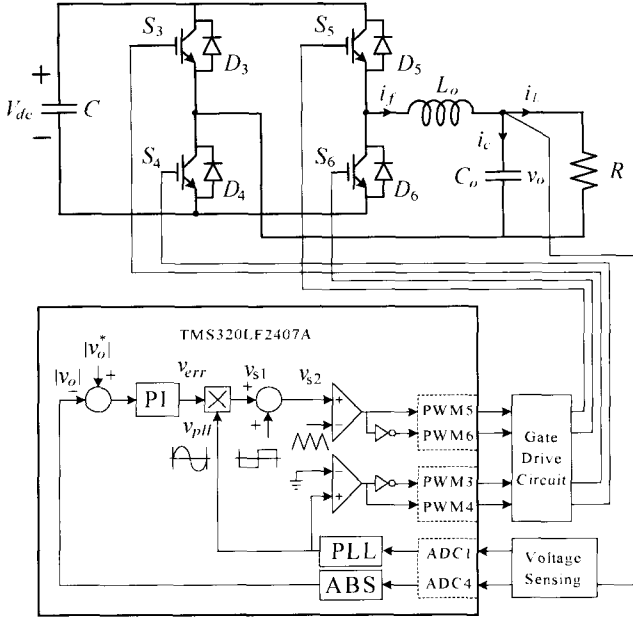
Fig. 3 Control block diagram of the inverter.

The circuit operation of the inverter is divided into four states. For positive output voltage v_o and if switches S_4 and S_5 are turned on, the current i_f flows in a path of V_{dc}, S_5, L_o, $C_o//R$, S_4, and back to V_{dc}. The differential equation of the current i_f and the output voltage V_o are defined as

$$\frac{di_f}{dt} = \frac{V_{dc} - v_o}{L_o} \tag{3}$$

$$\frac{dv_o}{dt} = \frac{i_f - i_l}{c_o}. \tag{4}$$

Then switch S_4 is still turned on, and if switch S_5 is turned off and switch S_6 is turned on, the current i_f flows in a path of L_o, $C_o//R$, S_4, D_6, and L_o. The output voltage V_o is regulated with low total harmonic distortion (THD) sinusoidal waveform.

Similar operation can be derived for negative output voltage with switches S_3 and S_6.

4. Parallel Operation Control Algorithm

Generally, the technical purpose of the parallel connected modules is to achieve balanced load sharing. Most of the control methods need interconnections among modules to get information, such as output current and frequency, from other modules. These methods are not suitable for the module UPS system. However, the droop method based on the frequency and voltage droop concept needs no control interconnections [1-4].

In this paper, this droop method, using the output frequency and voltage droops as function of the active and reactive powers respectively, is adopted. Each module measures only signals of output voltage and its own output current, no connective bus or other signals are needed. The block diagram of the frequency and voltage droop method is shown in Fig. 4.
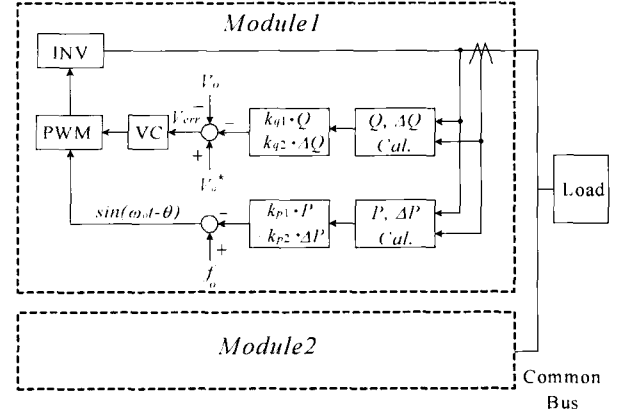

Fig. 4 Block diagram of the frequency and voltage droop method.

The control algorithm of the reactive power is

$$V'_{or} = V'_o - V'_o - K_{q1} \cdot Q - K_{q2} \cdot \Delta Q \tag{5}$$

where Q is the reactive power, ΔQ represents the reactive power difference between two continuous sampling times, and K_{q1} and K_{q2} are reactive power coefficients.

In Eq. (5), we can derive that the magnitude of the output voltage reference V_o^* droops in proportion to Q, and ΔQ. The reactive power sharing is controlled by the difference of the output voltage reference between the paralleled modules. The $K_{q2} \cdot \Delta Q$ term in Eq. (5) minimizes the output current fluctuation during hot-swap operation and abtains a fast transient response.

The droop method is simple to implement. However, in this case, a trade-off must be made between the accuracy of reactive power sharing and the output voltage quality. If the reactive power coefficients are high, the accuracy of reactive power sharing improves but the output voltage variation range is increased.

The control algorithm of the active power is

$$f_o = f_{o-1} - K_{p1} \cdot P - K_{p2} \cdot \Delta P \tag{6}$$

where P is the active power, ΔP represents the active power difference between two continuous sampling times,

f_n is the reference frequency of the inverter, and K_{p1} and K_{p2} are the active power coefficients.

Generally, the frequency difference creates the phase difference. In Eq. (6), we can derive that the reference frequency droops in proportion to P and ΔP. The active power sharing can be controlled by slightly varying the phase of output voltage phase from that of the bypass voltage and by making a trade-off between accuracy of active power sharing and phase synchronization.

5. Simulation

To verify the performance of the proposed control algorithm, a simulation was executed using the PSIM package program. The parameters for the simulations are as follows: the input and output voltages are 220V, the DC link voltage is 400V, the frequency of the switching device is 20kHz, the DC link capacitor is 2200 μ F, the reactance of the boost inductor is 0.5mH, and LC filters consist of reactance rating 0.5mH and capacitor rating 50 μ F.

Fig. 5 shows the transient and steady state operation characteristics of one UPS unit. From Fig. 5, the waveform of the input current is observed to be controlled so as to be sinusoidal and in phase with the input voltage.

To prove the validity of the parallel control algorithm based on the frequency and voltage droop, two parallel connecting UPS modules are composed with different line impedance: $Z_1 = 0.001 + j0.037\Omega$, $Z_2 = 0.002 + j0.075\Omega$.

Fig. 6 shows the simulation results of active powers and reactive powers of two UPS systems before and after the parallel control algorithm application. The parallel control algorithm is applied at 0.15sec. Before 0.15sec, the power differences of two modules were increasing. But after
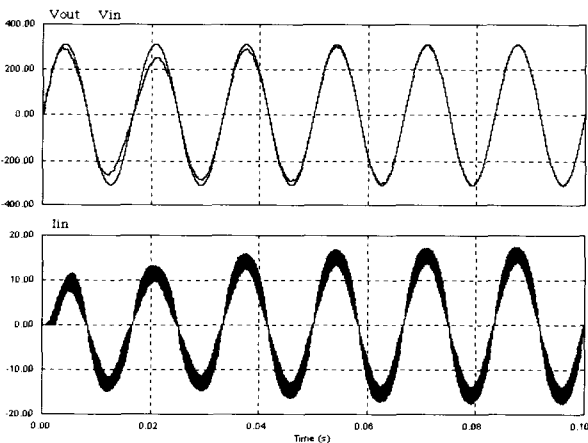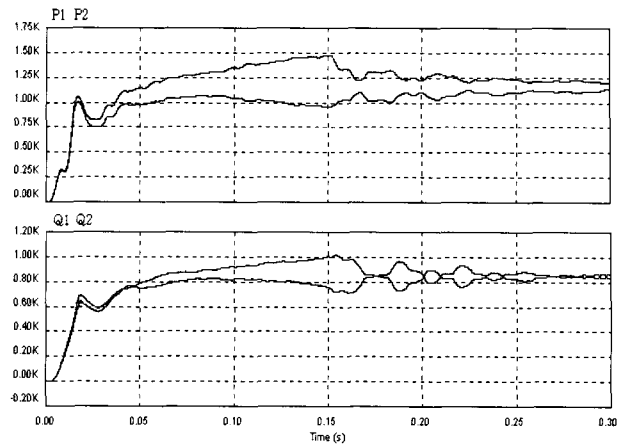

Fig. 6 Simulation results of the power sharing (upper traces are active powers and lower traces are reactive powers).

0.15sec, the differences were decreasing. This Fig. shows that the proposed control algorithm can control the active and reactive power sharing.

6. Experimental Verification

Two prototype modules have been constructed and used for experimentation. Each module's capacity is 3kVA. Before parallel operation of the module UPS system, the basic operations of one module are tested.

Fig. 7 shows the steady state performance of the input voltage and the input current waveforms with 25Ω load. It confirms that the PFC control can draw high power factor input current with low current harmonics. The input PF and the THD of the input current are 0.993 and 11.5%, respectively. The output voltage shows good regulation with low THD, 3.0%, sinusoidal waveform during steady state in Fig. 8.

Fig. 5 Simulation waveforms (upper traces are input voltage and output voltage and lower trace is input current).
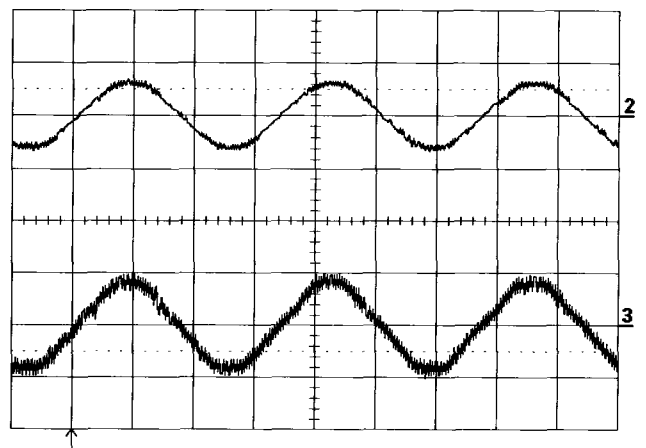
(500V/div, 20A/div, 5ms/div)

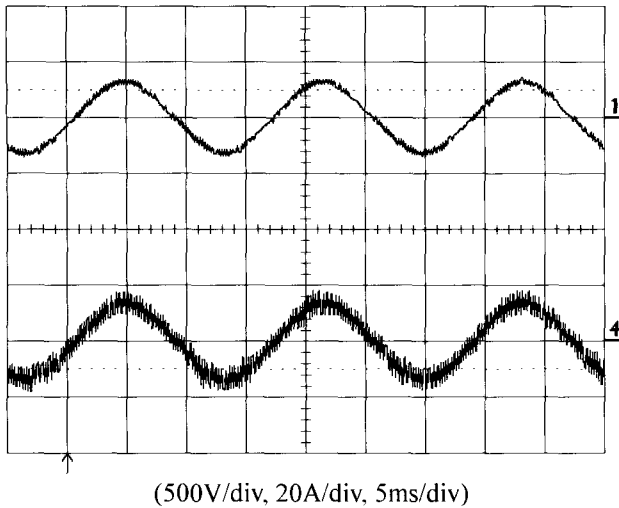**Fig. 7** Experimental results when the load is 25Ω (upper trace is input voltage and lower trace is input current).

(500V/div, 20A/div, 5ms/div)

Fig. 8 Experimental results when the load is 25Ω (upper trace is output voltage and lower trace is output current).
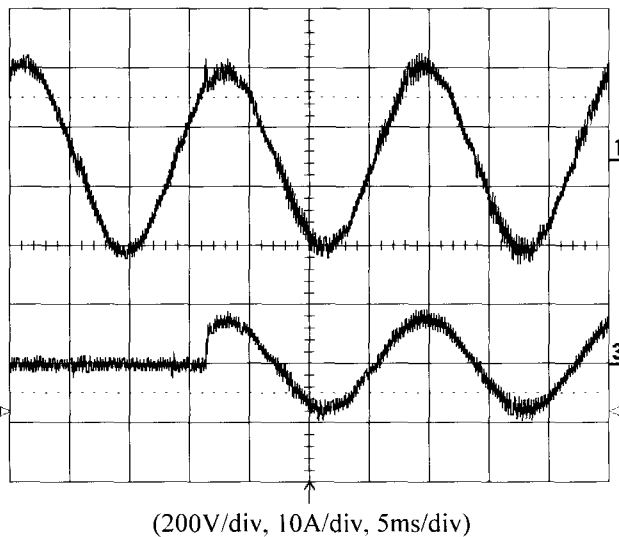

(200V/div, 10A/div, 5ms/div)

Fig. 9 Experimental results when the step load is changed (upper trace is output voltage and lower trace is output current).

Fig. 9 shows the transient performance of the output voltage and the output current under a step load change. The output voltage of the UPS module maintains a stable voltage and frequency with undistorted waveform at a sudden change of the load.

To verify the performance of the parallel operation control algorithm, two modules are connected in parallel. Each module is controlled by the frequency and voltage droop method to share the total load current equally.

Fig. 10 shows the waveforms of the output voltage, the load current, and the output currents of the two modules under a resistive load 40Ω and a reactive load 30Ω. As seen from Fig. 8, the output current differences in wave-

form are quite small. So we know that the load sharing between the two modules is stable and equal. The load sharing error is within 3%.

Fig. 11 shows the waveforms of the output voltage, the load current, and the output currents of the two modules when the R-L load is connected. Fig. 9 illustrates a fast transient response and good load sharing.

Therefore, the results of the experiment show that the three-arm converter/inverter has a high power factor, low distortion of output voltage and input current, and good load sharing characteristics.
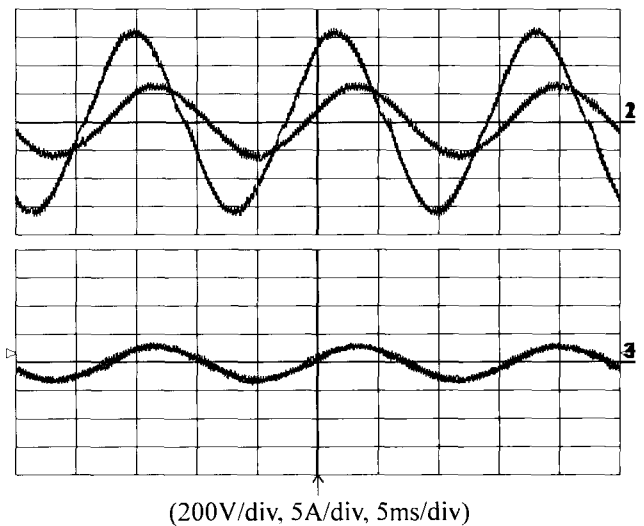

(200V/div, 5A/div, 5ms/div)

Fig. 10 Experimental results during parallel operation (upper traces are output voltage and load current and lower traces are output currents of paralleled modules).
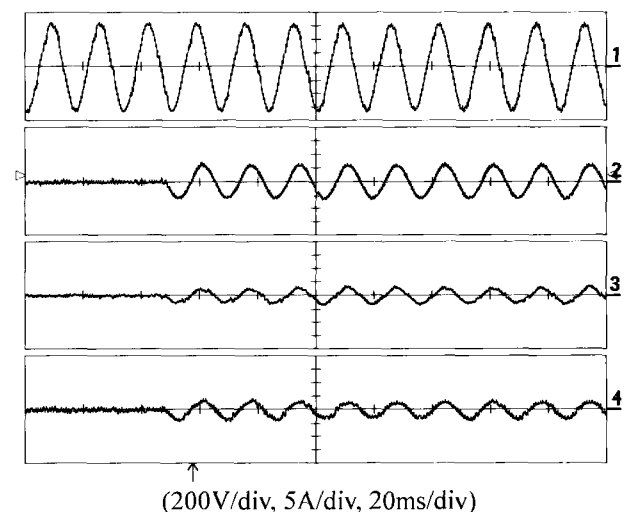

(200V/div, 5A/div, 20ms/div)

Fig. 11 Experimental results when RL load is connected (upper traces are output voltage and load current and lower traces are output currents of paralleled modules).

7. Conclusions

In this paper, a single-phase three-arm converter/inverter for a compact small scale module UPS system has been presented. The three-arm converter/inverter has been compared with the full-bridge and half-bridge topologies from a practical point of view, and the switching control approaches of the converter and the inverter has been described separately. The three-arm converter/inverter has been proven achieve some remarkable electrical performance while exhibiting a small physical size, lighter weight, high power factor, low distortion, and good load sharing.

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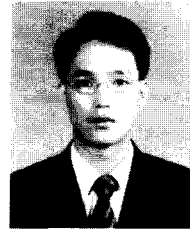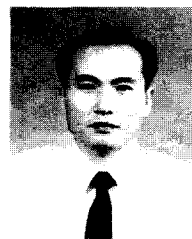
Tae-Geun Koo

He was born in Korea, on Jan. 27, 1970. He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from Yeungnam University, Kyungsan, Korea, in 1995, 1997, and 2002, respectively. He is currently an assistant researcher in the Power Electronics Group at Korea Electro-technology Research institute (KERI). His current research interests include UPS parallel operation and DSP application on power conversion systems. He is currently a member of the KIEE.

Young-Bok Byun

He was born in Pusan, Korea, on Mar. 23, 1961. He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from Pusan National University, Pusan, Korea, in 1984, 1986, and 1998, respectively. Since 1986, he has been with the Power Electronics Group at Korea Electro-technology Research Institute (KERI). His major interests are UPS and DSP application on power conversion systems. He is currently a member of the KIEE and the KIPE.

Ki-Yeon Joe

He was born in Korea, on Feb. 5, 1954. He received his B.S., M.S. and Ph.D. degrees in Electrical Engineering from Yeungnam University , Kyungsan, Korea, in 1980, 1982, and 1991, respectively. He is currently a Principal Research Engineer in the Power Electronics Group at Korea Electro-technology Research Institute (KERI). His current research interests include ultra high frequency energy conversion, digital and small control systems, and diagnostic techniques of power electronics equipment. He is currently a member of the KIEE and the KIPE.

Dong-Hee Kim
He was born in Korea, on Nov. 20, 1950. He received his B.S. and M.S. degrees in Electrical Engineering from Yeungnam University, Kyungsan, Korea in 1973 and 1975, respectively, and his Ph.D. degree in Electrical Engineering from Kobe University, Japan, in 1987. He is currently a professor in the School of Electrical and Electronic Engineering at Yeungnam University. His current research interests are high frequency resonant inverters and induction heating application systems. He is currently a member of the KIEE and the KIPE.

Cheul-U Kim
He was born in Tong- young, Kyung-Nam, Korea, in 1942. He received the B.S. degree in Electrical Engineering from Pusan National University, Pusan, Korea, in 1969, the M.S. degree from the University of Electro-Communication, Japan, in 1974, and the Ph.D. degree from Chung-Ang University, Korea, in 1986. Since 1975, he has been a professor at Pusan National University, Pusan, Korea. His research activities are in the areas of power electronics and motor control, including cyclo-converter design, drive systems, and high efficiency switch mode power supplies. He is a member of the Korea Institute of Electrical Engineering, Korea Institute of Power Electronics, Korea Institute of Illuminating and Electrical Installation Engineers, Japan Institute of Electrical Engineers, and the Institute of Electrical and Electronics Engineers.