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Optical Interconnection and Clocking
Using Planar-Integrated Free-Space Optics

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Integration and miniaturization at the systems level are key requirements for photonics applications. Here, we describe the concept of planar integration of free-space optical systems and its use as an optical interconnection technology. Two specific applications will be considered, a parallel chip-to-chip interconnect and an optical clock distribution network.

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I. INTRODUCTION

Optical interconnections are of interest at all levels in digital computers for communicating between boards, chips, and on a single chip [1,2]. They are in principle well suited for these applications because of their large temporal and spatial bandwidth, low signal crosstalk, immunity against electromagnetic influence, and low power consumption. The communications problems of electronic computing are due to a large extent to the mismatch between processing power and communications capabilities. This, in turn, is largely a cause of the 2-D nature of wired interconnections. Thus, for certain areas in the interconnection hierarchy like at the chip-to-chip level, the use of the third dimension offered by free-space optics is of interest [3].

A particular interconnection task is clock distribution, where high-speed signals are distributed over large distances. The clocking frequency of microprocessors will increase to 10 GHz in the next few years. Improvements in fabrication technology (smaller feature size, larger chip areas) tend to improve the performance of the processors. However, smaller features and larger distances pose problems to electronic communication due to increasing resistance of wires and higher loads. This is true in particular for the clock distribution network. The problem is further increased for multiprocessor systems where inter-chip distribution is used. In a multiprocessor system, the transmission distances may increase up to 100 mm and more. Power dissipation is another issue that starts to plague electrical clocking. For a current processor

chip, about half of the total power is dissipated just by the clocking network. To reduce these problems several techniques have been developed like placing distributed repeaters within the clock network, using symmetric distribution networks (H-tree structures) to minimized the clock skew, or use of an optimum clock skewing strategy that allows the circuit to run globally faster (clock skew scheduling). To solve the problem at the bottom, however, the use of optical clocking with the advantages mentioned above may become a viable solution [4,5].

In this article, we want to review the concept of planar integrated free-space optics (section II), describe its use as an interconnection technology (section III) and discuss its application to optical clocking (section IV).

II. PLANAR INTEGRATION OF FREE-SPACE OPTICS

Miniaturization and integration at the module and systems level are two of the key requirements for any photonics application. Thus, integration and packaging concepts for waveguide [6] and free-space optics [7-9] have gained considerable importance during the past years. First, we want to review the concept of planar integrated free-space optics, here briefly called P-IFSO.

A schematic drawing of a P-IFSO system is shown in Fig. 1. The concept is to fold a 3-D setup into a 2-D geometry. Thus we have physically the 3-D properties and can use 2-D lithographic batch processing
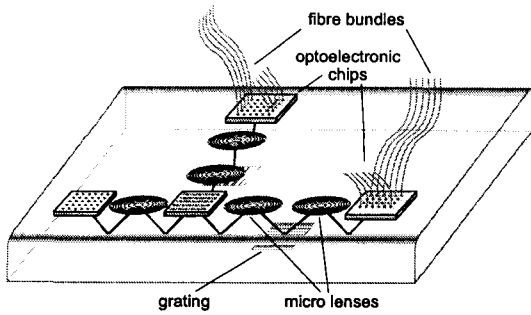
FIG. 1. Planar integrated free-space optics: light propages inside a transparent substrate. Microoptic elements are placed at well-defined positions to control the flow of light. The substrate is several millimeters thick and serves as a medium for the light propagation and as an open platform for the hybrid integration of input/output devices.

or replication. In P-IFSO, microoptical elements (diffractive, refractive, reflective) are monolithically integrated on one or both surfaces of a transparent slab (glass, plastic, semiconductor, ...) at well-defined positions. Light propagates inside the substrate along a tilted optical axis. The substrate serves as medium for the light propagation and as an open platform for input/output devices (emitters, detectors, modulators, fiber bundles, ...). The design of P-IFSO includes a combination of optical, thermal and electrical aspects. Various applications have been considered, for example, in the areas of interconnection [10-12], sensing [13] and imaging [14,15].

In the following section, we will present recent work on optical interconnection on the chip-to-chip level.

III. SYSTEM DEMONSTRATION

A particular advantage of free-space optics over guided-wave optics is the ability to realize highly compact and topologically complex interconnection schemes with comparatively simple hardware. To demonstrate this in practice we designed and constructed an optoelectronic multi-chip module that implements a vector-matrix-type interconnection scheme [16,17]. Such devices are of fundamental importance for communication networks since the vector-matrix-topology is generic for optical cross-connect switches which play a key role in optical routers.

The schematic architecture of our multi-chip module is shown in Fig. 2. Vector-matrix-type interconnects involve an optical fan-out stage followed by an optical fan-in stage; these two stages are implemented along the x-axis. A second optical fan-out stage along the y-axis can be used to program the central 2-D modulator chip optically. 1-D arrays of vertical-cavity surface emitting lasers (VCSEL)serve as signal sources
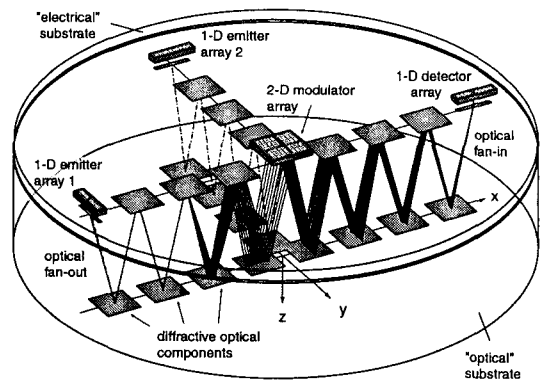

FIG. 2. Schematic of a P-IFSO vector-matrix module.

in our module, for detection a CCD camera was used. All optoelectronic chips as well as the electrical lines for power and data supply (not shown in Fig. 2) are integrated on a 0.5 mm thin substrate, termed "electrical". All the free-space optical components are integrated on a second 9 mm thick substrate, termed "optical".

Optical components were realized as phase-only surface-relief diffractive optical elements (DOE) and fabricated using multiple binary lithography and reactive ion etching. Reflective coatings are realized with athin layer of evaporated aluminum. Lithography in connection with a lift-off process was also used to realize the electrical lines on the "electrical" substrate.
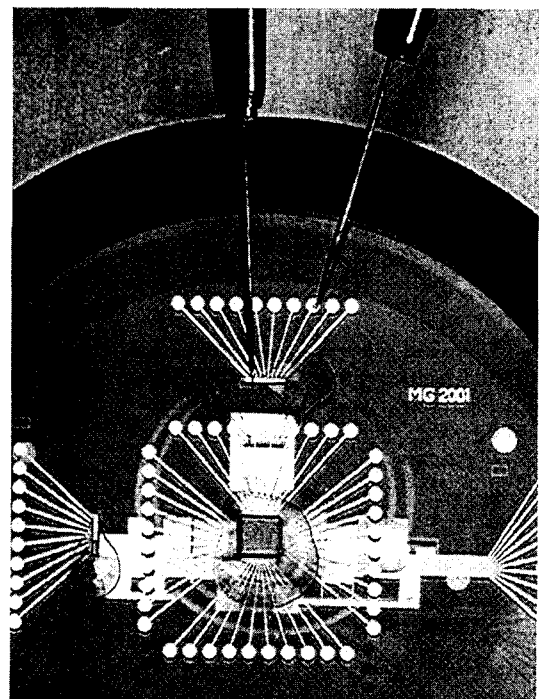

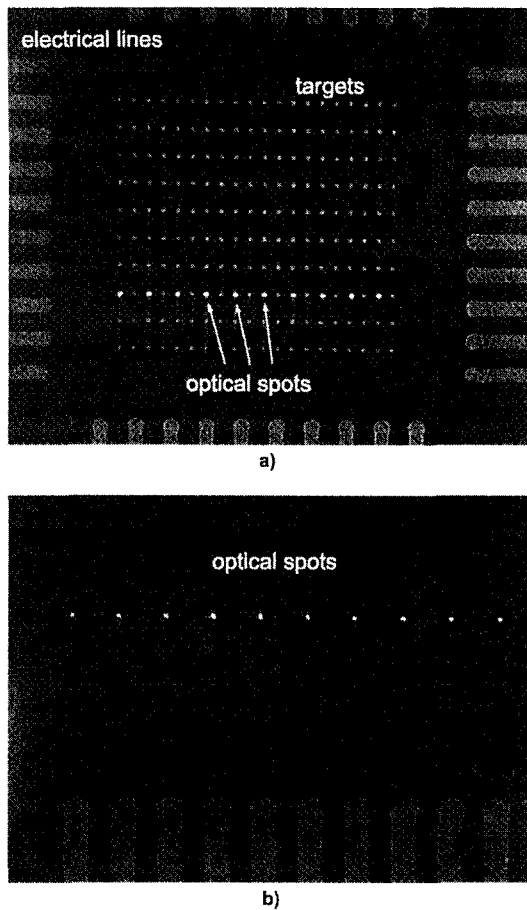FIG. 3. Electrical probing of the experimental vector-matrix demonstrator.

FIG. 4. Experimental results: (a) optical fan-out (b) optical fan-in.

The optoelectronic chips were then flip-chip bonded onto their respective positions. Finally the "optical" and the "electrical" substrate were aligned to each other. Fig. 3 shows the finished experimental demonstrator in an experiment where the basic functionality was tested by addressing individual VCSELs with electrical probe needles.

In these tests it was verified that all VCSELs could be electrically addressed and that the optical fan-out and fan-in worked as planned. Fig. 4(a) shows the view with a CCD camera onto the 2-D modulator array. One can recognize the 20 × 10 target areas which have a size of 20 μm × 20 μm, surrounded by the electrical lines. The 10 bright spots that are generated by the optical fan-out system obviously hit their respective targets almost perfectly. It was found that the spot diameter is 10.1 μm FWHM and thus narrow enough to ensure low intensity loss. Fig. 4(b) shows the view with a CCD camera onto the output area. Here one can recognize 10 spots that result from the optical fan-in.

The experimental demonstrator of Fig. 3 thus proves the feasibility of the P-IFSO interconnection approach and its compatibility with established standards of electronic VLSI integration.

IV. OPTICAL CLOCKING

Clock distribution has been identified as an interesting application for optical interconnection [1]. In [18], a free-space optical clock distribution system was suggested. In order to present a practical solution, a tolerantly designed system was described in [19]. The special purpose of a tolerant design is the requirement to accept large tolerances of the fabrication parameters (material and accuracy) and operating parameters (wavelength and temperature). This leads to a better performance and a cheaper fabrication.

The following sections address the following topics: In section IV 1, the planar integrated clock distribution system and the tolerant design of such a system are briefly described. In IV 2, we present the relevant equations for the simulation of the system and present experimental results in section IV 3. In the following section the tolerances of the correction system and their influence on the light distribution are analysed. At last a short conclusion with additional thoughts about further applications for an optical clock distribution system is given.

1. Integrated clock distribution

Fig. 5(a) explains the basic idea of a planar optical distribution system designed for a multi-chip application. In order to generate a large fanout and achieve a large separation of the output beams a cascade of 1 × 2 beam splitters is used. The modulated input beam carrying the clock signal enters the substrate through an AR-coated window and is split up into two beams by a beam splitter grating, BS. Highly reflective mirrors are used to keep the light bouncing inside the subtrate. The output beams travel along a zigzag path, get redirected by a beam deflector, BD, and are then split up again to yield four output beams overall. Beam splitter and beam deflection gratings are implemented as high frequency phase gratings [18, 20]. The light path can be calculated by simple geometric calculations, so that the position of the optical elements and the output windows on the surfaces is well defined. At these output positions the chips of a multiprocessor system are mounted. Integrated CMOS detectors convert the optical signals into electrical clock signals. A larger fanout than 1 × 4 is achieved by adding more stages to the cascade (Fig. 5(b)). The maximum fanout depends on geometrical parameters and, in particular, also on the power budget [18].
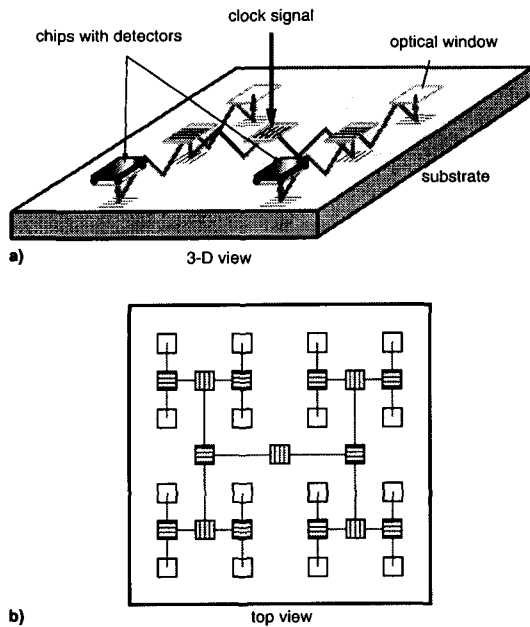
a)   **3-D view**

b)   **top view**

FIG. 5. Integrated planar-optical fanout system for multi-chip clock distribution. (a) Basic 1 × 4 stage. (b) Top view of an H-tree based on cascading multiple 1 × 4 stages.

Several effects influence the path of the light beam travelling inside the substrate and can cause a lateral and/or angular offset Δs of the beam. An offset may result in an intensity loss. This, in turn, leads to a skew of the detected electrical signal and hence to a nonuniformity of the clock signals at the various output positions. In the worst case the light beam does not hit the detector area at all. To minimize this influence and to stabilize the light propagation a tolerant design of the clock distribution system was developed. For this design the concept of a confocal laser resonator (lens waveguide) is adapted to the clock distribution system by placing a series of lenses in the path of the light beam at positions $s = 2mh \tan\theta$ where m is an integer number. The identical lenses are separated along the light propagation direction by a distance F that essentially equals the focal length of the lenses (Fig. 6). F depends on the substrate thickness h and the propagation angle θ through the
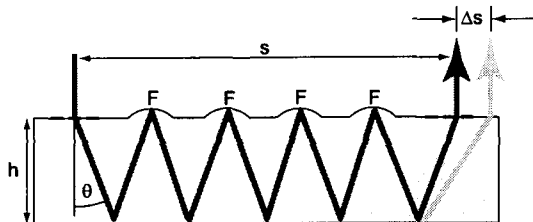

FIG. 6. Lens correction system to stabilize the light propagation. By chosing the focal lengths suitably to be $2h \cos\theta$, the lenses act as a sequence of field lenses.

equation $F = 2h (\cos\theta)^{-1}$. In the ideal case of no offset the lenses have no influence to the beam path through the substrate. In the other case of a lateral or angular offset the lens action tends to "pull back" the light beam towards its ideal path. In the following, we refer to the lenses as the "correction system."

2. Simulation and experiments

The effect of the correction system was analyzed by simulation and by experiment. Ray tracing was used for the simulations. The situation is depicted in Fig. 6. The input beam is simulated by a 2-D array of $N \times N$ parallel input rays. The purpose of the simulation is to calculate the lateral center position s of the beam as it propagates through the substrate. s is given as the average of the individual positions of the different rays. The lateral offset Δs is the difference between the calculated position s and the ideal output position sideal. The ideal output position is easily derived from simple trigonometric relations. After one double pass, the lateral propagation distance is given as $s_{ideal} = 2h \tan\theta$. Variations of the substrate thickness, the propagation angle due to a wedge between the substrate surfaces, the temperature, and the wavelength affect the light propagation. For the simulations the following values were assigned to these four types of variations.

$\Delta h = \pm 25\,\mu\text{m}$ substrate thickness
$\Delta\alpha = \pm 1'$ substrate wedge
$\Delta T = \pm 100\,^\circ\text{C}$ temperature
$\Delta l = \pm 10\,\text{nm}$ wavelength

In the ideal case, all four parameters are zero. It turns out that the strongest influence is due to the variation of the wedge between the substrate surfaces (Fig. 7(a)). Even small values of $\Delta\alpha$ can lead to large offsets Δs, since the error grows quadratically with the number of reflections.

The experiments were carried out using the setup shown in Fig. 7. Two glass substrates, each with a one-dimensional array of reflective lenslets are placed face to face at a distance h. The surfaces are coated with a reflective layer (Al). A laser beam enters the region between the two mirror surfaces under an angle θ, is repeatedly reflected and propagates in the same manner as in the substrate of a planar optical system. So the region between the substrates can be seen as a "virtual" substrate. The parameter h and the wedge angle $\Delta\alpha$ between the surfaces can be varied continuously. Behind the last lens a CCD camera monitors the position of the output beam.

The lens array consists of twelve lenses with elliptic symmetry. The elliptical phase profile is chosen in or-
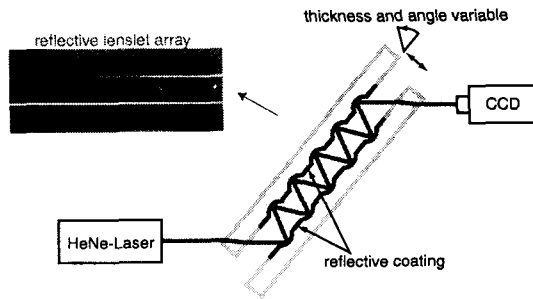
FIG. 7. Experimental setup for testing the performance of the tolerant system.

der to adapt the lens performance to the tilted optical axis [21]. As a consequence the focal length in y differs slightly from that in x, in our case $f_y = 2.3\,$mm vs. $f_x = 2.5\,$mm. The lenses have a diameter of 949 mm in y-direction and 1000 mm in x-direction, the distance h between the substrates was 1.8 mm, and the angle $\theta = 35°57'$ (Fig. 7).

The diagram in Fig. 8 presents the measured values of the lateral offset Δs as a function of the wedge angle $\Delta\alpha$ which was varied in the range of $-7' \leq \Delta\alpha \leq 7'$. These values are compared with the ray tracing simulations for a system with and without correction lenses. For the given values, the lateral offset in the position of the output beam was 3 mm. Such a large offset would certainly result in a total loss of the output signal. For the corrected system, the values for the measured and the calculated offset were smaller than 100 μm. This is a considerable improvement even though the tolerances were chosen to be rather large. For comparison, it might be useful to say that commercial substrates usually have wedge errors of $\Delta\alpha \leq 1'$.
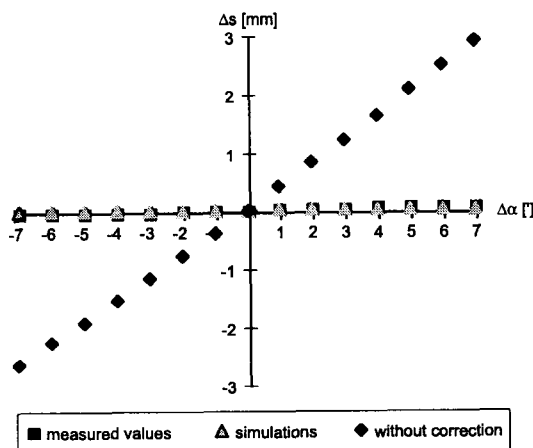
3. Tolerances of the correction system

As demonstrated in the previous section, the lateral and directional stability of the beam can be increased significantly by using a "tolerantly designed" optical system consisting of a series of lenses with a suitable focal length. The "lens waveguide" has the property that it keeps the direction and position of the light beam within certain tolerance intervals even for large lateral propagation distances s. An interesting situation occurs when the parameters of the "control system", i.e., the focal lengths and shape of the lenses, become uncertain themselves. This is the case, in particular, if the lenses are fabricated by an analog fabrication process. An example are reflective lenslets manufactured by melting photoresist (see, for example [22]). In this case, the thickness of the resist layer determines the focal length of the resulting lens. Due to variations of the photoresist's chemistry and fabrication tolerances, the phase profile of the resulting lenses may vary. This may result in tolerances of the focal length (of up to several percent) and in wavefront aberrations. In addition, the substrate surface itself may be irregular. The influence of these effects was also calculated by ray tracing simulations. Fig. 9 shows one of the results obtained. In this case, we consider the joint influence of three errors: a substrate irregularity, a variation of the focal length of the correction lenses expressed in terms of the resist layer thickness before processing, and aberrations generated by the lenses. The result of the simulation is graphically represented in terms of a "tolerance volume" as shown in the figure. Here, in addition a coupling error of 0.3 degrees was assumed. The picture shows that due to the correcting influence of the lens system very large variations (aberrations) can be tolerated.

With the given results, it is finally possible to estimate the temporal skew that may occur in a planar

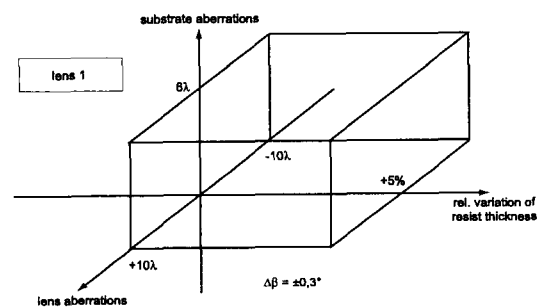

FIG. 8. Results of the simulations and measurements.

FIG. 9. Result of a simulation for calculating the effect of substrate irregularities and aberrations as well as irregularities of the lenslets in the correction system.

optical clock distribution system.

V. CONCLUSION

We have discussed the use of free-space optics as an interconnection technology for computing and switching applications. The use of the third dimension is the key to efficient data communications.

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