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Active Front End Inverter with Quasi – resonance

Henrik Siebel and J.M. Pacas*

Ingenieurbüro Siebel, Kreuztal, Germany
Institute of Power Electronics and Electrical Drives, University of Siegen, Siegen, Germany

ABSTRACT

A new three-phase soft-switching active front-end inverter is presented. The topology consists of a quasi-resonant PWM boost converter with an additional resonant branch, which provides low loss at high frequency operation. This leads to a high conversion efficiency and a remarkable reduction in the size of the input inductor. To synchronise the PWM pattern with the resonance cycle, a modified space vector modulation with asymmetrical PWM pattern is used. A high power factor can be achieved for both power flow directions. Due to a new control strategy the converter features a low content of harmonics in the line currents even for distorted line voltages.

Keywords: Power factor correction, resonant converters, front-end inverter

1. Introduction

The compliance with national and international regulations e.g. IEC1000-3-2 makes it necessary to develop in more and more applications new devices with a power factor correction (PFC) and low harmonics contents in the input currents. These requirements can be fulfilled by using active front-end inverters. Additional advantages of the active front-end inverter are the regenerative operation, the lack of the otherwise necessary braking chopper and resistor and the extended range of the input voltage. Thus the DC-link voltage can be held to a constant value despite of different values of the voltage in the mains or fluctuations of the same.

It is well known that the quality of the current on the mains, which can be represented by its ripple, depends on the switching frequency of the inverter and on the inductance of the input chokes. If the target is a low ripple in the currents by using low inductance, low weight, low volume chokes, a very high switching frequency is indispensable. In hard-switched topologies the high switching frequency leads to detrimental switching losses that lower the efficiency of the converter. As a consequence switches with higher rated currents are necessary. In early works of the authors a quasi-resonant topology for a very high efficiency active rectifier was presented. This was now extended as it is depicted in Fig. 1 for the active braking operation but essentially it works in the same manner. For the soft switching of the transistors in the main bridge, an auxiliary circuit is used building a quasi-resonant configuration, which provides ZVS conditions for the switches and a limited di/dt of the diode currents. As the switching frequency can be chosen very high, the dimensions, weight and cost of the input inductors can be reduced while keeping the total losses within an acceptable range.

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Corresponding Author: pacas@uni-siegen.de Tel: +49-271-740-4671, Fax: +49-271-740-2777

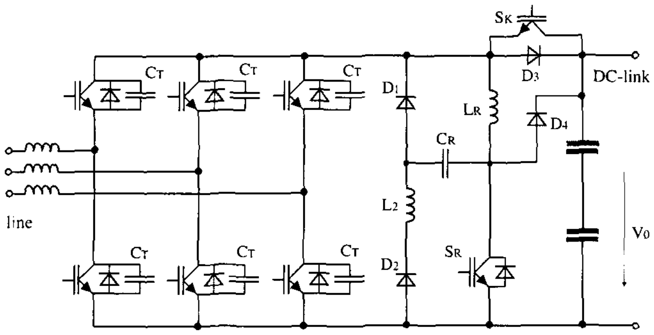


Fig. 1. Quasi-resonant active front-end inverter.

2. Operation

The quasi-resonant cycle starts at the beginning of every PWM period. The quasi-resonant cycle is very short and takes about 10% of the whole PWM-Cycle. During the quasi-resonant cycle the voltage across the transistors of the bridge is forced to become zero for a short time so that the current carrying switches can be closed with ZVS at this moment. With the snubber C_B, a soft turn-off (ZVS) is possible at any moment and PWM capability is given.

In order to explain the mode of operation of the quasi-resonant circuit the circuit can be presented in a simplified manner (Fig. 2). The equivalent circuit results in a current source I_0, an equivalent bridge capacity $C_B = 3\ C_T$ and an anti-parallel diode D_B. The DC-link Voltage will be assumed constant. The inductance L_2 can be neglected in the simplified analysis. In forward operation and in recuperation different switching sequences are necessary and both will be presented the following.

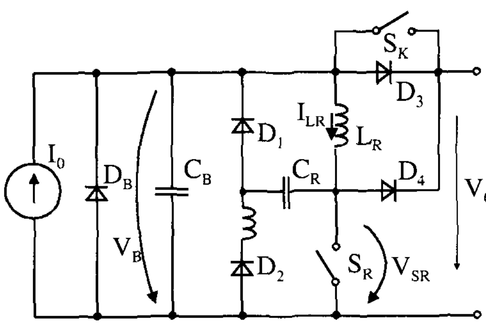


Fig. 2. Equivalent circuit.

2.1 Rectifier Operation

The resonant cycle for a positive power flow is shown in Fig. 3. The different phases of the cycle are:

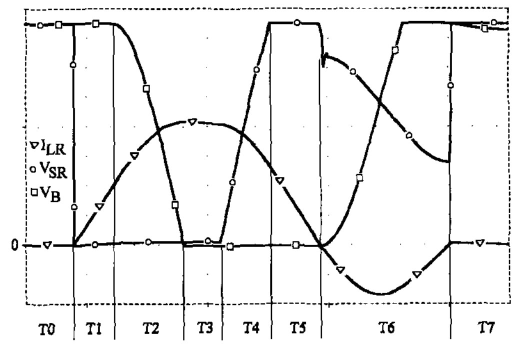


Fig. 3. Resonant cycle - positive power flow.

T0: Initial state. The current flows from the mains into the DC - link.

T1: Switch S_R is closed and current IR is built up in the inductance L_R.

T2: Current ILR is larger than current I0 and the diode D3 is currentless (ZCS and ZVS). The resonant current discharges the bridge capacitor CB.

T3: Bridge capacitor CB is completely discharged and the transistor bridge can be turned on by ZVS (I_0 gets zero). The current I_{LR} is now carried by the bridge diode D_B.

T4: Switch S_R is opened by ZVS and the current flows in the resonant capacitor C_R. While the current is decreasing in L_R, C_R is being charged up to V_O.

T5: Current in L_R flows through D_4 into the DC - link and gets zero. The maximum voltage stress on S_R is limited to V_0.

T6: Resonant process takes place discharging C_R and charging C_B up to V_0.

Final state. No current will flow from the mains into the DC - link due to zero vector switched in bridge.

2.2 Recuperation

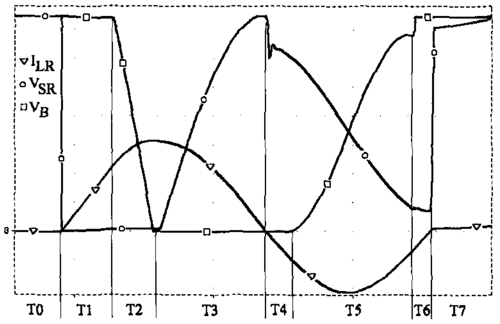
For recuperative operation i.e. for a flow of energy from the DC-link into the mains the different segments of the resonant cycle are explained in the following Fig. 4 and Fig. 5 depicts the 8 time segments T0 to T7.

T0: Initial state. The switches of the input bridge build a zero space phasor and no current flows from the DC-link into the mains.

T1: The switch S_R is closed (ZCS) and the current I_{LR} is built up in the inductance L_R. The time for the switch over into T2 is calculated in a way that the voltage V_{SR} reaches the value V_0 at the end of the interval T3.

T2: Switch S_K is opened (ZVS) and the resonance current I_{LR} discharges the bridge capacitor C_B.

T3: Switch S_R is opened (ZVS) and the current I_{LR} flows into the capacitor C_R. The current I_{LR} decays and goes through zero. During this time the voltage



ig. 4. Resonant cycle - negative power flow.

on capacitor C_B reaches V_0. The bridge capacitors are totally discharged and now the bridge switches can be switched on (ZVS). (I_0 is switched on).

T4: The current I_{LR} becomes negative and flows through the diode D_2 back into the bridge.

T5: The current I_{LR} becomes bigger than I_0 .In a resonant cycle C_R is discharged while C_B gets charged.

T6: When the voltage V_B becomes maximum or equal to V_0 the switch S_K is closed. The current I_{LR} decreases and becomes zero.

T7: Final state. The current flows from the DC-link into the mains.

3. Modified Space-Vector PWM

The principle of the space-vector modulation is a well-known method for the generation of sinusoidal

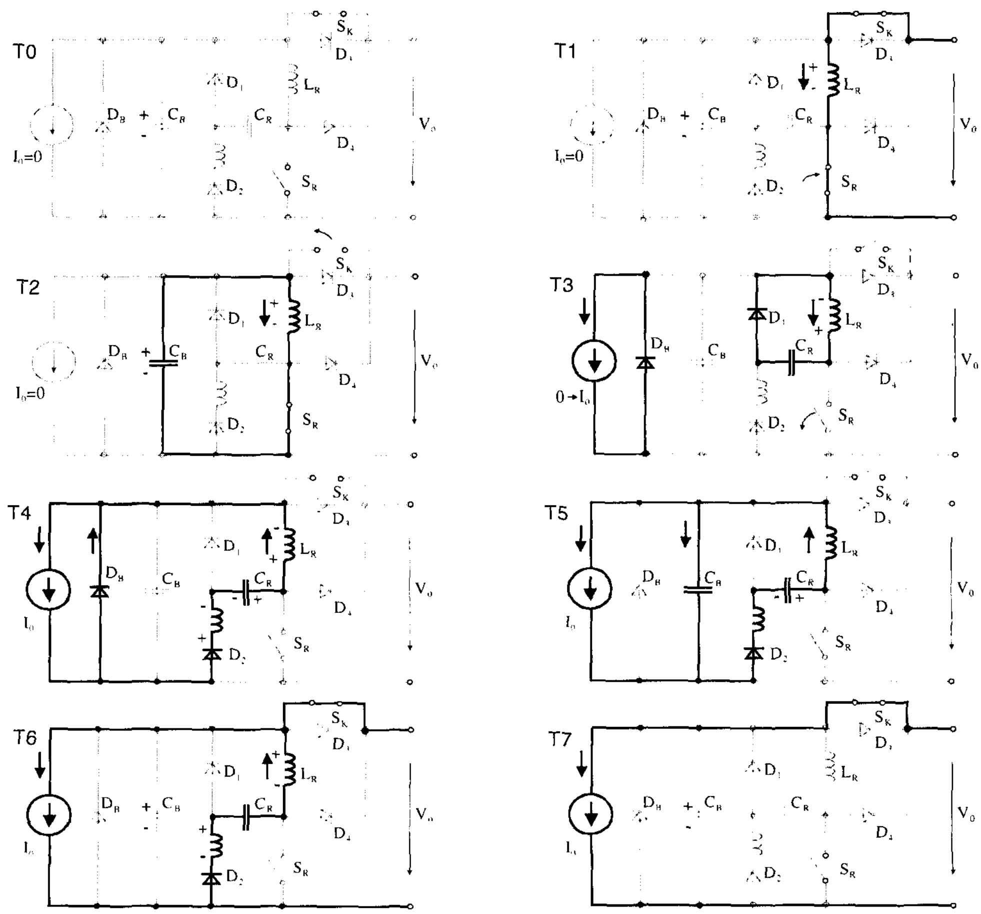


Fig. 5. Resonant cycle - negative power flow.

currents in inverters. This principle can also be used for controlled rectifiers to achieve sinusoidal input currents. The mains can then be considered as a synchronous generator able to work in different operating regions.

The voltage vector V_{rect} is generated by space vector modulation. Fig. 6 shows the eight possible space vectors, where Z_0 and Z_7 are zero vectors. Z_0 means that the three lower switches are closed and Z_7 means upper ones are closed. The required voltage space phasor V_{rect} is generated in each PWM-period out of three of the eight space phasors Z_n. The power will flow from the mains into the DC - link if the angle between the current vector I_{line} and voltage vector Z_n is smaller than 90. If this angle is greater than 90° the energy flow is from the DC-link into the mains.

For the realisation of the PWM it must be taken into account that the line current charges and discharges the bridge capacitors C_B. Therefore the polarity of the line current determines the sequence of the space phasors to be switched. Depending on the position of the current space phasor I_n either Z_0 or Z_7 are chosen as the zero-space-phasor.

It is common practice in the space phasor modulation to define 6 sectors V1 to V6 limited by the space phasors Z_0 - Z_7. In the same way it is possible to define six sectors I1 to I6 for the position of the current space phasor I. Within one of these sectors the polarity of the line currents $\underline{I}_n$ does not change. The border between two sectors corresponds to the zero crossing of one of the line currents and is depicted by the dotted line in Fig. 6. The hatched areas illustrate the sectors V1 and I1.

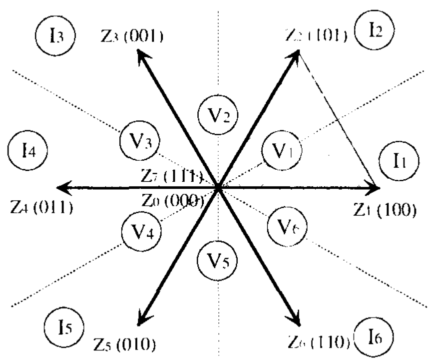


Fig. 6. Space vectors.

In each of the six current sectors the voltage space phasor will be located in one of the adjacent voltage segments if the unit works as rectifier or in the opposite sectors if working in recuperation.

Table 1 shows the sequence for the switching of the voltage space phasors Z_n in each of the sectors. This sequence changes within a voltage sector if the current space phasor moves into the next sector. For the correct operation of the whole system the resonance cycle must be started prior to each PWM-Cycle. This is indicated in the table with R_E for rectifier operation and R_R for recuperation.

4. Non-linear Voltage Controller

One advantage of the development of active rectifiers is the size reduction of the DC link capacitor. To avoid overvoltages in the DC link, a fast voltage controller is usually employed. This leads to a constant DC link

Tab. 1. Space vector sequence.

	V_1	V_2	V_3	V_4	V_5	V_6
I_1	R_E, Z_7,Z_2,Z_1	-	R_R, Z_4,Z_3,Z_0	R_R, Z_4,Z_5,Z_0	-	R_E, Z_7,Z_6,Z_1
I_2	R_E, Z_0,Z_1,Z_2	R_E, Z_0,Z_3,Z_2	-	R_R, Z_5,Z_4,Z_7	R_R, Z_5,Z_6,Z_7	-
I_3	-	R_E, Z_7,Z_2,Z_3	R_E, Z_7,Z_4,Z_3	-	R_R, Z_6,Z_5,Z_0	R_R, Z_6,Z_1,Z_0
I_4	R_R, Z_1,Z_2,Z_7	-	R_E, Z_0,Z_3,Z_4	R_E, Z_0,Z_5,Z_4	-	R_R, Z_1,Z_6,Z_7
I_5	R_R,Z_2,Z_1,Z_0	R_R, Z_2,Z_3,Z_0	-	R_E, Z_7,Z_4,Z_5	R_E, Z_7,Z_6,Z_5	-
I_6	-	R_R, Z_3,Z_2,Z_7	R_R, Z_3,Z_4,Z_7	-	R_E, Z_0,Z_5,Z_6	R_E, Z_0,Z_1,Z_6

voltage and the power in the mains is equal to the load power at any time. The fast controller ensures a low content of harmonics in the line current only for ideal conditions i.e. for constant load current and sinusoidal line voltage. Yet, variations in the line voltage produce variations of the same order in the currents (Fig. 7). The same effect is obtained at fast variations in the DC load.

A controller with a lower open-loop gain avoids this effect, because it behaves like a current source (Fig. 8). However sudden changes in the load current, for example a load disconnection, can produce an overvoltage in the DC link.

To combine the advantages of both control strategies an adaptive voltage controller with a variable open-loop gain is developed. For small voltage errors, the gain is low and the DC link voltage can vary within the given margins. The gain increases with the error and a fast reaction is given at the boundaries of the tolerance band.

A MATLAB-simulation was carried out to calculate the voltage peaks for different current steps. Fig. 9 shows the response of the DC link voltage for a current pulse of 2 A, Fig. 10 for a current pulse of 16A. Although the disturbance in the second simulation is the eightfold of the first, the voltage peak only increase by a factor of three. One possibility to realise this controller is to use a cubical characteristic (Fig. 11).

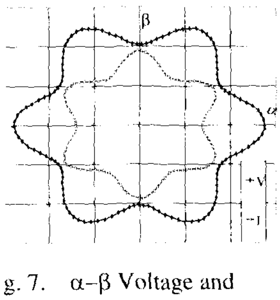


Fig. 7. α–β Voltage and current with a fast controller

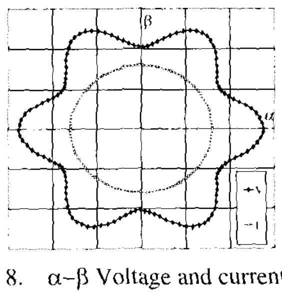


Fig. 8. α–β Voltage and current with a slow controller

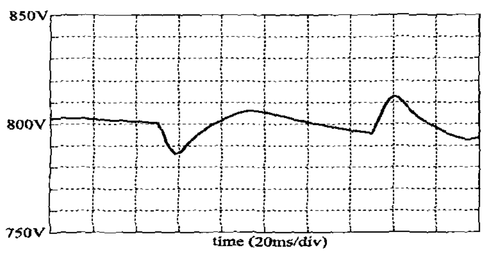


Fig. 9. Voltage response for a 2A current pulse.

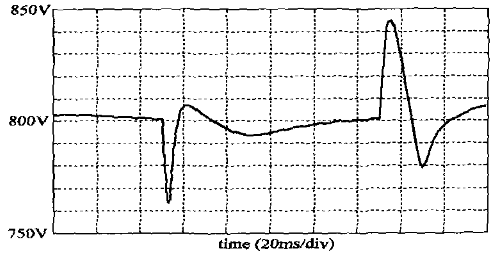


Fig. 10. Voltage response for a 16A current pulse.

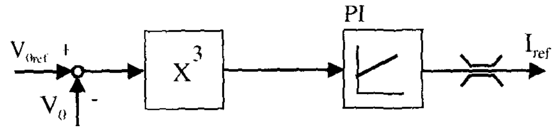


Fig. 11. Cubical voltage controller.

5. Measurements

For the experimental validation of the proposed topology laboratory prototypes were built. The measurements presented in the following were carried out on a 25 kW prototype (Fig. 12) in which the main bridge and the resonant branch was equipped with IGBTs BUP314S. The digital control was realized with a DSP320F240.

There are two criteria to assess active rectifiers: The quality of the input current and the efficiency of the rectifier. The prototype unit is optimised for a high power quality. The content of harmonics is significantly lower than the limits of IEC1000-3-2. The fifth harmonic represents with 0.4 A the greatest distortion. The line currents (Fig. 14) are very smooth at a PWM frequency of 40 kHz and exhibit a very low harmonic content.

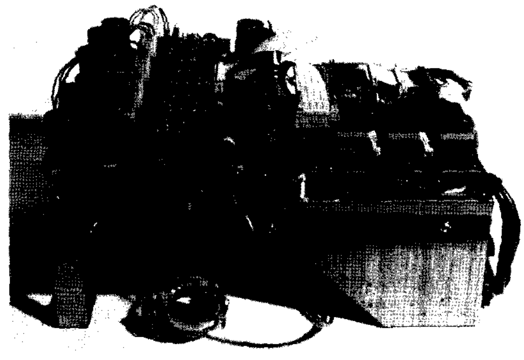


Fig. 12. 25 kW prototype unit.

The efficiency stays in an acceptable range in spite of the high switching frequency. It increases with the input voltage because the input current decreases and the power losses depend on the current.

A weight and cost optimised unit has to work with a lower switching frequency and smaller input inductors at the same time. The efficiency increase, but the quality of the line currents suffers.

In order to examine the behaviour of the unit under real condition additional measurements were carried out. The operation of the active front-end inverter together with a welding machine as load was tested and the dynamic and EMC requirements could be fulfilled.

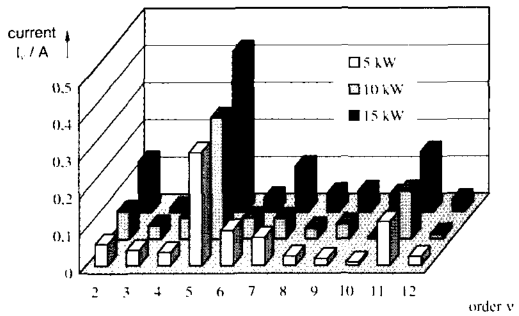


Fig. 13. Harmonics (V_{line} = 400V).

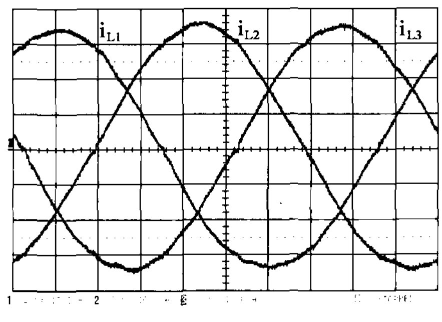


Fig. 14. Line currents (10A/div).

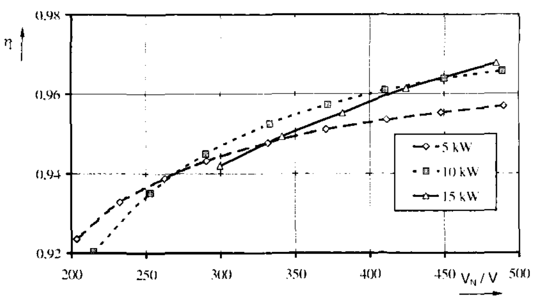


Fig. 15. Efficiency at 40 kHz.

6. Conclusion

In this paper a new three - phase high power factor active front inverter has been presented. The circuit employs an additional quasi-resonant branch, which provides soft switching for all semiconductor devices. The operation of the resonant cycle for positive and negative power flow has been described. A modified space – vector modulation has been developed able to cope with the restrictions of the resonant topology. Measurements of the harmonics and of the efficiency on a weight optimised laboratory prototype were made to verify the proposal.

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José Mario Pacas, Senior Member of the IEEE, studied Electrical Engineering at the University of Karlsruhe in Germany obtaining the Dipl.-Ing. and the Dr.-Ing. -degree in 1978 and 1985 respectively. From 1985 to 1995 he worked for BBC/ABB in Switzerland and Germany in different R&D and management positions with a very wide experience in international projects. In the last years with ABB he was responsible for the development of servo drives and later Product Responsible Manager for these products. Since 1995, he is a member of the Faculty of Electrical Engineering and Computer Sciences of the University of Siegen and heads the Institute of Power Electronics and Electrical Drives. Dr. Pacas is technical consultant to some German companies working in the field of high dynamic drives and power electronics. His special fields of interest are motion control, the integration of intelligent power components, optimisation of mechatronic systems and the rational use of electrical energy in industrial environments.

Henrik Siebel received the Dipl.-Ing. -Degree in electrical engineering from the University of Siegen, Germany, in 1996 and the Dr.-Ing.-Degree in 2001 at the same institution. He was with the Institute of Power Electronics and Electrical Drives, University of Siegen, Germany, as a Research Assistant. He heads currently his own engineering consulting firm. His research activities are related to the design of switching converters for industrial applications.