JPE 3-1-1

Performance Evaluations of Digitally-Controlled Auxiliary Resonant Commutation Snubber-Assisted Three Phase Voltage Source Soft Switching Inverter

Eiji Hiraki* and Mutsuo Nakaoka

Dept. of Electrical and Electronic Engineering, Yamaguchi University, Yamaguchi, Japan

ABSTRACT

This paper presents a performance analysis of typical Auxiliary Resonant Commutation Snubber-assisted three phase voltage source soft switching inverter which can operate under a condition of Zero Voltage Switching (ZVS) using a digital control scheme which is suitable for high power applications compared with resonant DC link snubber assisted soft switching inverter. The system performances of this inverter are illustrated and evaluated on the basis of experimental results.

Keywords: Auxiliary resonant commutation snubber, Zero voltage soft switching, Voltage source inverter, DSP-based digital control scheme

1. Introduction

In recent years, the voltage-source three phase inverters and PFC converters which can operate under the principle of zero voltage or zero current transition soft switching schemes have been developed in order to minimize the switching losses of power devices (such as IGBTs, power MOS-FET, SIT and the like), their electrical dynamic voltage and current stresses as well as voltage and current surge related EMI/RFI noises under high frequency switching.

Of these, three phase voltage-source sinusoidal PWM soft switching inverters and converters are roughly divided into four categories; resonant commutated leg-link[1], resonant AC link[3], resonant DC link[4][5] and resonant switching block link[6]. The feasible comparative studies of the soft switching units mentioned above have been done by many power electronic researches[2].

In this paper, the performances of a three phase voltage source space voltage vector modulated inverter with Auxiliary Resonant Commutated leg-link Snubbers (ARCS) on the basis of the optimal digital control scheme is presented and compared with the conventional hard switching inverter.

2. Circuit Description

Fig. 1 shows the equivalent circuit of a bridge leg in a single phase of ARCS linked three phase voltage source soft switching inverter using IGBT power modules.

Manuscript received March 26, 2002; revised July 23, 2002.

Corresponding Author: hiraki@pe-news1.eee.yamaguchi-u.ac.jp, Tel: +81-836-85-9472, Fax: +81-836-85-9401

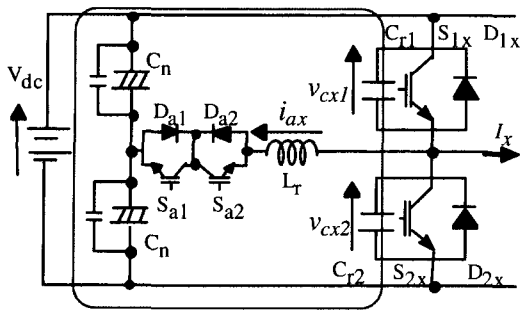


Fig.1. ARCS circuit of one-phase bridge leg.

To illustrate the operating principle of the ARCS-assisted inverter treated here, the resonant commutation from D_{2x} to S_{1x} is discussed. For simplicity, two assumptions are made as follows:

(1) All the switching power semiconductor devices incorporated into this inverter are ideal.

(2) Load current equals to the positive I_x as indicated in Fig. 1, which is kept constant during a short commutation interval.

Fig. 2 displays theoretical operating voltage and current waveforms of main switching devices and auxiliary switching devices in this ARCS circuit. As shown in Fig. 3, there include 10 operation modes. The operating principle of ARCS circuit in a steady-state can be described as follows:

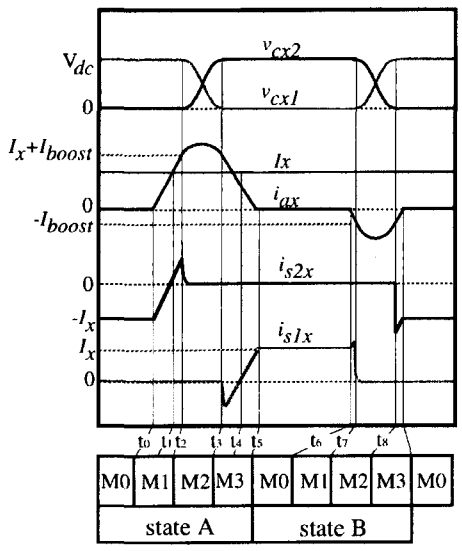


Fig. 2. Theoretical voltage and current waveforms of ARCS circuit.

State A: mode 0 ($t < t_0$)

A positive load current I_x is freewheeling through D_{2x}, while S_{2x} remains on and S_{1x} is off.

State A: mode 1-1(t_0 - t_1)

S_{a2} is turned on under zero current switching (ZCS) condition. The current through D_{2x} begins to decrease linearly as the current through the resonant inductor i_{ax} increases linearly.

State A: mode 1-2(t_1 - t_2)

At t_1, the current via D_{2x} decreases to zero, when a resonant inductor current i_{ax} is equal to the load current I_X. The current flowing into S_{2x} begins to increase. The resonant inductor current becomes greater than the load current, and continues rising until the stored energy is high enough to charge and discharge the resonant capacitors.

State A: mode 2(t_2 - t_3)

After turning off S_{2x} with zero voltage switching (ZVS), the resonant capacitor C_{r1} begins to discharge to zero, while the other resonant capacitor C_{r2} begins to charge towards dc-link voltage. This is a resonance between the resonant inductor and the resonant capacitors C_{r1} and C_{r2}.

State A: mode 3-1(t_3 - t_4)

At t_3, D_{1x} begins to conduct and resonant inductor current begins to decrease linearly. On the other hand, S_{1x} can be turned on at complete ZVS/ZCS hybrid conditions.

State A: mode 3-2(t_4 - t_5)

At t_4, the current via D_{1x} commutates to S_{1x} and resonant inductor current decreases linearly.

State B: mode 0(t_5 - t_6)

At t_5, the resonant inductor current becomes zero and D_{a1x} is turned off. The load current will be totally transferred to S_{1x}.

State B: mode 1(t_6 - t_7)

S_{a1} is turned on with ZCS condition. The resonant inductor current begins to increase linearly towards the minus direction and continues to rise until the stored energy is high enough to charge and discharge the resonant capacitors C_{r1} and C_{r2}.

State B: mode 2(t_7 - t_8)

After turning off S_{1x} with ZVS, the resonant capacitor C_{r1} begins to charge to full dc-link voltage while C_{r2} begins to discharge towards zero.

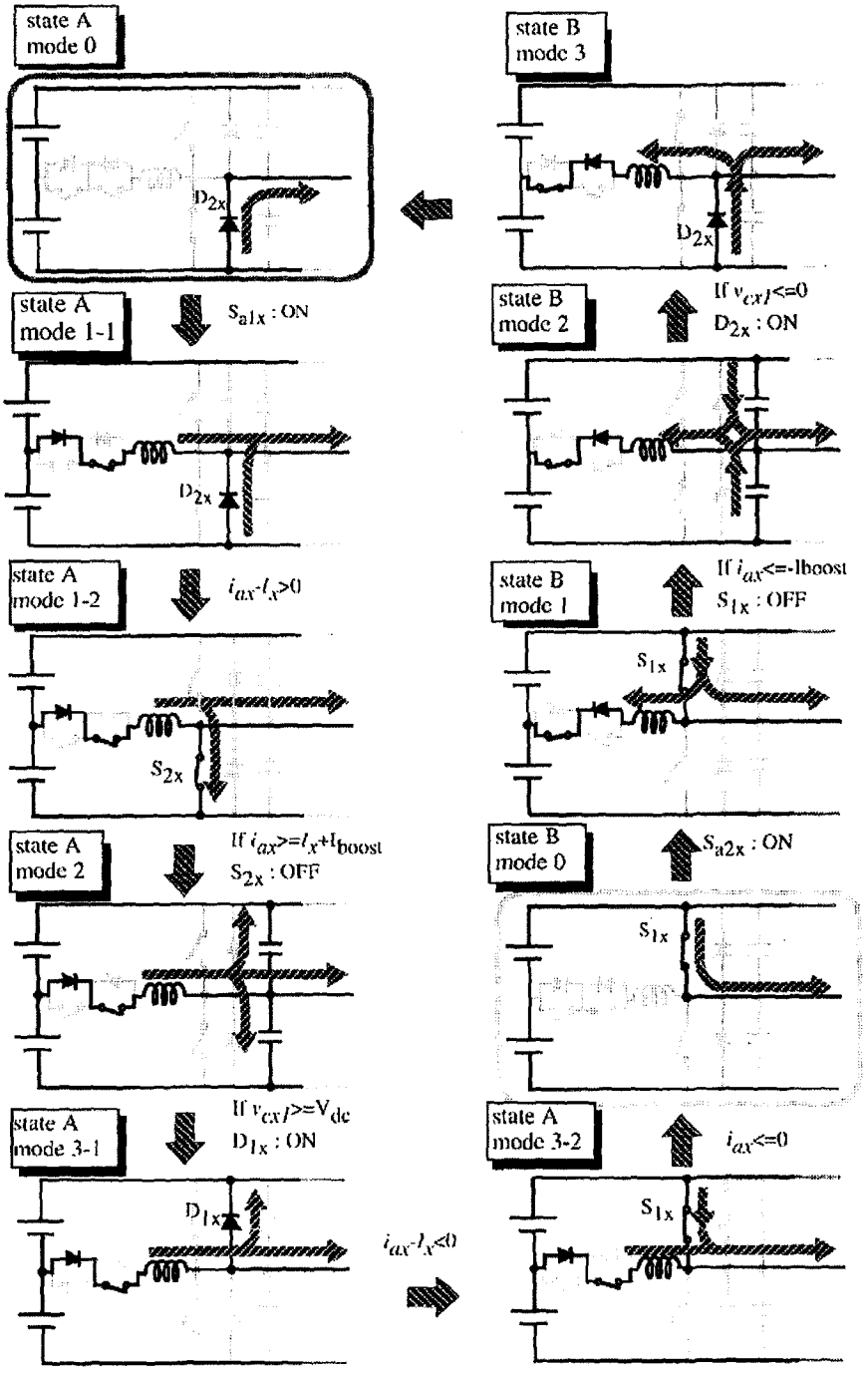


Fig. 3. Equivalent circuit for each operation stage of ARCS.

State B: mode 3($t > t_8$)

At t_8, D_{2x} conducts and a resonant inductor current begins to decrease linearly towards minus direction. When the resonant inductor current becomes zero, D_{a2x} is turned off and transfers back to state A: mode 0.

In this operation, the resonant capacitor C_{r1} or C_{r2}, which is parallel with the active switch D_{1x} or D_{2x} incorporated into the bridge leg, behaves as a lossless capacitive snubber due to a quasi-resonance.

3. System Model and Digital Control Scheme

3.1 Inverter System Model

Fig. 4 shows a schematic diagram of ARCS-assisted three phase voltage source inverter. The output stage of this inverter is depicted in Fig. 5. The inverter output voltage vector, filter capacitor line voltage vector, filter reactor current vector, filter capacitor current vector and load current vector are respectively defined as,

$$i_A = \begin{bmatrix} i_{Au} \\ i_{Av} \\ i_{Aw} \end{bmatrix},\ i_C = \begin{bmatrix} i_{Cu} \\ i_{Cv} \\ i_{Cw} \end{bmatrix},\ i_L = \begin{bmatrix} i_{Lu} \\ i_{Lv} \\ i_{Lw} \end{bmatrix},\ v_A = \begin{bmatrix} v_{Au} \\ v_{Av} \\ v_{Aw} \end{bmatrix},\ v_C = \begin{bmatrix} v_{Cu} \\ v_{Cv} \\ v_{Cw} \end{bmatrix}$$

In this system, the state equation is described as,

$$L_f \frac{d}{dt}\hat{i}_A = \hat{v}_A - \hat{v}_C - R_f \cdot \hat{i}_A \tag{1}$$

$$3C_f \frac{d}{dt}\hat{v}_C = \hat{i}_A - \hat{i}_L \tag{2}$$

The state vector equation of this inverter system transferred into the coordinate d-q axis plane is represented as follows:

$$\frac{d}{dt}\hat{i}_A = \begin{bmatrix} -R_f/L_f & \omega_e \\ -\omega_e & -R_f/L_f \end{bmatrix} \hat{i}_A + \frac{1}{L_f}\hat{v}_A + \frac{1}{L_f}\hat{v}_C \tag{3}$$

$$\frac{d}{dt}\hat{v}_C = \begin{bmatrix} 0 & \omega_e \\ -\omega_e & 0 \end{bmatrix} \hat{v}_C + \frac{1}{L_f}\hat{i}_A + \frac{1}{L_f}\hat{i}_L \tag{4}$$

Finally, the system equation of this circuit is written as,

$$\frac{d}{dt}\hat{x} = A_C\hat{x} + B_C\hat{v}_A + D_C\hat{i}_L \tag{5}$$

where,

$$\hat{x} = \begin{bmatrix} i_{Ad} \\ i_{Aq} \\ v_{Cd} \\ v_{Cq} \end{bmatrix},\ A_C = \begin{bmatrix} -R_f/L_f & \omega_e & -1/L_f & 0 \\ -\omega_e & -R_f/L_f & 0 & -1/L_f \\ 1/3C_f & 0 & 0 & \omega_e \\ 0 & 1/3C_f & -\omega_e & 0 \end{bmatrix}$$

$$B_C = \begin{bmatrix} 1/L_f & 0 \\ 0 & 1/L_f \\ 0 & 0 \\ 0 & 0 \end{bmatrix},\ D_C = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ -1/3C_f & 0 \\ 0 & -1/3C_f \end{bmatrix}.$$

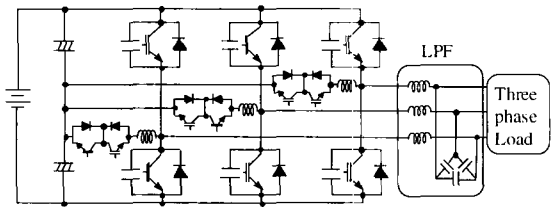


Fig. 4. ARCS assisted three phase voltage-source inverter system.

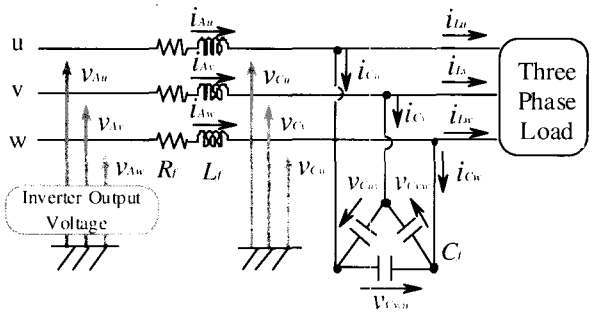


Fig. 5. Three phase low-pass filter and load circuit.

The state vector equation as a discrete-time inverter system is given by,

$$\hat{x}[i+1] = A_Z\hat{x}[i] + B_Z\hat{v}_A[i] + D_Z\hat{i}_L[i] \tag{6}$$

where, $A_Z = e^{A_C T_s}$, $B_Z = \int_0^{T_s} e^{A_C C^\tau} d\tau \cdot B_C$,

$D_Z = \int_0^{T_s} e^{A_C C^\tau} d\tau \cdot D_C$, Ts : sampling period.

Therefore, the output equation of this inverter system is

$$v_C[i] = C_Z\hat{x}[i] \tag{7}$$

where, $C_Z = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$.

3.2 Optimal Type I Digital Servo-Based Control Scheme

The mathematical model of this three phase inverter system is formulated as a two input (vd*, vq*) and two output system, for which the state feedback control scheme is more suitable. The optimal type I digital servo system is constructed in accordance with the internal model principle, since it guarantees a stable feedback system without steady-state errors in response to a step reference and various disturbances.

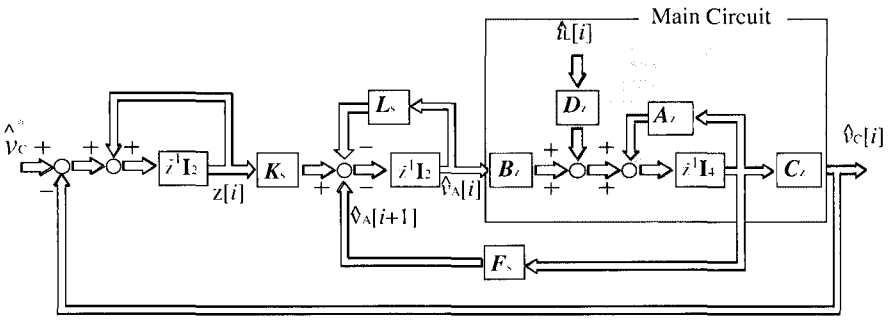


Fig. 6 shows the two inputs and two outputs optimal type I digital servo control system. In this system, the control law is specified as the following equations:

$$\hat{v}_A[i+1] = -F_S\hat{x}[i] - L_S\hat{v}_A[i] + K_S z[i] \tag{8}$$

$$z[i+1] = z[i] + \hat{v}^*_C - C_z\hat{x}[i] \tag{9}$$

where, $\hat{v}^*_C = \left[\hat{v}^*_{cd} \quad \hat{v}^*_{cq}\right]^T$: a reference voltage vector in d-q axis plane, FS, LS and KS: feedback gain vector of the type I digital servo controller. In order to determine the system gains; F_S, L_S and K_S values, an optimal feedback gain F_{re} indicated in Fig. 7 is estimated from linear control theory. The performance index J of this power conditioning system is defined as the following quadratic form:

$$J = \sum_{i=0}^{\infty}\left\{\hat{x}[i]^T \; Q\hat{x}[i] + \hat{v}_A[i]^T \; R\hat{v}[i]\right\} \tag{10}$$

where, Q and R: weighting coefficients.

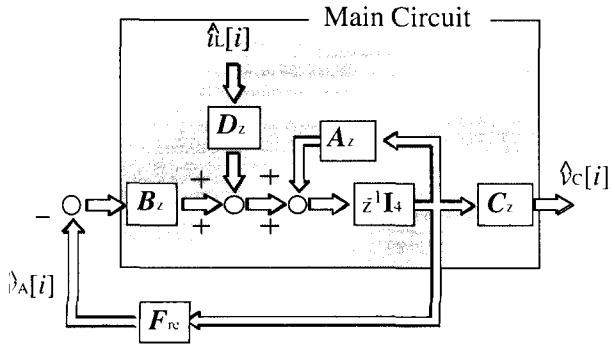


Fig. 7. Optimum digital regulator.

The optimum feedback gain vector is regulated such that it minimizes the performance index J and is estimated as follows:

$$F_{re} = \left(R + B_Z^T P B_Z\right)^{-1} B_Z^T P A_Z \tag{11}$$

where, P is a semi-definite matrix which satisfies the following Riccati equation:

$$P = Q + A_Z^T P A_Z - A_Z^T P B_Z \left(R + B_Z^T P B_Z\right)^{-1} B_Z^T P A_Z \tag{12}$$

In this case, the feedback gains of the optimal type I digital servo controller are estimated by the following equations:

$$L_s = F_{re} + I_2 \tag{13}$$

$$\left[F_s \quad K_s\right] = \left[F_{re}A_Z^2 \quad F_{re}A_Z B_Z + F_{re}B_Z + I_2\right]\begin{bmatrix} A_Z I_4 & B_Z \\ C_Z & 0 \end{bmatrix}^{-1} \tag{14}$$

4. Feasibility Study of Inverter System

4.1 Experimental Setup

Fig. 8 shows the total system configuration of ARCS-assisted three phase soft switching inverter with optimally controlled digital servo scheme. This inverter system is composed of a DC voltage Source, three phase inverter stage with low pass filter, ARCS stage with the mid point of DC busline for each bridge-leg in the inverter its 32bit DSP based controller (TMS320C40) and ARCS control circuit including voltage and current sensors.

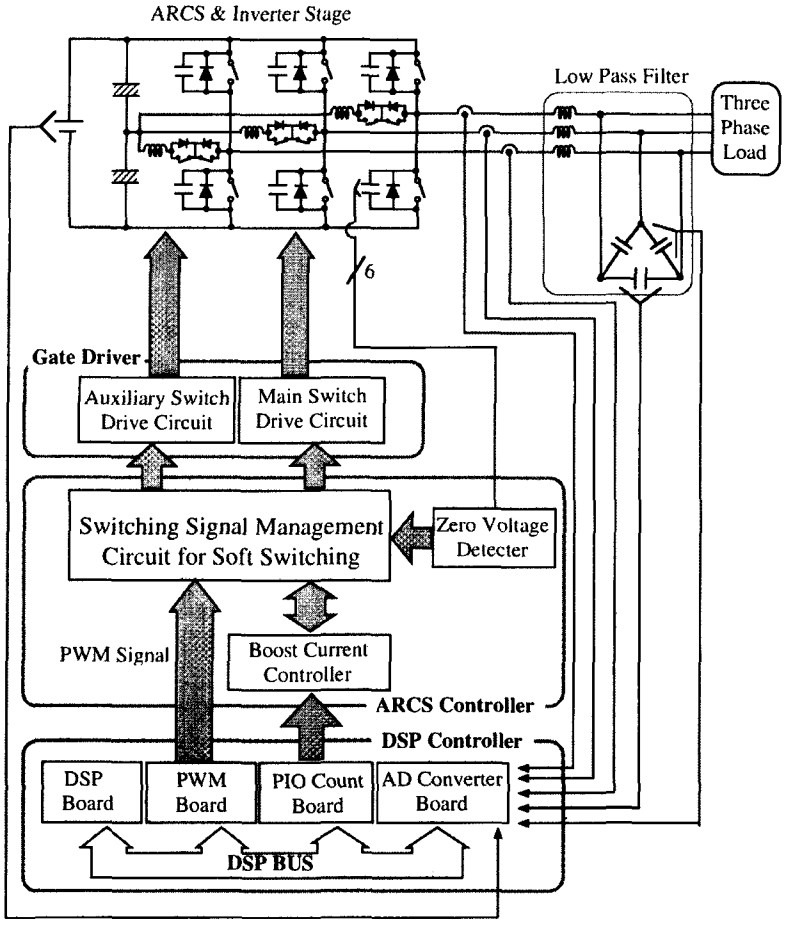


Fig. 8. Block Diagram of Experimental Apparatus.

IGBT 2 in 1 modules (Fuji electric Co. Ltd.; 2BMI100-060N) is used for all switching power devices. The control circuit receives PWM signals from DSP controller, and then starts resonant commutation operation, and sends the inverter switching signals immediately when the voltage across the switching power device comes down to zero.

A conventional hard switching PWM control scheme can be easily obtained by using this experimental setup, directly connecting with DSP controller and inverter driver circuit. The dead time in the hard switching can be easily changed by the DSP controller setting.

4.2 Experimental Results of Soft-Switching Inverter System

In order to verify the total system performances, the ARCS-assisted three phase inverter system was built and tested under a balanced resistance load. Table1 indicates the design specifications of this soft switching inverter system and conventional hard switching inverter system.

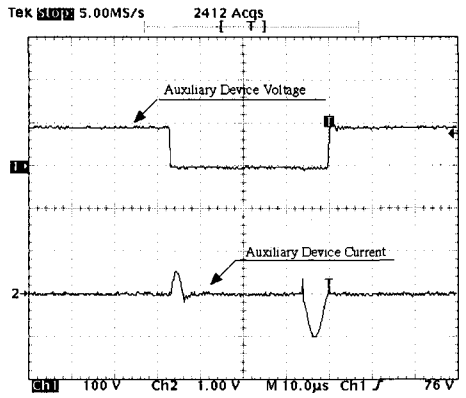
The voltage and current waveforms in the ARCS stage are displayed in Fig. 9. The voltage across the auxiliary switching power devices; IGBTs, are exactly clamped to a half of the DC bus line voltage level.

Fig. 10 shows voltage and current traces of the main switching power devices in the inverter stage during the turn off and turn on periods. Fig. 11 illustrates the switching voltage and current waveforms of the conventional hard-switching voltage source inverter. From these figures, it is clearly proved that all the main and auxiliary switching power devices can completely achieve soft switching, ZVS/ZCS turn on and ZVS turn off for the main devices in the inverter stage in addition to ZCS for auxiliary devices in the ARCS stage.

Fig. 12 represents the output voltage waveforms of this

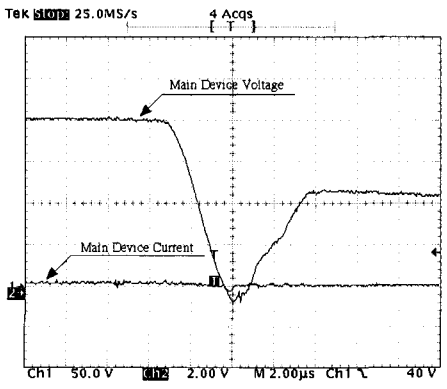
Table 1. Design specifications.

DC Bus line Voltage	Vdc	200 [V]
Devided DC Voltage Capacitor	Cn	8200 [μF]
Resonant Inductance	Lr	12 [μH]
Resonant Capacitance	Cr	0.08 [μH]
Initial Boost Current	I_{boost}	9 [A]
Filter Reactance	Lf	500 [μH]
Filter Resistance	Rf	0.1 [Ω]
Filter Capacitance	Cf	20.0 [μF]
Max Rating Filter Current	I_{fmax}	20.0 [A]
Output AC Voltage	Vac	100 [Vrms]
Output Frequency	Fe	60 [Hz]
Sampling Frequency	Fs	16 [kHz]
Load Resistance	Rl	10 - 100 [Ω]

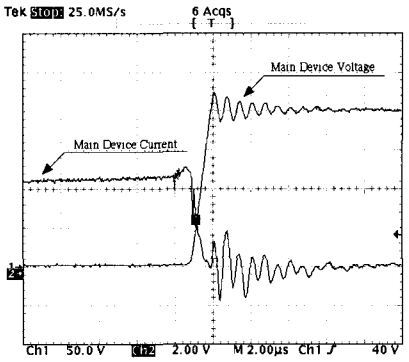


100V/div, 20A/div, 10μs/div

Fig. 9. Measured waveforms of auxiliary device voltage and current in ARCS circuit.



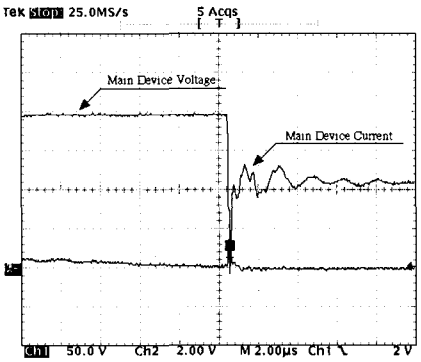
(a) Turn on waveforms



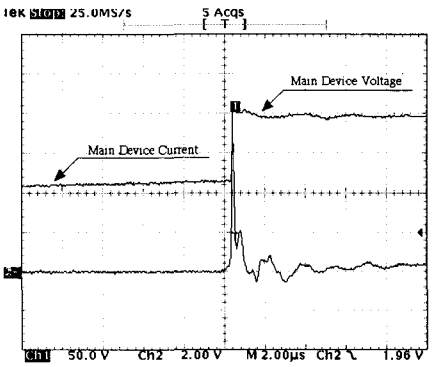
(b) Turn off on waveforms

50V/div, 10A/div, 2μs/div

Fig. 10. Switching waveforms of main devices in ARCS soft switching inverter.



(a) Turn on waveforms

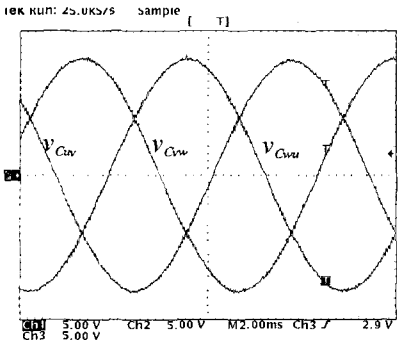


(b) Turn off waveforms

50V/div, 10A/div, 2μs/div

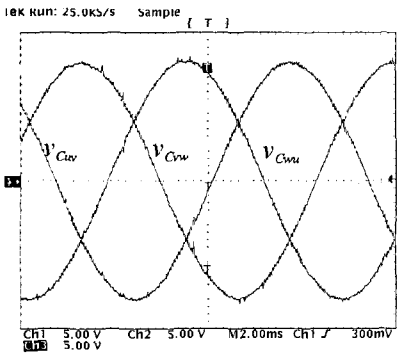
Fig. 11. Switching waveforms of main devices in Hard switching inverter.

soft switching inverter system for the case of a three phase resistive load. Additionally, the output voltage waveforms of conventional hard switching inverter system are shown in Fig. 13. In both case, the reference output voltage is 100 Vrms.



44V/div, 2ms/div

Fig. 12. Output voltage waveforms of soft switching inverter.



44V/div, 2ms/div

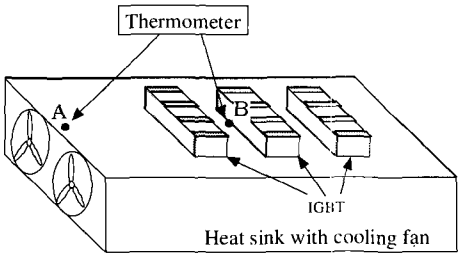
Fig. 13. Output voltage waveforms of hard Switching inverter.

The measured RMS value is 99.9V at soft switching operation and 100.3V at hard switching operation. The measured total Harmonic Distortion (measurable order limitation - 100^{th}: 6kHz); in the case of soft switching, THD is 0.23%, on the other hand, in case of hard switching, THD is 0.37%. These facts indicate that optimal type I digital control scheme mentioned above gives remarkable performance. For the meanwhile, the spike on the waveforms caused by EMI noise related high-speed hard switching operation is frequently observed for hard switching operation.

4.3 Loss Estimation of ARCS System

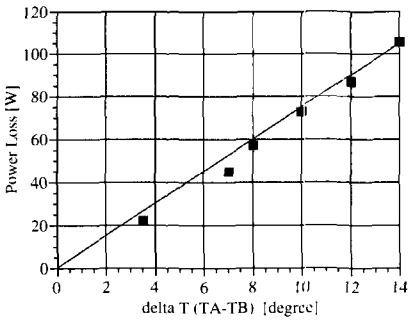
The power losses of the ARCS inverter system have to be separated to ARCS stage losses and main inverter stage losses by using a conversion method from thermal loss to electrical loss. This method of estimating the power losses in the switching power devices from their temperature rise is very effective in a practical system. In the experimental set-up, inverter stage and ARCS stage are mounted each independent large heat sink with cooling fan. As shown in Fig. 14, the average value of power conversion loss including switching losses and conduction losses of the inverter stage can be obtained from relationship between the temperature raise ΔT ($=T_A-T_B$) of the heat sink, which has been pre-measured by the hard switching system. Fig. 15 shows the losses in the ARCS stage and inverter stage as the sampling frequency, changed from 3 to 16kHz, which are obtained under the fixed resistive load condition with the output current at 10.3A. From Fig. 15, the losses of the inverter stage in ARCS-assisted soft switching inverter system are not affected by their switching losses in a wide range of the sampling frequencies. This result suggests that switching losses generated in the power devices on the inverter stage are remarkably reduced.

Fig. 16 shows the total system efficiency of ARCS soft switching inverter and hard switching inverter under 16kHz sampling frequency. Because of the rating current of the output low pass filter, the measurable power area is 3kW maximum. However, these results suggest that the total efficiency of ARCS soft switching inverter is superior to that of the hard switching inverter under a power rating of more than several kW of output power.



A, B : Temperature measured points
$\Delta T=T_B-T_A$

(a) Measure method of inverter stage loss



(b) Conversion data for power loss – temperature

Fig. 14. Power loss analysis.

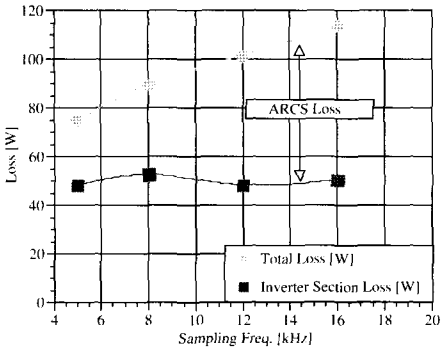


Fig. 15. Measured ARCS soft switching inverter losses.

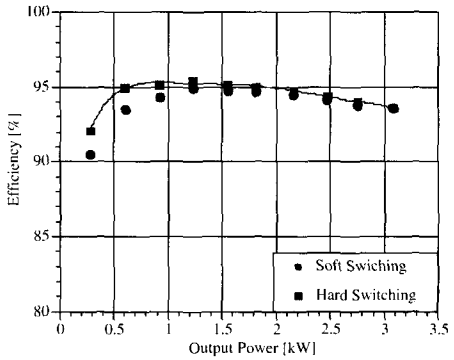


Fig. 16. Total system efficiency.

5. Conclusions

This paper has described the operating principle and features of ARCS linked three phase voltage source soft switching inverter with the optimal type I digital servo controller to track a specified output reference voltage. In addition, the mathematical models of three phase voltage source PWM inverter and its digital control scheme have been represented and formulated. It was proved that the proposed soft switching inverter is able to efficiently operate with high performance ZVS-PWM in order to minimize the switching losses, dynamic electrical stresses as well as EMI noises as compared with that of conventional hard switching inverter.

References

[1] R.W. De Doncker, "The Auxiliary Resonant Commutated Pole Converter", IEEE IAS '89 Records, pp. 829~834, 1989.

[2] R.W. De Doncker, "Hard and Soft-switched Voltage Source Inverters", PESC '94, Taiwan, R.O.C.

[3] J.S. Lai, "Practical Design Methodology of Auxiliary Resonant Snubber inverters", Proceedings of IEEE PESC '96, Vol. 1, pp. 432~437, June 1996.

[4] H. Yonemori, H. Ishii, M. Yoshida, and M. Nakaoka, "Three-Phase ZVS-PWM Inverter System with Transformer-Assisted Quasi-Resonant DC Link and its Feasible Comparative Evaluations", Proceedings of IEEE-PESC, Vol. 1, pp. 171~176, June 1996.

[5] Yong C. Jung, Hyo L. Liu, Guk C. Cho, and Gyu H. Cho, "Soft Switching Space Vector PWM Inverter Using a New Quasi-Parallel Resonant DC Link", Proceedings of IEEE Trans. Power Electronics, Vol. 1, No. 3, pp. 503~511, May 1996.

[6] Eiji Hiraki, Masaki Ishibashi, and Mutsuo Nakaoka, "Feasible Performance Evaluations of Active Resonant Snubber-Assisted Three Phase Soft-Switching Inverter", Proceedings of IEEE-PELS Power Electronics Specialists Conference, Vol. 2, pp. 999~1004, June 1999.

Eiji Hiraki received his M.S. in Electrical Engineering from Osaka University, Japan in 1990. He is currently with the Power Electronic System and Control Engineering Laboratory at Yamaguchi University, Japan, as a Research Associate. His research interests are in the soft-switching technique for high frequency switching power conversion systems. Mr. Hiraki is a member of IEE-Japan and IEEE-USA.

Mutsuo Nakaoka received his Ph. D. degree in Electrical Engineering from Osaka University, Osaka, Japan in 1981. He joined the Electrical and Electronics Engineering Department of Kobe University, Kobe, Japan in 1981. Since 1995, he has been a professor of the Electrical and Electronics Engineering Department, the Graduate School of Science and Engineering, Yamaguchi University, Yamaguchi, Japan. His research interests include application developments of power electronics circuit and systems. He received the 2001 premium paper award from IEE-UK. Dr. Nakaoka is a member of IEE-Japan, Institute of Electronics, Information and Communication Engineers of Japan Institute of Illumination Engineering of Japan, European Power Electronics Association, IEE-UK and IEEE-USA.