유전알고리즘을 사용한 HVDC용 퍼지 제어기의 설계

論 文 52A-1-5

Tuning of Fuzzy Logic Current Controller for HVDC Using Genetic Algorithm

安鍾普·黃琪鉉**·朴俊灏*** (Jong-Bo Ahn·Gi-Hyun Hwang·June Ho Park)

Abstract - This paper presents an optimal tuning method for Fuzzy Logic Controller (FLC) of current controller for HVDC using Genetic Algorithm(GA). GA is probabilistic search method based on genetics and evolution theory. The scaling factors of FLC are tuned by using real-time GA. The proposed tuning method is applied to the scaled-down HVDC simulator at Korea Electrotechnology Research Institute(KERI). Experimental result shows that disturbances are well-damped and the dynamic performances of FLC have the better responses than those of PI controller for small and large disturbances such as ULTC tap change, reference DC current change and DC ground fault.

Key Words: HVDC, Genetic Algorithm, FLC, ULTC

1. Introduction

High Voltage Direct Current (HVDC) converts AC into direct current (DC) in a rectifier and transmits DC power through the transmission line, and then reconverts DC into AC power in a inverter and supplies the power. Since voltage, current, and transmission power in the DC transmission can be controlled rapidly relative to the AC transmission, it is robust against a disturbance and increases a dynamic characteristic of AC power system, while decreases a short-circuit capacity.

Power system controllers based on the modern control theory such as optimal and modal controller[1-2] show better performances to the dynamic disturbances than conventional PID controllers. However, the practical application of the modern control theory in real HVDC system is difficult because it is a highly nonlinear system dependent on the ignition angle of converter and AC system voltage.

The conventional controllers [1-4] used to improve a dynamic characteristic are a lead-lag controller and a Proportional-Integral (PI) controller. They are designed by

the root locus and Bode plot method, using the linearized model at a specific operating point. As they are designed using the linearized model at a specific point and linear control theory, they can show a good performance at a specific point, however, they are not to be expected to obtain a good performance, in cases where operating conditions of power system, such as load variation and system default, change. Furthermore, methods [5-7] are proposed. They have an adaptive capability against time-variation and nonlinear of power system using an adaptive control theory. They increase the dynamic characteristic of power system, but cannot control in real-time. Recently, intelligent controls [8], such as fuzzy logic controller (FLC) and neural network controller as HVDC system controller, are proposed, such that it improves the dynamic characteristic of HVDC system[9,10].

The HVDC systems have the advantages of fast power controls and power modulations[11,12]. Therefore, the control characteristics of the HVDC system are very important for the stabilization of the HVDC system. In this paper, we propose an FLC current controller for HVDC using genetic algorithms(GA). To evaluate the effectiveness of the proposed FLC, HVDC power system simulator is utilized in Korea Electrotechnology Research Institute(KERI). As a result of the experiment, the FLC shows the better performance than PI controller in regard to the disturbance used in designing the FLC. Also, it shows better robustness than PI controller in regard to disturbances, which is not used in designing the FLC for evaluating the robustness of the proposed FLC.

接受日字: 2002년 8월 27일 最終完了: 2002년 9월 29일

^{*} 正 會 員 : 한국전기연구원 메카트로닉스부

^{**} 正 會 員 : (주)이노트론 기술연구소 소장·工學博士

^{***} 正 會 員:釜山大 電氣工學科 教授・工學博士

2. System Model

2.1 HVDC System

Fig. 1 shows the configuration of HVDC simulator at k ERI which is used to evaluate the validity and to design F .C using GA. This HVDC simulator is a scaled-down nodel of 300MW of actual HVDC system that links the nainland Haenam and island Jeju. The rated capacity is 5 kW] on the output side of DC reactor, where its voltage is ±250[V] and current is 10[A]. The HVDC system is configured in bi-polar mode by two conductors, where the conductors have opposite poles to each other in order to control the two poles independently.

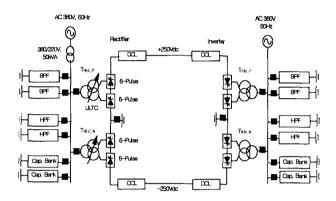


Fig. 1 Configuration of HVDC simulator in KERI

The advantage of bi-polar configuration is that it has a capability of operating in mono-polar mode when one of tie two poles is damaged. Thyristor valve has 2 bridges per pole and 6 valves per bridge, which outcomes total 48 alves and each will be replaced when it becomes camaged. The model of the DC line can simulate the estual line of up to 500[km] and is composed of two quivalent variable resistors. Total four of step-down 1 ansformers has the capability of two-way DC t ansmission at 0~150[%] load condition while maintaining the variation range of AC voltage within $\pm 10[\%]$. lurthermore, for having easier control of two-way power tow, the transformers secondary voltage is calculated according to the various operating condition and then LTC is utilized, in order that it maintain the maximum · oltage in transformer and minimum voltage in inverter when the transformer is 150[%] overloaded. The voltage eviation between the taps in the transformer is 1.5[%] each, and total 24 taps are installed. The range of tap oltage falls from -18.0[%] to +16.5[%]. The compensation of reactive power is shared by the high pass/band pass 1 lters, capacitor banks and the ac power system. For the Turpose of having the compensated capacity of each 11/13th harmonic filter and each high-pass filter to meet the required capacity at the minimum load, the transformer is designed, where unit capacity of the filters is set to 0.6[kVar] and the overall capacity of reactive power compensation becomes 4.8[kVar] per each terminal. Consequently, it is set so the reactive power can be supplied from the AC power only during the excessive occurrence of AC under-voltage and of firing angle. Two capacitors, on the other hand, are installed in 380[V] ac bus, where the AC voltage variation is considered as $\pm 10[\%]$.

2.2 Basic Control Principle of HVDC

The basic control principle of HVDC system is constant current control of dc link. It is because of limiting dc current due to faults and making the system stable due to fluctuation of the ac voltage. Generally, the rectifier is provided with current control and constant ignition angle(CIA) control whereas the inverter is operating on constant extinction angle(CEA) mode.[15] But when the ac voltage at one converter drops by more than about 30%, there are some problems that the reactive power demand of the other converter increases, and commutation failure and voltage instability may happen. Hence as shown in Fig. 2, VDCOL(voltage dependent current order limiter) is used to prevent these risks.

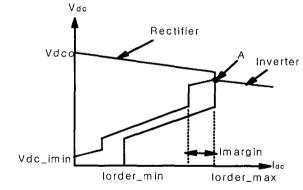


Fig. 2 HVDC steady-state V-I Characteristics

1) Constant current control: Constant current control is a controlling operation that maintains constant current on dc line. In general, however, dc current may undergo a rapid change due to its large influence from the system operating condition. This rapid change of dc current has an effect on the system; therefore, the constant current control is normally performed in the converter that is connected to the weak ac system. The block diagram of the constant current controller is shown in Fig. 3. In the figure, the alpha(rated) of rectifier is 18° and of inverter 155°.

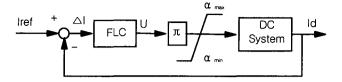


Fig. 3 Block diagram of the rectifier controller

2) CIA and CEA modes: Constant ignition angle(CIA) mode and constant extinction angle(CEA) mode have a fixed firing angle($\alpha_{\min} = 5$) and fixed extinction angle ($\gamma_{\min} = 15$) respectively. If ac voltage is less than 0.85[pu], CEA and CIA are being controlled, whereas if the ac voltage is greater than 0.85[pu], constant current is being controlled. The block diagram of CEA and CIA controller is shown in Fig. 4.

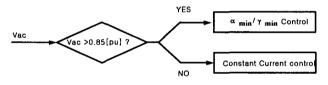


Fig. 4 Control of CEA and CIA

3. The Tuning of FLC Using GA

Conventionally, FLC based on the knowledge of experts and trial-and-error method shows a good control performance. However, it is still difficult for the controller designers to determine the scaling factors and shape of membership functions. Hence, various tuning methods using EC are recently proposed to modify the fuzzy rule and the shape of fuzzy membership function[9,10]. And method that the scaling factors of FLC is tuned by GA was proposed.

Evolutionary computations(ECs) are the optimization algorithms based on the principles of the genetics and natural selection. There are three broadly similar categories of investigation in ECs: Genetic Algorithm (GA), Evolution Strategy(ES), and Evolutionary Programming (EP). In this paper, GA that shows good characteristics in the view of diversity and convergence is used to tune parameters of FLC. The GA operators used in this paper are roulette wheel selection for reproduction, one point crossover, random mutation and elitism[13,14].

Fig. 5 shows the overall configuration of the on-line GA-based FLC tuning system with HVDC simulator. As shown in the figure, the system consists of three parts; master controller, current controller and HVDC simulator.

Master controller(personal computer) performs generating reference signal, gathering data from controller and computing GA. The DSP-based current controller receives reference signal from master controller, performs FLC current control and finally generates the firing signal of HVDC simulator. The controller uses analog-to-digital converter(ADC) to feedback the dc current. HVDC simulator that received the firing angle signal actually thyristors and flows DC current. communication between master and current controllers is via ethernet/TCP network.

After HVDC starts up and builds the dc current at low current level stably, GA tuning procedure starts. Master controller sends step reference change at every 2[sec] with the evaluated FLC parameters. The current controller calculates the error at every sampling interval and sends back to master controller. Master controller evaluates fitness using fitness function and updates parameters through the tuning procedure that will describe hereafter.

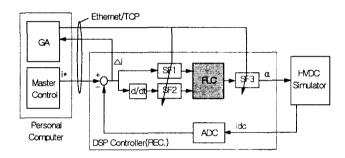


Fig. 5 Configuration of the on-line GA-based FLC tuning system

In this paper, we use GA-based FLC on-line tuning for current controller of HVDC system. The parameters to be tuned are the input and output scaling factors. Fig. 6 shows a triangular membership function used, where we set the center of ZE to 0 and positive and negative membership functions are constructed to be symmetrical of 0. Here, linguistic variable such as NB denotes Negative Big, NM denotes Negative Medium, NS denotes Negative Small and so on. Fig. 7 shows the configuration of population for tuning the scaling factors of FLC.

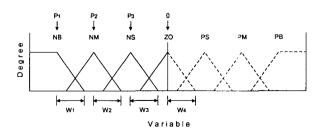


Fig. 6 Symmetrical membership function

S1	SF ₁₁	SF ₁₂	SF ₁₃
S2	SF ₂₁	SF ₂₂	SF ₂₃
		•	
		•	
		•	
Sn	SF _{n1}	SF _{n2}	SF _{n3}

where, 1 : population size

SF_i : Scaling factors

Fig. 7 Strings architecture for tuning scaling factors

The fitness function used to evaluate the each string of population is a sum of the absolute error of direct current as shown in (1). The error data is obtained by digital controller for 2[sec] from the time to change the reference by sampling frequency of 1.8[kHz]. 10[%] step reference is applied to controller at the every generation.

$$fitness = \frac{a}{b + \int_{t=1}^{T} |I_{ref}(t) - I_d(t)|}$$
(1)

where, $I_{dc}(t)$: measured direct current

 $I_{ref}(t)$: reference direct current

T: specified time that data is acquired (2[sec])

a, b: constants

The tuning procedure of FLC for HVDC using GA is as follows.

Step 1) Initialization: As shown in Fig. 7, the initial population is randomly generated after considering the constraints. Set arbitrarily the population size using scaling factors of FLC.

Step 2) Evaluation: Evaluate each string generated in step 1) using the fitness function in equation (1). Evaluation process is done for every populations in specified generation.

Step 3) Reproduction: Roulette wheel reproduced in proportional to the fitness is used.

Step 4) GA operation: The real-valued coding is used o represent a solution. Modified simple crossover and miform mutation are used as genetic operators. The modified simple crossover operator is a way to generate offstrings opulation, selecting two strings randomly in parent opulation as shown in Fig. 8. If crossover occurs in k-th variable, random selection of two strings in t-th generation, offstrings of t-1-th generation are shown in Fig. 8. In miform mutation, we selected a random k-th gene in an adividual. If an individual and the k-th component of the adividual are the selected genes, the resulting individual is as shown in Fig. 9.

Sefore Crossover >
$$S_{\nu}^{l} = [V_{l}, \dots, V_{k}, \dots, V_{n}]$$

$$S_{w}^{l} = [W_{l}, \dots, W_{k}, \dots, W_{n}]$$

$$Crossover point$$

$$\text{where, } V_{j} = a_{l} \ V_{j} + a_{2} \ W_{j}$$

$$a_{l}, a_{2} : \text{Random numbers from } [0, 1]$$

$$V_{j} : j\text{-th gene of the vector } S_{w}$$

$$n : \text{Number of parameters}$$
After Crossover >
$$S_{\nu}^{l+1} = [V_{l}, \dots, V_{k}, V_{k+1}, \dots, V_{n}]$$

$$S_{\nu}^{l+1} = [W_{l}, \dots, W_{k}, W_{k+1}, \dots, W_{n}]$$

$$W_{j}^{l} = a_{l} \ W_{j} + a_{2} \ W_{j}$$

$$S_{\nu}^{l+1} = [W_{l}, \dots, W_{k}, W_{k+1}, \dots, W_{n}]$$

$$S_{\nu}^{l+1} = [W_{l}, \dots, W_{k}, W_{k+1}, \dots, W_{n}]$$

$$W_{j}^{l} = a_{l} \ W_{j} + a_{2} \ W_{j}$$

$$S_{\nu}^{l+1} = [W_{l}, \dots, W_{k}, W_{k+1}, \dots, W_{n}]$$

$$S_{\nu}^{l+1} = [W_{l}, \dots, W_{k}, W_{k+1},$$

Fig. 8 Simple crossover method

where, Vi: Random value between upper bound

Fig. 9 Uniform mutation method

Step 5) Elitism: Elitism is used to reproduce the best individual in terms of fitness into GA and ES population separately.

Step 6) Convergence criterion: Iterate Step 2) ~ Step 5) until satisfying a specified generation.

4. Experimental Results

To evaluate the effectiveness of the proposed FLC, HVDC power system simulator is utilized in the KERI. The overview of HVDC simulator and controllers is shown in Fig. 10. Master controller and rectifier current controller is shown at left in the figure. Fig. 11 shows the detail configuration of current controller. In the figure, DIO, TC, SC, ADC, GD represent digital input/output, timer counter, signal conditioner, analog- to-digital converter and gate driver respectively.



(a) Master controller(upper), DSP controller(lower)



(b)HVDC simulator Fig. 10 Overview of HVDC Simulator in KERI

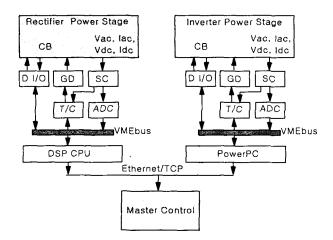
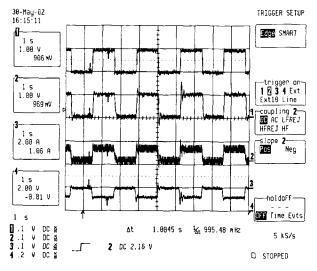


Fig. 11 Hardware configuration of HVDC control system

As described before, HVDC simulator is scaled-down bipolar model and control system is fully digitalized. Therefore, tuning process can be done on-line automatically. First of all, Fig. 12 shows the tuning



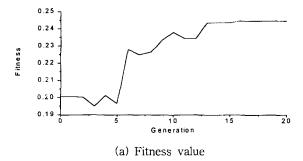
(Ch 1: current reference, Ch 2: filtered DC current, Ch 3: actual DC current, Ch 4: firing angle, time scale: 1[sec/col], y scale: scaled)

Fig. 12 waveform during tuning process

process scaling factor of FLC using GA. From the top in the figure represents DC current reference, filtered feedback DC current, actual DC current and firing angle of rectifier respectively. Each step of reference signal corresponds to the response with parameters that determined at the each population. Because each population has their own parameters, i.e. the scaling factors, figure shows different step responses for every step.

The Fig. 13 shows tuning results after 20 generations. The fitness trend through each generation is displayed in (a) of the figure. Fitness increases gradually and converges as the generation progresses. The Fig. 13(b) represents the gains of input and output of FLC through each generation. As shown in this figure, the gains of input and output of FLC converges to a certain value as the generation increases.

To estimate the usefulness of the tuned parameters of FLC after 20 generations, we test under the various disturbance conditions including step response at the different operating points and large disturbances such as dc line ground faults and ULTC tap sudden change. Figure 14 shows the step responses of the proposed FLC and of the conventional PI controller.



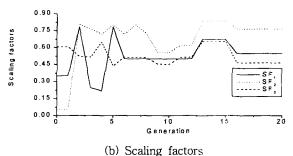
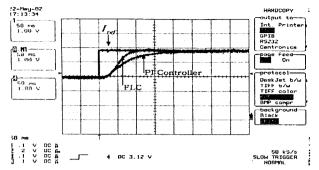


Fig. 13 Fitness and scaling factors in each generation

The current reference changed 0.3[pu] to 0.5[pu]. As presented in this figure, the proposed FLC shows better performance than PI controller in view of the rising and settling time. Figure 15 shows the response of the proposed FLC and of the PI controller to ULTC tap sudden change at 0.5pu current command. In this case, since ULTC tap changes abruptly in the direction of decreasing ac voltage, current drops temporarily and



l ig. 14 Comparison of step response to current reference (0.1[pu/col], time: 50[ms/col])

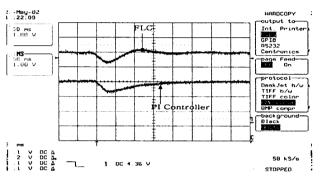
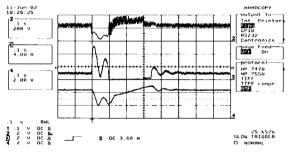
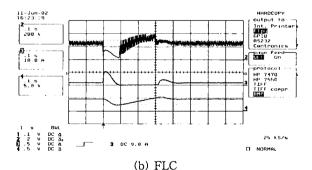


Fig. 15 Response to ULTC tap change (at 0.5[pu], time: 50[ms/col])



(a) PI controller

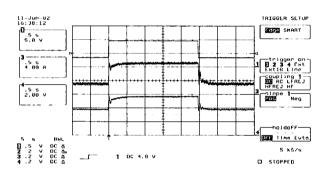


(top : dc volage, mid : dc current, bot : firing angle)

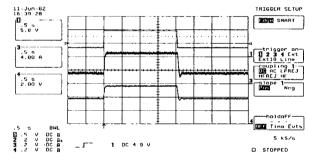
Fig. 16 Response to DC Line Ground Fault

1 estores by the current control action. As presented in this 1 gure, proposed FLC also shows better performance than 1 I controller in the rising time and the settling time, a though slight overshoot exists.

Figure 16 shows response to large disturbance. During the HVDC system is operating at 0.2[pu] current reference, ground fault with some resistance at the dc line is happened for about 0.1[sec]. FLC shows better performance in viewpoint of limiting fault current and restoring after fault clearing than PI controller. Figure 17 shows response to large step reference change of 0.6[pu]. Current reference steps from 0.3[pu] to 0.9[pu] and current response shows the same as the point that tuning was performed, i.e. 0.3[pu]. And this proofs that the tuned parameters are valid for wide operating ranges. For comparing the response more explicitly, results of two experimental cases are displayed the same figure in Fig. 18. It shows that the difference of response is more clear. PI controller raises output very rapidly due to its high gain but it results in longer settling time and undershoot responses.



(a) PI controller



(b) FLC

(top: current reference, mid: dc current, bot:firing angle)

Fig. 17 Response to large step reference change (0.3->0.9[pu])

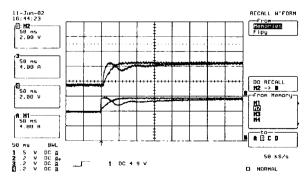


Fig. 18 Step Response (top : dc current, bot : output of controller)

5. Conclusions

In the paper, we propose a fuzzy current controller tuned by the on-line GA. It tunes the three scaling factors of FLC, two input scaling factors and a output one using GA optimization technique. As the result of the experiment using the scaled-down HVDC simulator in KERI in order to compare the proposed FLC with PI controller, the proposed FLC shows the better control performance than PI controller under the various disturbance conditions. Therefore, we concludes as follows;

- (1) We verifies that the FLC current controller tuned on-line under the limited operating condition, that is to say, at the low but relatively stable current reference region(0.3[pu]) shows the better performance than conventional PI controller under various disturbances. That means the tuned FLC guarantees the robustness under different operating points.
- (2) By implementing on-line tuning system by GA technique using the scaled-down HVDC simulator, the proposed tuning methods can be applied to actual HVDC system.
- (3) Further works will be necessary in the areas such more complicated fitness function establishment to classify the difference of response and shortening the tuning time guaranteeing the stability and performances.

Acknowledgement

This work was supported by the grant of 2001 Pusan National University's Oversea Research Program for professors.

References

- [1] C. E. Grund and C. M. Pollard, Power modulation controls for HVDC systems , CIGRE 14-03, 1984.
- [2] S. Lefebvre, HVDC controls for system dynamic performance, IEEE PWRS-6, pp. 743-752, 1991.
- [3] M. A. Chudhury, A. S. Emarah, K. A. Ellithy and G. D. Gallanos, Stability analysis of a modulated ac/dc system using the eigenvalue sensitivity approach, IEEE Trans. PWRS-1, pp. 128-137, 1986.

- [4] Y. Y. Hsu and L. Wang, Damping a parallel ac/dc system using PID power system stabilizers and rectifier current regulators, IEEE Trans. Energy Converson, vol. 3, no. 3, pp. 540-548, 1988.
- [5] S. Lefebvre, M. Saad, and A. R. Hurteau, Adaptive control for HVDC power transmission systems, IEEE Trans. Power Apparatus Syst., vol. PAS-104, no 9, pp. 2329-2335, Sept. 1985.
- [6] W. J. Rugh, Analytical framework for gain scheduling, IEEE Control Syst. Mag., vol.¥±, no. 1, pp. 79-84, Jan. 1991.
- [7] J. Reeve and M. Sultan, Gain scheduling adaptive control strategies for HVDC systems to accommodate large disturbances, IEEE Trans. Power Syst., vol. 9, no. 1, pp. 366-372, Feb. 1994.
- [8] A. Daneshpooy, A. M. Gole, D. G. Chapman and J. B. Davies, Fuzzy Logic Control for HVDC Transmission, IEEE Trans. Power Delivery, vol. 12, no. 4, pp. 1690-1697, Oct. 1997.
- [9] Gi-Hyun Hwang, J. H. Park, H. T. Kang and Sungshin Kim, Design of Fuzzy Power System Stabilizer Using Adaptive Evolutionary Algorithm, Proceedings of IEEE International Symposium on Industrial Electronics, Vol. 2, pp. 42-47, December, 2000.
- [10] Gi-Hyun Hwang, June Ho Park, Jae Young Yoon, Genetic Algorithm Approach to Design the Optimal Fuzzy Logic Controller for Rectifier Current Control in HVDC System, Vol. 3 No. 6, pp. 792-797, 1998, Journal of Electrical Engineering and Information Science.
- [11] C. E. Grund and C. M. Pollard, Power modulation controls for HVDC systems, *CIGRE* 14-03, 1984
- [12] S. Lefebvre, HVDC controls for system dynamic performance, *IEEE PWRS-6* 1991, 743-752
- [13] Z. Michalewicz, Genetic Algorithms + Data Structures = Evolution Programs, Springer-Verlag, 1992.
- [14] Mitsuo Gen and R. Cheng, Genetic Algorithms & Engineering Design, A Wiley-Interscience Publication, 1997.
- [15] P. Kundur, Power System Stability and Control, McGraw-Hill, Inc., 1994

Appendix

1. HVDC simulator ratings

Item	Rating	Remarks
AC Voltage	220[V], 50/60[Hz] 380[V], 60[Hz]	Rectifier Inverter
DC Rating	±250[Vdc], 10[A] 5[kVA]	Bipolar mode
Thyristor	600[V], 25[A]	48pieces, 12-pulse
Transformer	3[kVA], 380/104/104V	Y/Y-△ connection
DC Reactor	12.48[mH]	4 units
11/13th Filter	0.6[kVA]	
High Pass Filter	0.6[kVA]	
Capacitor Bank	1.2[kVA]	2 Bank/station

저 자 소 개



안 종 보(安 鍾 普)

1961년 8월16일생 1986년 서울대학교 전기공학과 졸업. 1995년 한국과학기술원 제어 및 자동화 설계공학과 졸업(석사) 1986년~1996년 이천전기공업(주) 중앙연구소 근무 1996년 ~현재 한국전기연구원 산업전기연구단 메카트로닉스연구그룹(선임연구원)

Tel: 055-280-1478 E-mai: jbahn@keri.re.kr



황 기 현(黃 琪 鉉)

1968년 3월 1일 생. 1994년 경성대 공대 전기공학과 졸업. 1996년 부산대 전기공학 과 졸업(석사). 2000년 2월 부산대 일반대 학원 전기공학과 졸업(공박). 현재 부산대 컴퓨터 및 정보통신 연구소 기금교수

Tel: 051-510-3188

E-mail: hwanggh@hyowon.pusan.ac.kr



박 준 호(朴 俊 頌)

1955년 9월 17일생. 1978년 서울대 공대 전기공학과 졸업. 1980년 동 대학원 전기공학과 졸업(석사). 1987년 동 대학원 전기공학과 졸업(공박). 1978년~1981년 한국전기연구소연구원. 1981년~1984년 충남대 공대 전기공학과 전임강사 및 조교수. 1989년~1990년

Pen. State Univ. Visiting Scholar. 현재 부산대 공대 전기공

학과 교수

Tel: 051-510-2370

E-mail: parkjh@hyowon.pusan.ac.kr