Trenched-Sinker LDMOSFET (TS-LDMOS) Structure for 2 GHz Power Amplifiers

Cheon Soo Kim, Sung Do Kim, Mun-Yang Park, and Hyun-Kyu Yu

This paper proposes a new LDMOSFET structure with a trenched sinker for high-power RF amplifiers. Using a low-temperature, deep-trench technology, we succeeded in drastically shrinking the sinker area to one-third the size of the conventional diffusion-type structure. The RF performance of the proposed device with a channel width of 5 mm showed a small signal gain of 16.5 dB and a maximum peak power of 32 dBm with a power-added efficiency of 25% at 2 GHz. Furthermore, the trench sinker, which was applied to the guard ring to suppress coupling between inductors, showed an excellent blocking performance below –40 dB at a frequency of up to 20 GHz. These results confirm that the proposed trenched sinker should be an effective technology both as a compact sinker for RF power devices and as a guard ring against coupling.

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I. Introduction

Laterally-diffused metal oxide semiconductor field effect transistors (LDMOSFETs) have been widely used in base station power amplifiers for global systems for mobile communication, personal communication service, and wideband code division multiple access for their several advantages: they have good thermal stability; they have no thermal runaway; and they make amplifiers more rugged [1]-[6]. However, for 60 W of output power at a supply voltage of 28 V, a large channel width of a few centimeters is required for transconductance of 4 to 5 S. This constraint results in a large chip size [2]. Much of the chip area is consumed by the source sinker region, which is formed by a high-dose/high-energy implant and thermally driven until it merges with the heavily doped p+ substrate. Thus, a wide gate to the sinker space comparable to the sinker depth is needed due to the lateral diffusion of the heavily doped sinker (Fig. 1(a)). These conditions restrict the structure of conventional LDMOS devices: the chip size cannot be further reduced and high frequency operation above 2 GHz cannot be used.

In this paper, we propose a new device structure called the Trenched-Sinker LDMOSFET (TS-LDMOS), in which the sinker is formed by trench etching and refilled with a doped polysilicon process [7]. Because the sinker area is defined by a trench etching process rather than lateral diffusion and is formed at a temperature below 900 °C, the gate edge to the sinker edge space can be shrunk significantly from 7 μm to 2 μm (Fig. 1(b)). In this way, we reduced the sinker area to less than one-third. We also reduced the total chip area to less than 40% by reducing the pitch of the unit transistor [8]. Furthermore, the resistance of conventional sinkers cannot be easily reduced, because it is fabricated by high temperature

diffusion with a depth of 10 μm. We, however, easily lowered the deep sinker (source) resistance by refilling the heavily doped poly-silicon. Our investigation demonstrated that the TS-LDMOS device is a promising structure for next generation base station RF power amplifiers.

Our trenched-sinker technology can also block the coupling between inductors and the cross talk with adjacent circuit blocks in mixed-signal RF ICs. The trenched-sinker guard ring we used around the spiral inductors showed a superior coupling suppression performance up to 20 GHz and much better isolation characteristics compared with that of deep well technology [9].

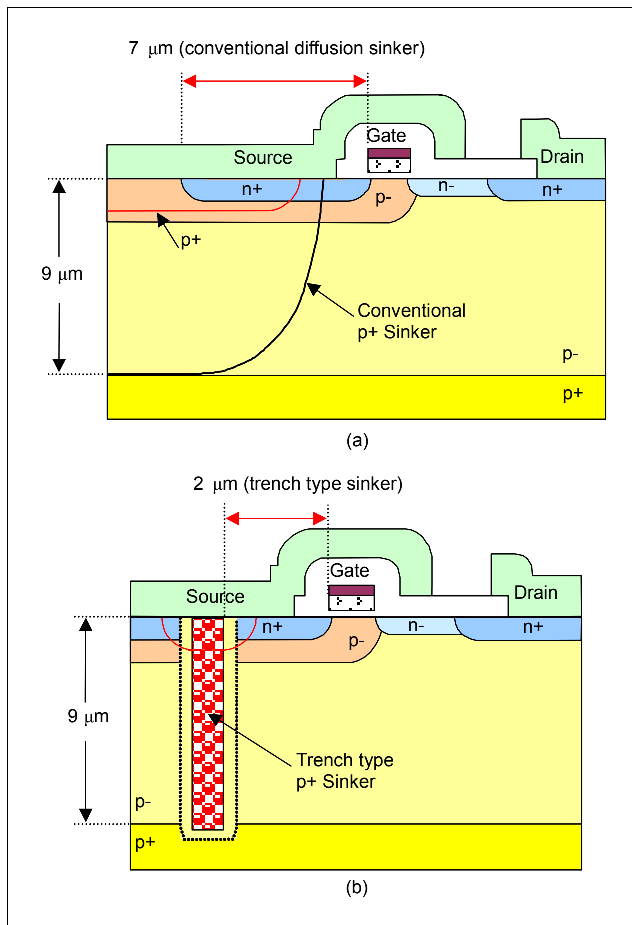

Fig. 1. Comparison of a cross-sectional view of (a) the conventional LDMOS and (b) the Trenched-Sinker LDMOS. The gate edge to the sinker edge space can be reduced from 7 μm to 2 μm by adopting a low temperature trench process.

II. Device Simulation and Design

We used a device simulator in designing the TS-LDMOS structure for transistors in high power base stations. The basic device structure was the conventional 0.5 μm nMOSFET, which uses an asymmetric lightly doped drain (LDD) shape and is a well-known technique for increasing breakdown voltage (BV_{dss}). We fixed the graded channel implantation condition at 4E12 cm^{-2} for a threshold voltage of 2.5 V, and the n-dose of the LDD region at 1E13 cm^{-2} to meet the BV_{dss} specification for more than 65 V. The BV_{dss} depends primarily on the length of the n-region, but with simulations only, we weren't able to predict the exact BV_{dss}. Thus, we designed a group of devices to optimize the n-length of the LDD region. The entire gate of the TS-LDMOS was shielded and grounded by source metal to increase the BV_{dss} by reducing the electric field of the drain as shown in Fig. 1 [2]. Figure 2 shows the simulated results of the electric field contour and the current and voltage (I_{ds}-V_{ds}) characteristics of the TS-LDMOS device that was processed with the final device fabrication conditions.

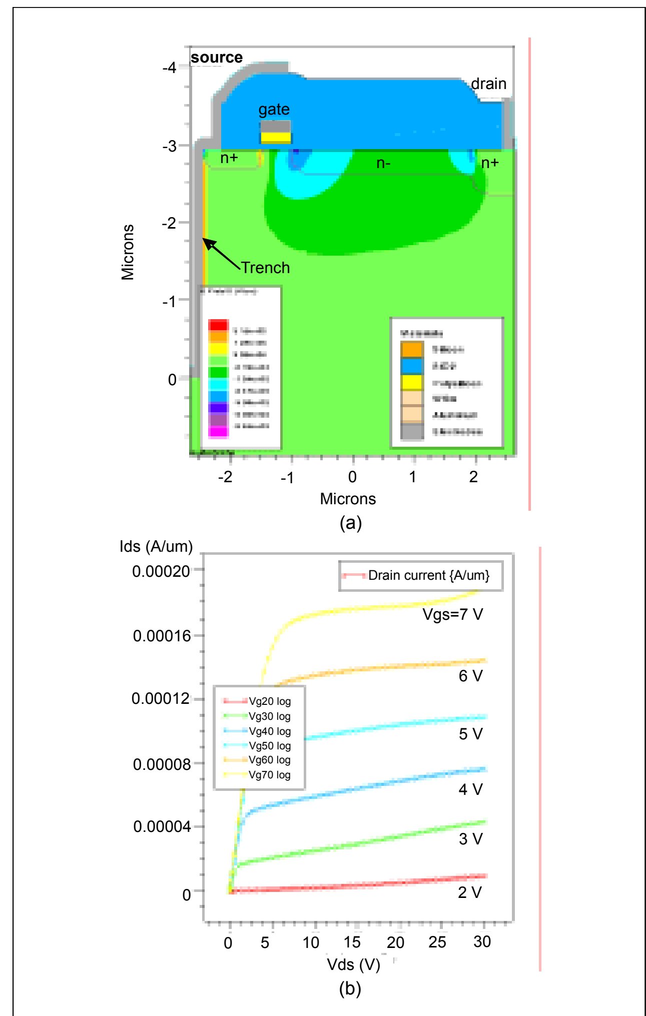

Fig. 2. Simulated results of the TS-LDMOS for a breakdown voltage (BV_{dss}) larger than 65 V and a threshold voltage of 2.5 V: (a) electric field contour at V_{ds}=30 V, V_{gs}=7 V, (b) V_{ds}-I_{ds} characteristics (V_{gs}=2, 3, 4, 5, 6, 7 V).

We designed various kinds of devices to characterize the DC and RF performances and large width devices to evaluate the RF gain and power performance. The expected channel width of the TS-LDMOS for a 30-dBm and 36-dBm output power was 5 mm and 20 mm, respectively. Several spiral inductors with trenched-sinker guard rings were also included to evaluate the coupling suppression effect of the trenched sinker.

III. Device Fabrication

The fabrication of the TS-LDMOS followed the conventional nMOSFET fabrication process after we had etched the trenched sinker and refilled it with doped polysilicon. The starting material was a (100) orientation substrate with a resistivity of 0.01 Ω-cm, and a lightly doped epitaxial layer of 9 μm. First we created a low resistance source sinker on the backside by trenching the substrate to a narrow width of 1 μm and a depth of about 10 μm; then we filled the trenched sinker with p+ doped polysilicon and plannarized it by an etch-back process. A gate oxide of 70 nm was thermally grown after the field oxide growth. Tungsten silicide was deposited on the polysilicon gate to reduce gate resistance. A graded channel was formed by the lateral diffusion of boron ions that had been implanted self-aligned to the gate, and the diffusion time was controlled to prevent lateral diffusion of the heavily doped sinker. We defined an asymmetric LDD region by adding a mask after forming a sidewall spacer.

After making two layers of aluminum metallization, we thinned the wafer backside and applied gold metallization to assure a sink with good electrical and thermal characteristics. We attached sliced chips to the metallic package for sinking the thermal flow and bonded multi-wires to sustain a high current flow over 500 mA. Figure 3(a) shows a cross-sectional scanning electron microscope view of the fabricated TS-LDMOS. The trenched sinker and gate electrode shielded by source metal is clearly seen. Figure 3(b) is a photograph of the chip and package of the TS-LDMOS for a 4-W output power.

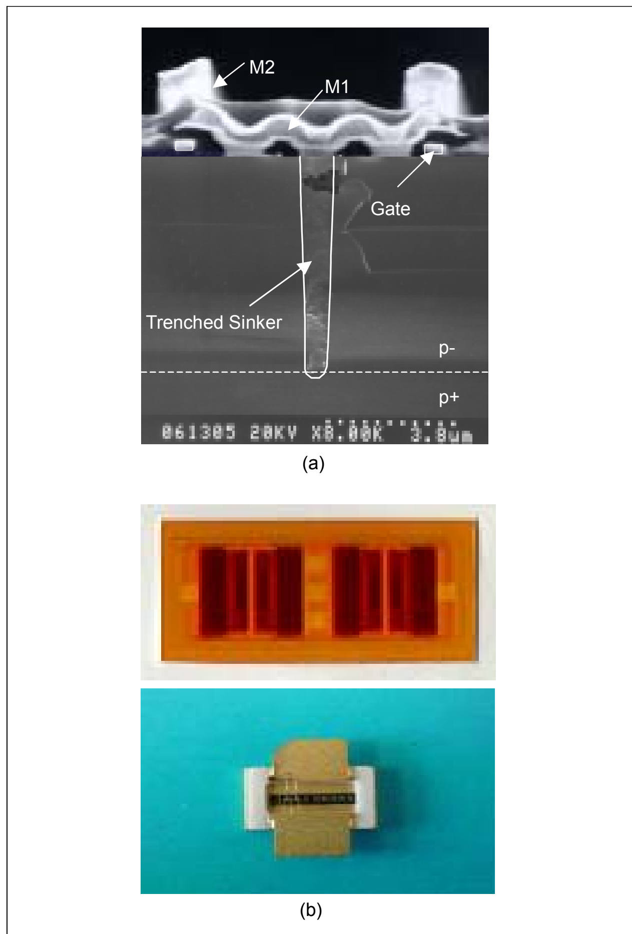

Fig. 3. (a) A cross-sectional SEM view of the fabricated TS-LDMOS, (b) a chip and package photograph of the TS-LDMOS for a 4-W output power at 2 GHz.

IV. TS-LDMOS Performance

We measured the DC performance with a parameter analyzer and the S-parameter with an HP8510 network analyzer. We also measured the power and efficiency using a load-pull setup. Figure 4 shows the measured BV_{dss} of the TS-LDMOS with various LDD n-extension lengths; the results reveal that an n-length longer than 2.7 μm is required for a BV_{dss} larger than 65 V. To improve the BV_{dss}, we experimented to optimize the extension length of the source metal over the

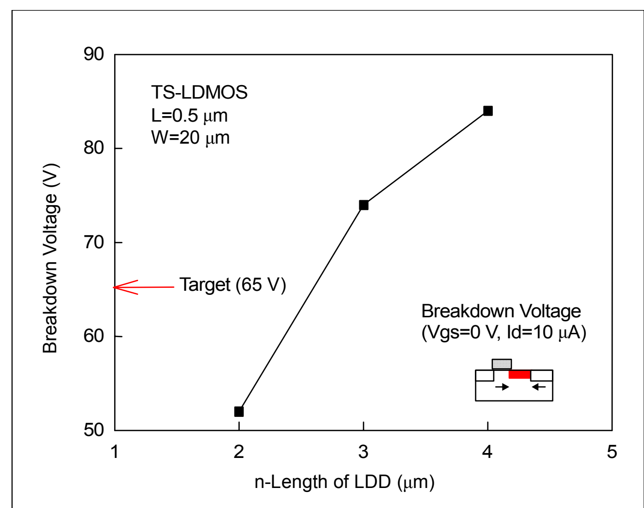

Fig. 4. Breakdown voltage (BV_{dss}) of the TS-LDMOS with various LDD lengths.

gate electrode (gate field shield). When the source electrode fully shielded the gate, the BV_{dss} showed about a 7% improvement over the non-shielded gate, but when the gate was overshielded, the BV_{dss} was about 12% lower (Fig. 5(a)). These results were consistent with the simulated results that also showed that the shielded gate device had a much lower electric field in the drain region than the nonshielded TS-LDMOS (Fig. 5(b)).

Figure 6 shows the measured I-V characteristics of the TS-LDMOS fabricated with the final fixed conditions. The graded channel and n-region implant dose were 4E12 cm^{-2} and 1E13 cm^{-2}, respectively; the n-length was 3 μm and the gate had a fully shielded layout. It showed a threshold voltage of 2.5 V, a transconductance of 0.27 S/cm, and a BV_{dss} of 77 V.

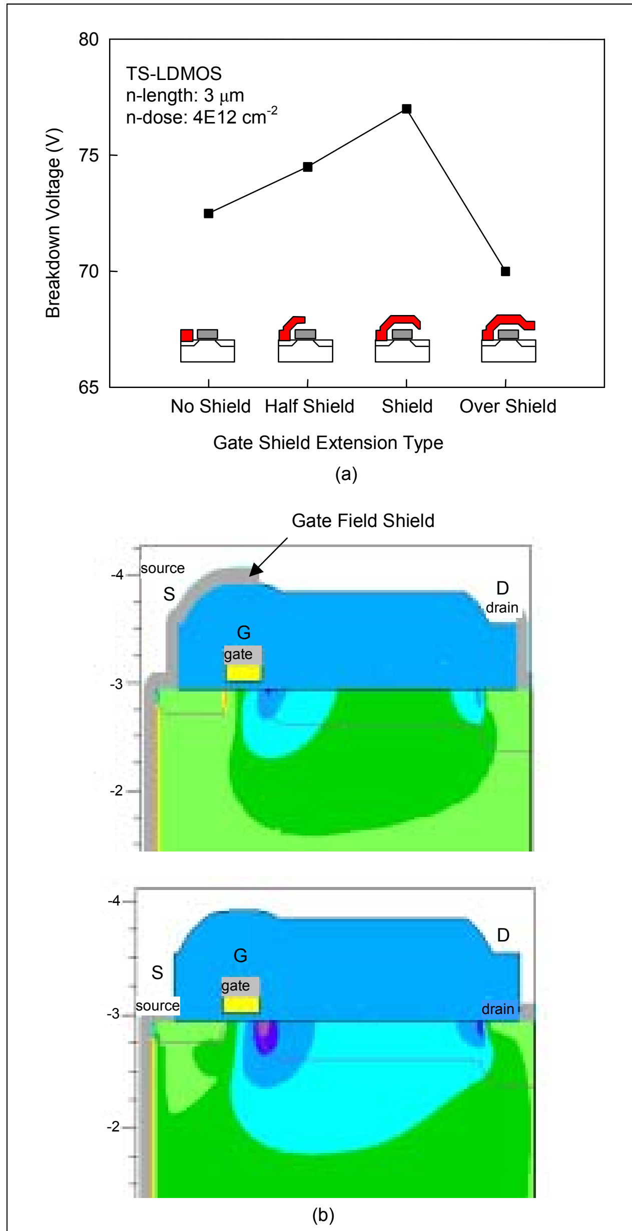

Fig. 5. (a) Breakdown voltage (BV_{dss}) and (b) the simulated electric field contour, with variations of the gate field shield metal structure. The gate-shielded device showed a lower electric field at the drain than the nonshielded device.

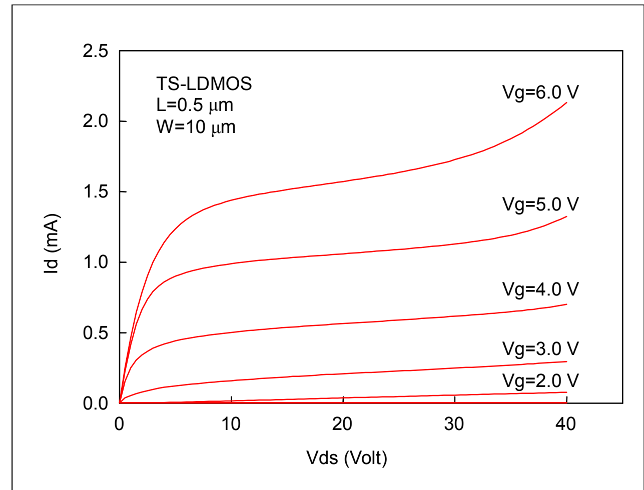

Fig. 6. Drain current characteristics of the TS-LDMOS with a channel length of 0.5 μm and a width of 20 μm.

To maximize the RF performance of the device, optimizing the unit finger width (W_u) was crucial because the gate resistance and parasitic capacitance of the device govern the RF performance [10], [11]. For a large width device, a large W_u is best for reducing the finger number, and thereby producing a compact chip size. In this way, the parasitic capacitance, mainly due to junction and interconnection, can be reduced by increasing the W_u, but the gate resistance also increases and results in degradation of the maximum oscillation frequency (f_{max}). To prevent the increase in gate resistance with a large W_u, we strapped the silicide gate with a second metal [5], [6], and its effect is clearly seen in Fig. 7. The metal-strapped gate structure showed a 2 to 3 GHz higher f_{max} than the conventional silicide gate, and it also showed that W_u can be enlarged up to 200 μm without significant degradation of the f_{max}. All the metal-strapped devices, even when the W_u varied from 100 μm to 200 μm, showed a uniform gain of 16.5 dB at 2 GHz due to their low gate resistance, but only the silicide gate device showed a strong dependency on the W_u.

We measured on-wafer and package power performances of the devices by a load pull setup at 2 GHz. Figure 8 shows the gain, power, and power added efficiency (PAE) of 5 mm devices, which were designed for a maximum power (P_{max}) of 30 dBm. The source and load impedance for the P_{max} was 60+j27 and 57+j60, respectively. There was a large signal gain of 11 to 13 dB with the various

values of W_u, and the device designed with a W_u of 200 µm showed the highest P_{max} at 32 dBm and a PAE of 25% due to the small chip size and comparable gate resistance. These results confirm that the proposed TS-LDMOS should be a suitable device structure for the next generation high RF power transistor.

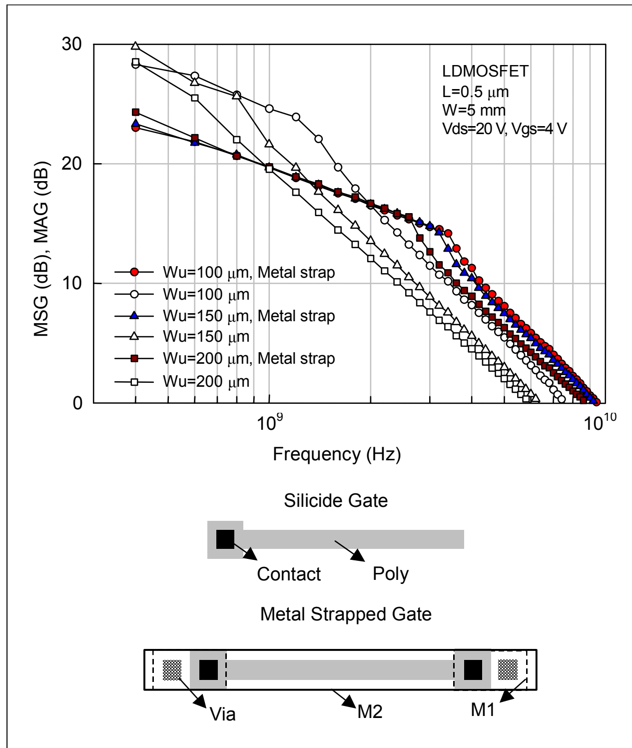

Fig. 7. RF characteristics (on-wafer status) of several TS-LDMOS devices with various unit gate lengths and structures. The metal strap denotes that the silicide gate is strapped at the 50-µm step by a second metal.

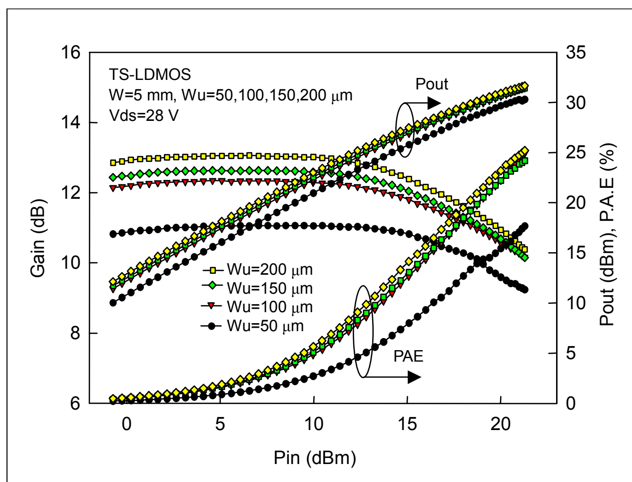

Fig. 8. On-wafer measured power performance of the TS-LDMOS with a total channel width of 5 mm. All the devices were measured at a frequency of 2 GHz and a bias condition of 120 mA.

Figure 9 shows the gain and power performance of 20 mm devices with the various bias conditions. A 400 mA drain current showed a large signal gain of 8.3 dB and a P_{max} of more than 30 dBm. We expected that the P_{max} would be much higher than 30 dBm, because the gain had not decreased and the output power had not been saturated up to 30 dBm. We ran into difficulty at a measurement input power source limit of about 22 dBm.

We attached sliced chips to a metallic package that had high thermal conductivity and bonded multi-wires to sustain the high current flow.

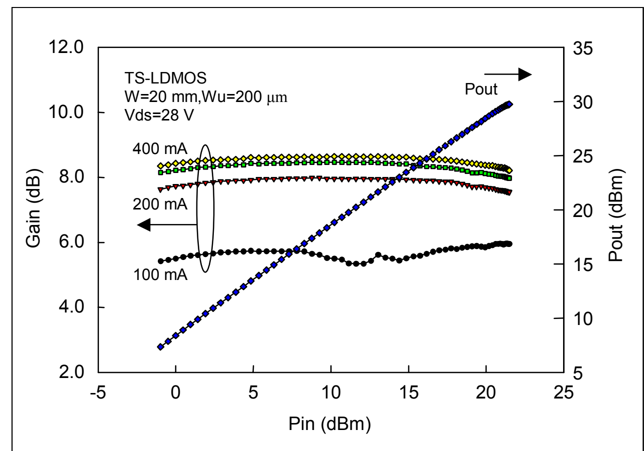

Fig. 9. On-wafer measured power characteristics of the TS-LDMOS with a total channel width of 20 mm.

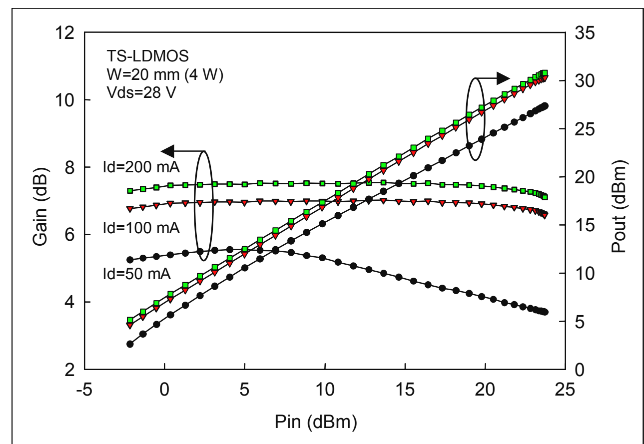

Fig. 10. Measured power characteristics of the 4-W metallic packaged TS-LDMOS. Unlike the on-wafer measurement, at a large bias current of over 200 mA, the device showed an unstable operation, which we expected because of the thermal effect.

Figure 10 shows the gain and power performance of a 20 mm packaged device. The load impedance for the P_{max} was 5.7+j8.9, which was much lower than the on-wafer measurement due to the multi-bonding wire and package

parasitic. As the device size increased, the in/out impedance of the devices decreased, so it was not easy to determine the optimum load impedance for the P_{max}. At a drain current of 200 mA, the gain was 7.5 dB and the P_{max} was 31 dBm. Unlike the on-wafer measurement, at a large bias current of more than 200 mA, the device showed an unstable operation, which we expected because of the thermal effect. We thought that multiple trench sinkers or a wider sinker would enhance the efficiency of the thermal sink.

V. RF Coupling Suppression of the Trenched Sinker

Because of its high conductivity, a silicon substrate is vulnerable to coupling between inductors and coupling from substrate noise [12]-[15]. Highly integrated silicon RF circuits are also more susceptible to interferences from adjacent devices. Thus, coupling phenomena has been a serious problem in silicon RF ICs. Trenched guards, which are essentially the same as trenched sinkers, have been used to block the coupling between inductors or the cross talk between adjacent devices and circuits [15]. We fitted a trenched sinker around the spiral inductors and grounded it to suppress the coupling between inductors (Fig. 11). We also measured the S-parameter of the inductor pairs and the degree of coupling was indicated by the amplitude of the S_{21} parameter for the pattern.

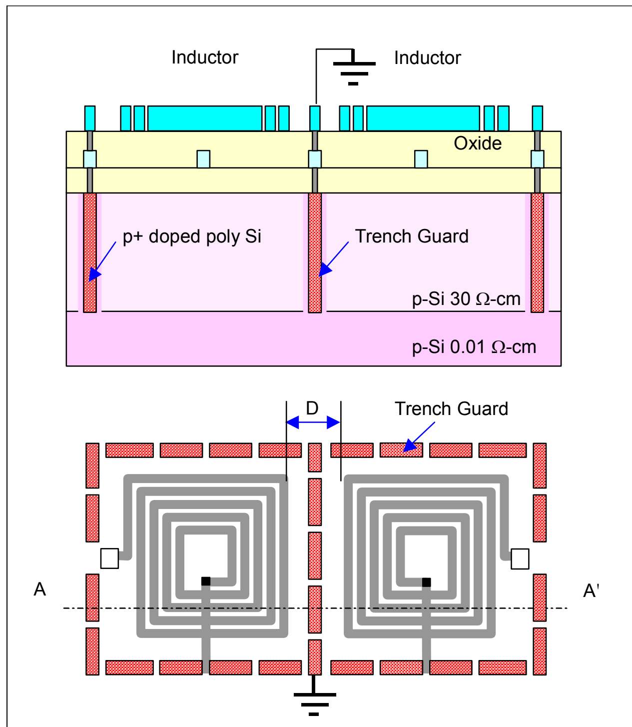

Fig. 11. Cross-sectional and top view of the trenched guard design to evaluate the coupling suppression effects. Each inductor has a 60 μm inner diameter and an 8-turn with an inductance of 13 nH.

Figure 12 shows the measured S_{21} of the inductor pairs with the trenched guard around the inductors as well as the measurements for inductors with a diffusion guard and no guard. The test structures had identical geometries except for the guard ring. The comparison clearly showed that the trench with the guard ring could block coupling from below –40 dB up to 20 GHz. Compared with published deep-well technology [9], which was not investigated at a frequency above 3 GHz, our device showed superior performance at a high frequency. Furthermore, the diffusion guard showed a negligible effect in suppressing inductor coupling. These results suggest that the trenched guard will be an effective technology for blocking inductor coupling and signal interference from adjacent devices or circuits in RF ICs.

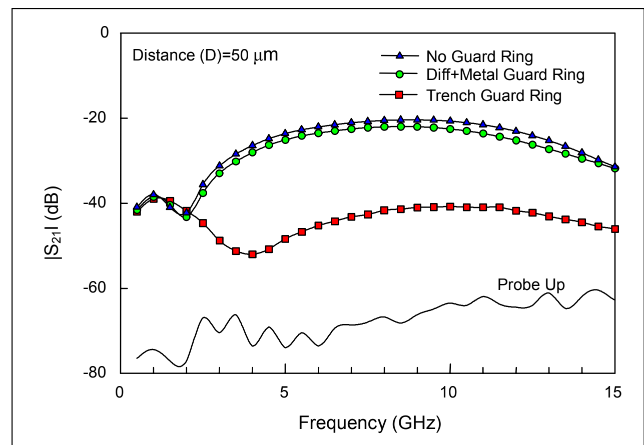

Fig. 12. S_{21} measurements of the inductor pairs with a trenched guard around the inductors compared with inductors with a diffusion guard or no guard. The test structures had identical geometries except for the guard ring.

To apply our new structure to the conventional CMOS technology, which usually does not use the epi-substrate due to its high cost, we applied the trench guard technology to a conventional substrate and varied the trench depth to determine the optimal trench depth for efficient blocking performance. Figure 13 shows the S_{21} measurements of the inductor pairs with trenched guards at various trench depths on a conventional silicon substrate. The inductor coupling was suppressed below –30 dB when the trench depth was about 3 μm, but the coupling was not suppressed further by only increasing the trench depth up to 15 μm. The figure also suggests that the bottom plate of the grounding cage played an important role in blocking the coupling between inductors [16].

These results confirmed that the proposed trenched sinker technology on a high conductivity epi-substrate will be a good

solution to blocking the coupling between inductors and the cross talk from adjacent circuit blocks in mixed-signal RF ICs.

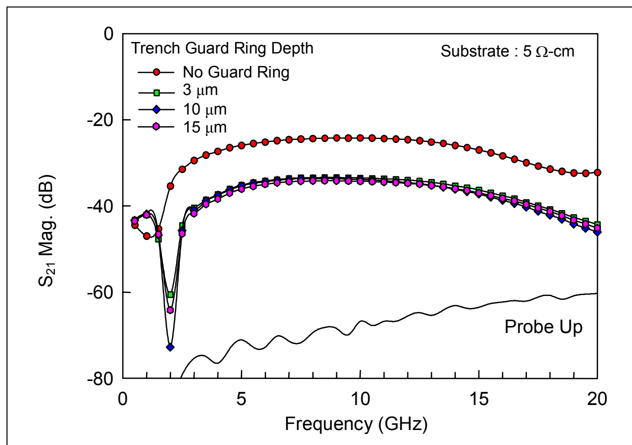

Fig. 13. S_{21} measurements of the trench guarded inductor pairs on a conventional silicon substrate with various trench depths.

VI. Conclusions

The proposed TS-LDMOS was easily and successfully implemented using 0.5 μm NMOSFET technology followed by a low temperature trench process. The measured DC performance of the device showed a BV_{dss} of 77V and a Gm of 0.27 S/cm, and the AC performance of the device with a channel width of 5 mm showed a gain of 16.5 dB, and a P_{max} of 32 dBm at 2 GHz.

We also used the trenched sinker technology on inductor guards to suppress coupling, and it showed an excellent blocking performance below –40 dB at a frequency range of up to 20 GHz.

These results confirm that the proposed trenched sinker should be an effective technology both as a compact sinker for RF power devices and as a guard ring against coupling.

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