Low Power 260k Color TFT LCD Driver IC

Bo-Sung Kim, Jae-Su Ko, Won-Hyo Lee, Kyoung-Won Park, and Soon-Yang Hong

In this study, we present a 260k color TFT LCD driver chip set that consumes only 5 mW in the module, which has exceptionally low power consumption. To reduce power consumption, we used many power-lowering schemes in the logic and analog design. A driver IC for LCDs has a built-in graphic SRAM. Besides write and read operations, the graphic SRAM has a scan operation that is similar to the read operation of one row-line, which is displayed on one line in an LCD panel. Currently, the embedded graphic memory is implemented by an 8-transistor leaf cell and a 6-transistor leaf cell. We propose an efficient scan method for a 6-transistor embedded graphic memory that is greatly improved over previous methods. The proposed method is implemented in a 0.22 μm process. We demonstrate the efficacy of the proposed method by measuring and comparing the current consumption of chips with and without our proposed scheme.

Keywords: LCD driver, graphic memory, low power.

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Bo-Sung Kim (Phone: +82 2 538 9171 ext. 308, email: kdream@tomatolsi.com), Jae-Su Ko (email: fortune@tomatolsi.com), Won-Hyo Lee (email: ilchui@tomatolsi.com), Kyoung-Won Park (email: knight@tomatolsi.com), and Soon-Yang Hong (email: justin@tomatolsi.com) are with the TomatoLSI Company, Seoul, Korea.

I. Introduction

Current telecommunication technology has improved amazingly. These improvements have revitalized hand-held modules and increased services. Because of this, it is even more important that the chip enable voice communication, data, graphic images, and moving pictures. To use a hand-held module for a longer time, each chip needs to become smaller and consume less power.

Improvements in telecommunications have made display technology improve too. The size of display equipment has become bigger and the resolution higher. Due to this, power consumption of display equipment has also become higher. Power reduction for display equipment has become a very important issue. The display equipment in hand-held phones is super twisted nematic (STN) and thin film transistor (TFT) LCDs. Electro-luminescence will be a practical utility.

Display material can have an altered arrangement according to the level of voltage or the amount of current. In accordance with the arrangement, the rate of a transmission changes. We can control the brightness of a display panel, and the black/white display panel is implemented with this method. The multi-color display panel is implemented by arranging an RGB color filter. The color rectangular panel is supplied by row-direct voltage and column-direct voltage. The difference of the two direct voltages is the driving voltage of the pixels. This method is called multiplex addressing. The LCD driver IC generates and supplies the voltage level.

This paper presents a 260k color TFT LCD driver module that consists of a gate driver and source driver. The gate driver generates the driving voltage of column direction and common voltage.

Figure 1 shows how the TFT array is constructed. The gate driving voltage is of two types: a selected level and a non-selected level. The level of these voltages is determined by the characteristics of each panel. When one gate line is selected,

the source IC drives data voltage levels that are valued by decoding stored data. The different voltage of the gate's selected level and source's data level determine the display material arrangement.

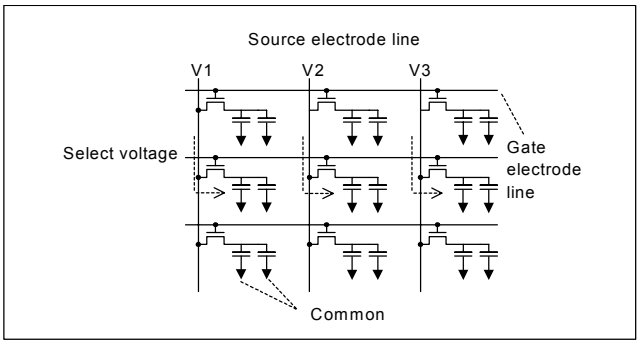

Fig. 1. TFT array.

Currently, the LCD panel is implemented in mono, 4-gray, 256-color, 65k color, and 260k color for hand-held phones. With a higher color resolution, the embedded memory capacity needs to be bigger in the LCD driver IC. With a larger memory capacity, the metal line from the logic part to the memory needs to be longer. Because of this, the embedded graphic memory-addressing block, the embedded graphic memory control block in the logic, and a time control block in the embedded graphic memory becomes more important in designing the embedded graphic memory. The internal control block in the embedded graphic memory is especially important in AC characterization. The power consumption of the merged memory also becomes a very important issue.

With a higher resolution and bigger panel, a bigger embedded memory size is necessary. Because of this, shrinking the RAM size is a dominant factor in the chip size of a driver IC. Because of these factors, the architecture of the embedded memory was improved from an 8-transistor SRAM architecture to a 6-transistor SRAM architecture.

In this paper, section II presents the architecture of the graphic driver IC. Section III discusses the architecture of the 8-transistor/6-transitor embedded graphic SRAM and the architectural defect of the write/read/scan method in 6-transistor architecture. In section IV, a low power scan method in a 6-transistor architecture is proposed. In this chapter, another low power accessed method is proposed. In section V, the implemented two-chip sample is compared in power consumption. The chip samples are implemented in a 0.22 μm process and tested in manual board.

II. Structure of the Driver IC

Generally, the driver IC is composed of a logic part, an analog part, and a memory part. The analog part is composed of the LCD driver, DCDC converter, voltage divider, and oscillator. The oscillator circuit generates a clock for display. The DCDC converter circuit receives the generated clock and generates the highest/lowest voltage level. The voltage divider circuit divides between the highest and lowest level. The driver block supplies the various voltages to the panel, which are generated in the voltage divider circuit.

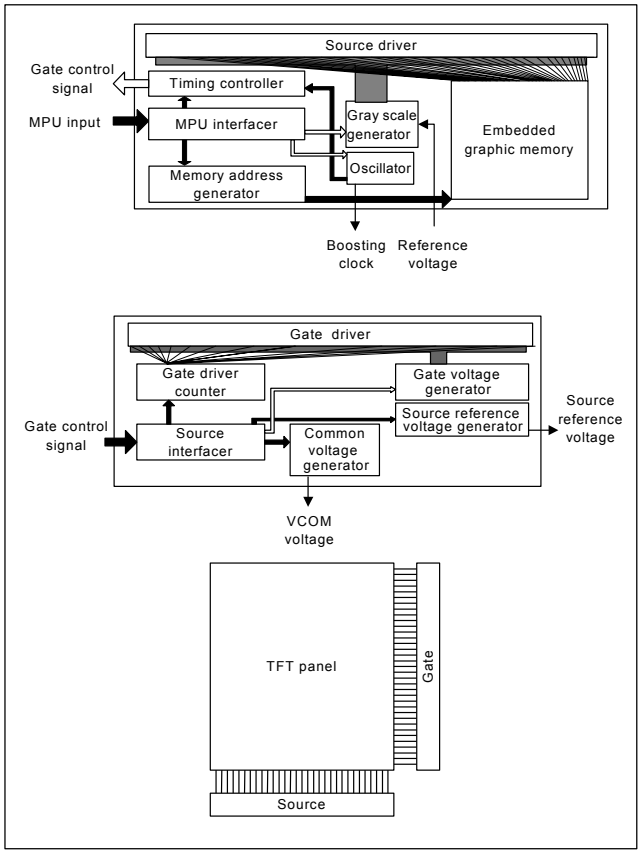

Fig. 2. Driver IC block diagram.

Figure 2 is a block diagram of the implemented 260k color TFT LCD driver IC. The implemented IC is composed of a gate driver IC and a source driver IC.

The source driver IC is composed of a logic, a merged memory, an oscillator, and a driver block. The logic part is composed of an MPU interface block, memory-addressing block, and timing control block. The MPU interface block interfaces between the driver IC and the external MPU. The memory-addressing block receives the decoded signal in the MPU interface and generates the memory address. The resister array is included in the gray scale generator. The implemented driver IC has three types of adjustment: a gradient adjustment, an amplitude adjustment, and a fine adjustment. The timing control block generates a signal, which controls the display

panel. The control signal of the panel transfers a synchronous signal for the gate IC.

The gate IC receives a panel control signal from the source IC and drives the gate on/off level voltage (VGH/VGOF), common level voltage (VCOM), and the source reference-voltage of a gray-scale (VGMA). The gate IC sequentially generates the different voltages in order to reduce power consumption of the DCDC converter (Fig. 3).

The TFT panel must have a capacitor for storage. The driving method is a two-type per capacitor connection that is named the capacitor for storage in a TFT panel (CST) on the gate and the CST on the common (Fig. 4).

The embedded memory is the same as normal memory. In addition, the embedded memory has the operation of accessing whole-bit cells in the X-address. The accessed data is received and decoded in source drivers. The source driver drives the panel with the voltage level, which is decoded by the accessed data. One time, the gate driver circuit selects one line of the panel. The next time, the gate driver circuit selects the next line, and the embedded memory transmits a whole-bit cell in the next X-address. The gate driver circuit selects a next-column line. With this accessing process, one line of the LCD panel is displayed.

The implemented 260k color TFT driver IC is assembled as in Fig. 5. The source IC is contacted with the panel's chip-on-glass (COG) and the gate IC is connected with the panel's chip-on-film (COF).

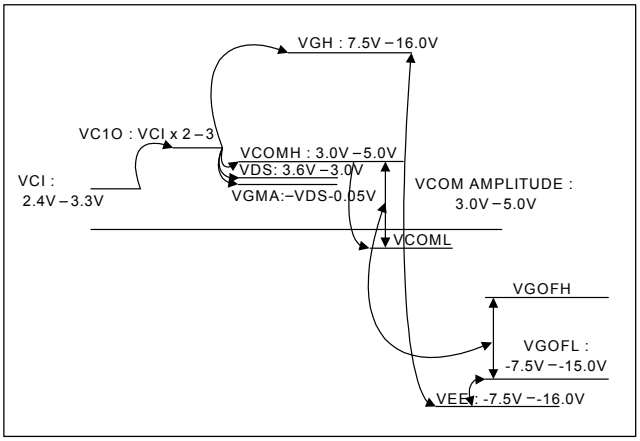

Fig. 3. Sequence of the voltage generator.

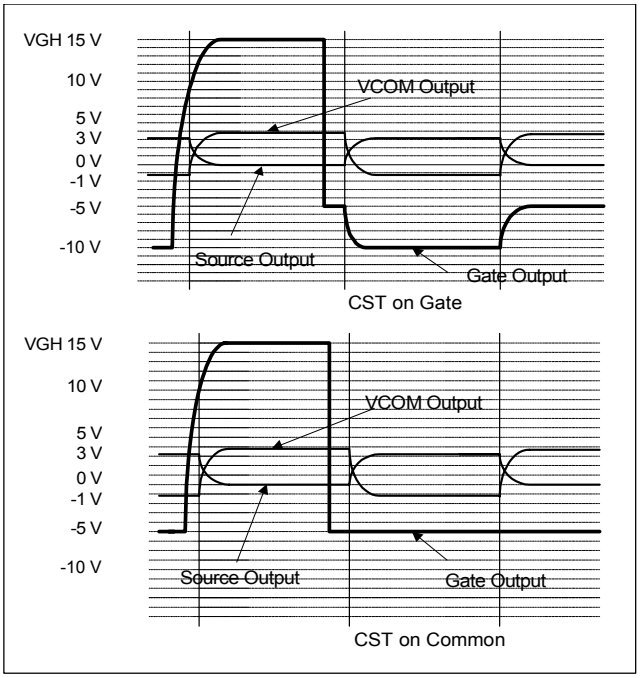

Fig. 4. Two types of CST.

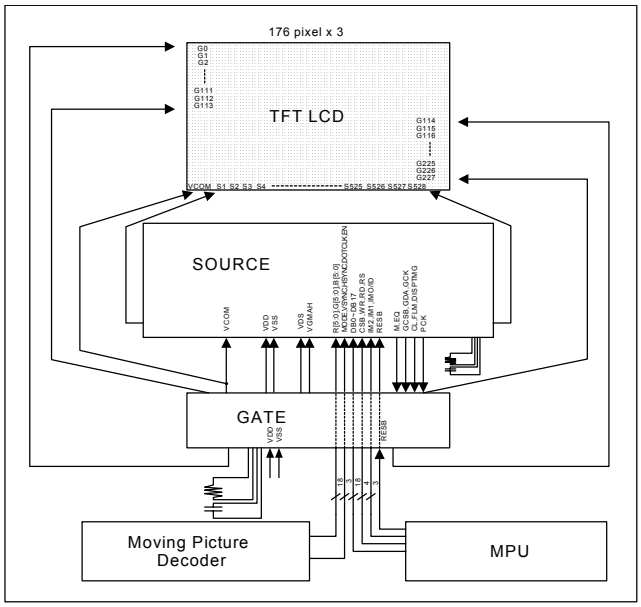

Fig. 5. The proposed chip set module.

III. Structure of Graphic Memory

The embedded graphic SRAM is composed of a bit cell core block, I/O & pre-charge block, a control block, a scan line decoding block, a word-line decoding block, a scan latch block, and several buffer blocks (Fig. 6). The bit core block stores display data. The I/O & pre-charge block controls charging and discharging of the bit/bitb line. The scan/word line-decoding block controls the word-line cell in the bit core block. This block accesses stored data and stores data. The scan-latch block does scan operations.

The control block receives external write/read/scan enable signals from the address-generating block of the logic part and regenerates ram internal signals. The received-origin signal is transferred through a long metal line and the length of the metal

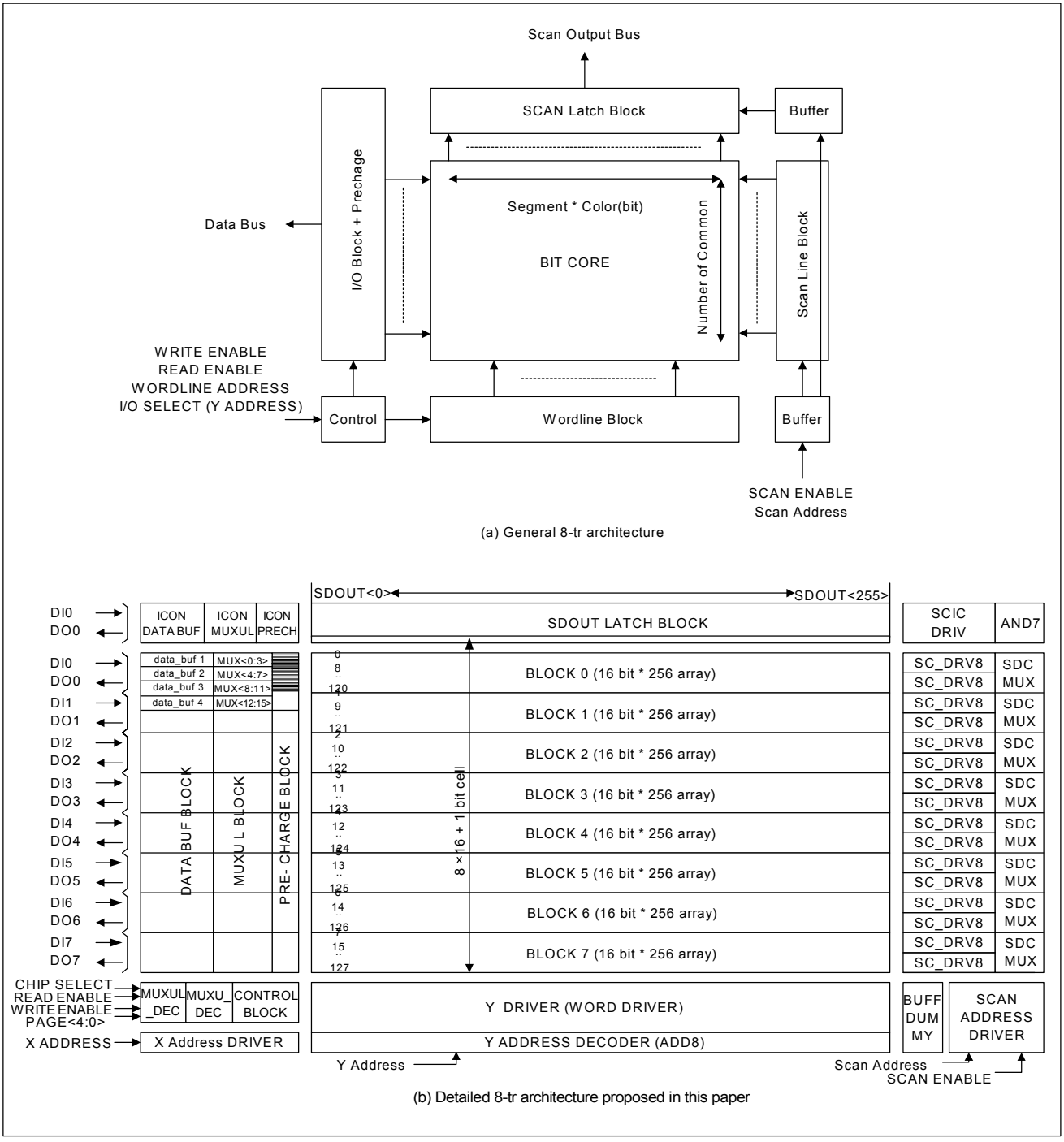

Fig. 6. Graphic memory block diagram.

line differs. Because of this, the write-enable signal of the most left word-line block can have a time gap with the most right word-line block. The slope of the external signal through the long metal line is low and the driven gate of the sloped signal consumes more power. If the origin signal is used without refining the I/O block and word-line block, the operation of the memory is unstable. Because of this instability, as the higher storage memory is embedded, regenerating the timing becomes more important.

The regenerated signal enables the access operation when the bit/bitb line is perfectly stable. The control block has an auto-detect circuit, which detects the bit/bitb stable time.

In the 8-transistor graphic SRAM architecture, the read/write operation is the same as in a normal SRAM. However, a leaf cell has two additional transistors, which directly connect to the

storage path. Because the additional two transistors are connected to the storage cell independently of the bit/bitb line, the 2-transistor can independently access stored data. The additional transistor with a different access path makes it possible to access storage data even though write/read is operating. Because the 8-transistor has an independent scan operation, the memory access logic for the embedded graphic SRAM is simple. However, because of the additional 2-transistor, the chip size is bigger than the 6-transistor graphic SRAM. In a mono STN driver IC and a low-resolution multi-color STN driver, the embedded graphic SRAM size is not dominant in a full chip. As the panel becomes bigger and the resolution higher, the size of the embedded graphic SRAM becomes dominant in the driver IC. Due to this, currently, the 6-transistor embedded graphic SRAM is used in 256/65k/260k color driver ICs.

In a 6-transistor graphic SRAM, the additional 2-transistor is removed. The scan operation is the same as in the read operation, but the select leaf cell is a whole column line of one row. Because the scan operation of the 6-transistor graphic SRAM uses a bit/bitb line, when the write/read operation is in process, the scan operation is prohibited. The RAM accessing logic block must control write/read timing and scan timing. The scan enable signal must be masked and the duration of masking is the writing time. In the writing time, the addressing block must transfer the writing address. When the mask time is removed, the scan signal is transferred and the scan address must be transferred.

The logical time can be a critical time violation and can cause a redundant signal. During the scan operation, the additional sense amplifier operates and the bit/bitb lines are discharged. Because of this, the 6-transistor architecture is inferior in power consumption.

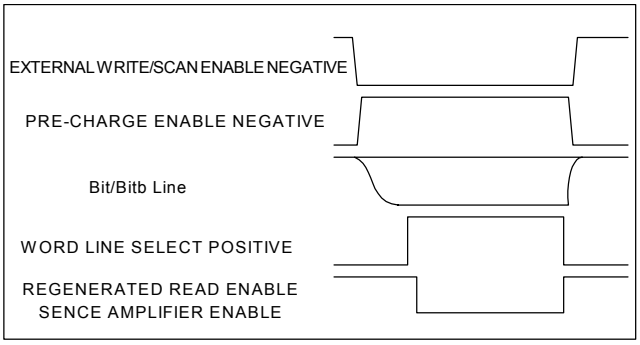

Fig. 7. Normally regenerated memory access signal.

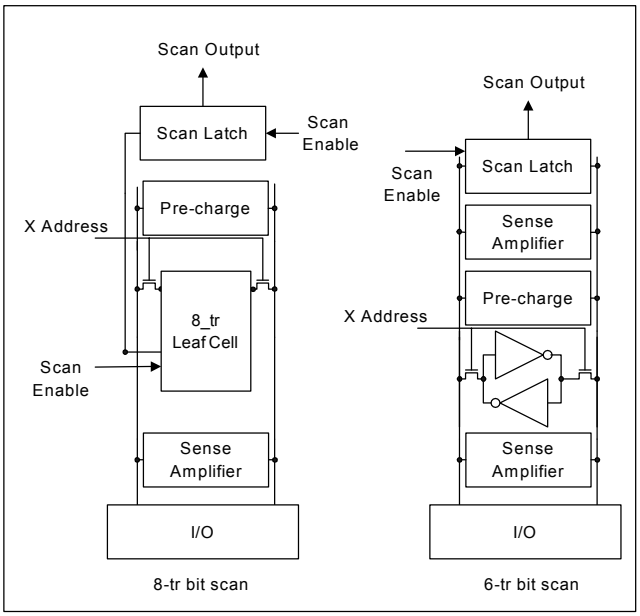

Fig. 8. Comparison of 8-tr scan and 6-tr scan.

IV. Reducing Power Consumption

In a general graphic SRAM, the power consumption of the write operation is overlooked. As the capacity of the graphic SRAM and panel size becomes bigger, the power consumption of graphic SRAM blocks as well as that of analog blocks is an important issue in driver ICs. Because of this power consumption, it is necessary to shorten the graphic SRAM internal transition time. The write-enable signal of the external input of the graphic SRAM generates a word-line signal.

Normally, the signal of the external logic block has a long time period because of the timing margin. The embedded graphic SRAM receives the external signal and regenerates the optimized time signal, which is a shorter select time of the word line than the normal select time. The optimized time is a decision in time that the read/write operation is stable. This means that the bit/bitb has enough of a voltage level gap. If the bit/bitb gap is high, the power consumption is high and the memory operation is stable. If the bit/bitb gap is low, the power consumption is low and the memory operation is likely to be unstable.

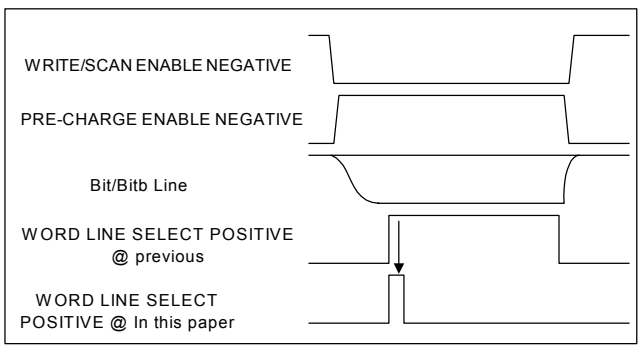

Fig. 9. Shortened word line select positive.

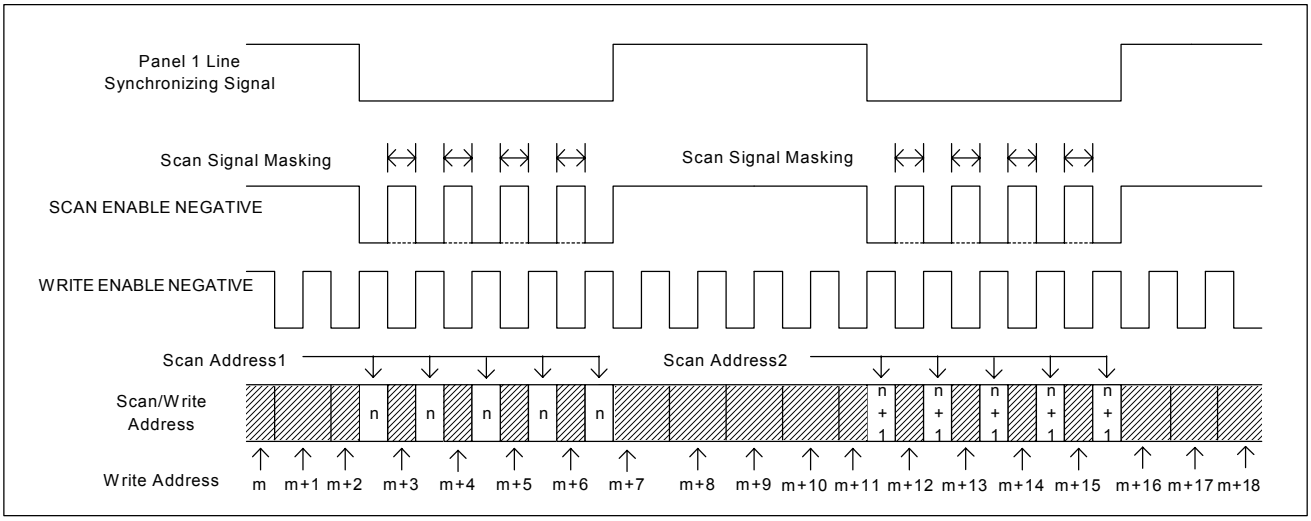

Fig. 10. Scan signal masking.

This method is efficient for reducing power consumption because the open-time of a path from the bit/bitb to the leaf cell is shortened. This method can be used in the scan operation. It can also reduce the time of the sense amplifier operation and word-line select (Fig. 7). In the scan operation of the 6-transistor embedded graphic SRAM, the power consumption is bigger than the 8-transistor graphic SRAM because column-direction connected bit/bitb cells are wholly charge/discharge. The scheme of the regeneration time is necessary in the embedded graphic 6-transister memory.

Normally, the generated clock by an internal oscillator determines the scan clock and the frequency of the scan clock determines the display frame frequency. Because the frame frequency is normally several tens Hz which is a much lower frequency than the writing frequency of a moving picture, if the write and scan signal occur simultaneously, the scan signal must be masked by the writing signal.

Figure 11 describes the masking operation when the scan signal and the writing signal occur concurrently. The write/read address and scan address are independently generated and supplied by the masking signal. While the scan signal is masked, the write signal is applied to the graphic SRAM. The other scan signals, except the first scan signal, access the same data as the first scan data (Fig. 12). This method is not efficient, so we propose removing the redundant scan operation.

Figure 11 also describes the method of removing the scan signal. In case 2, if the second scan signal were removed, the first scan time margin might disappear in the AC characterization in the first scan signal. The scan signal and write signal are not synchronized. Due to this, the first scan signal may be distorted by the writing signal. Thus, the minimum number of the removing scan signal must be 2. Figure 12 presents a diagram of the removing circuit. The

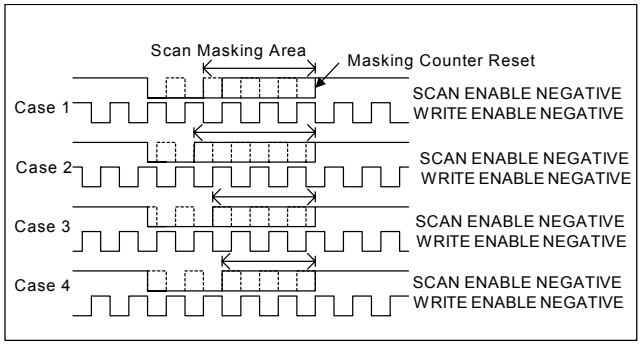

Fig. 11. Redundant scan masking.

independently generated WEN and SEN1 signals are transferred to the masking circuit. The masking circuit generates the same function as previous SEN2 and WEN signals. The scan signal counter circuit counts the SEN2 signal and the counter holds at 3. When the original SEN1 signal is high, the counter returns to 0. The counter waits for the SEN2 signal. At only 1 and 2 counts, the masking enable signal is generated. At 0 and 3, the SEN signal is removed. This method can reduce the redundant toggling scan signal and can deduce the power consumption of redundant toggling.

$$\frac{Scan\_time}{write\_time} = \frac{\dfrac{1}{Fram\_frequency \times Gate\_line/2}}{1/Access\_frequency} = \frac{\left(\dfrac{1}{30 \times 228/2}\right)}{50} = 5847 \quad (1)$$

For example, if the TFT LCD driver IC uses a color panel with a size of 176×228 and the access time is a 20 MHz MPEG interface, the number of writing can be 5847 during the

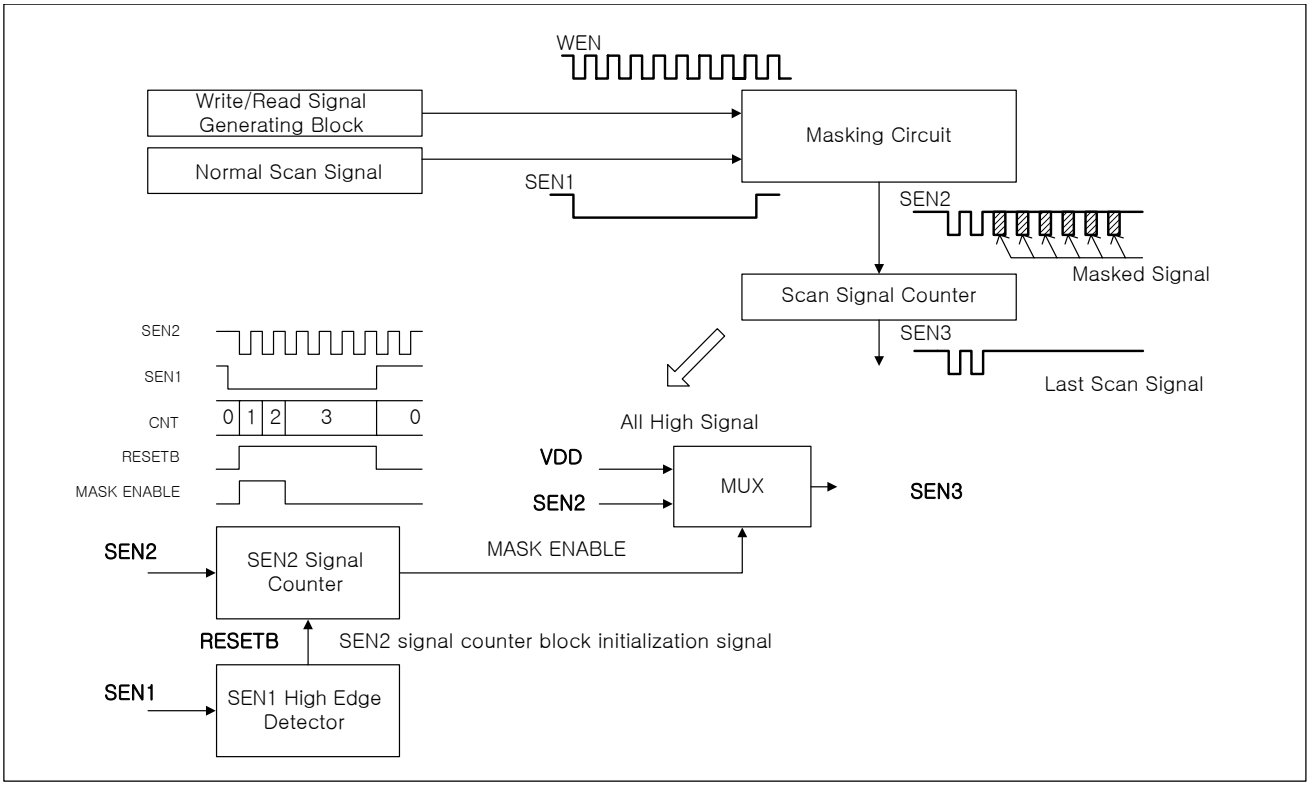

Fig. 12. Removing block diagram.

scan operation as in (1). In (1), as the access time becomes faster, the redundant consumption of power increases. The proposed algorithm for removing the scan signal can remove the redundant power consumption. The proposed algorithm can reduce power consumption by more than 24%. The following section verifies this.

V. Experimental Device

Figure 13 is a photograph of a 260k color small TFT LCD driver IC. The IC is the TFT source driver IC with 528 segment outputs. The chip size is 21700×1950 μm^2. The chip of the previous algorithm and that of the proposed algorithm are fabricated in a 3-metal 0.22 μm process. The center part is the logic block and the both side blocks of the logic block are embedded graphic memory blocks. The oscillator circuit is located in between the logic block and the left memory macro-block. The gray scale block is located in the upper part of the logic block. The driver block is located above each memory macro-block. The four-quarter sides are wrapped by a pad.

Fig. 13. Full chip of a 260k color small TFT driver.

The embedded graphic 722,304-bit memory block is divided by 16 macro-blocks because of the reduced height of the chip. The optimization of the height and length is an important factor in the number of a net-die. Each macro-memory block can be selected by a select signal when the read/write signal is supplied. This method reduces memory access power. Scan operating can be concurrently executed.

The test is accomplished in a Q-tab manual test board. The power consumption is measured at 2.5 V. Figure 15 describes

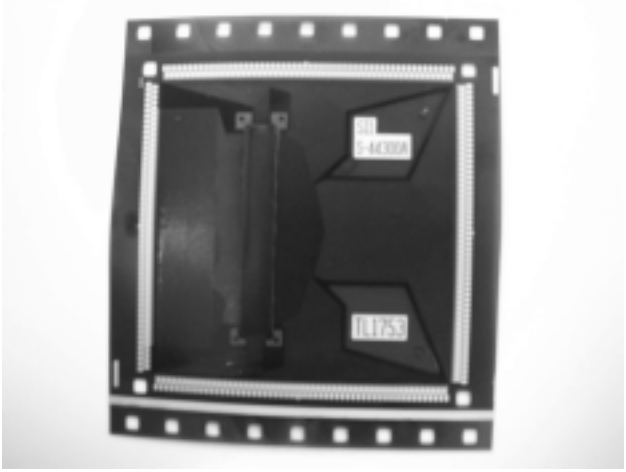

Fig. 14. Q-tab test module.

the consumed current of only the logic part at the writing time. The REV.0 is a normal scan method chip. The REV.1 is the chip with the algorithm for removing the redundant scan.

Figure 15 illustrates that as the access speed increases, so the power consumption increases. In the REV.0 chip, power consumption is 16.6 mA in 4 MHz. In REV.1 chip, power consumption is 6.745 mA. The 59% power consumption of the REV.0 chip is reduced in the REV.1 chip.

Table 1 shows the consumed current in only the logic part at the writing time and the scan time. The writing and scan test is accomplished by a manual board with a PC interface. The write time is supplied in 4 μs, which is the minimum clock in the PC. In one scan enable duration, the total number of the maximum writing is 7, which is the scan method in previous algorithms. In our REV.1 chip, the scan masking method is included. Table 1 shows the consumption of power for various numbers of scans. When the number of the valid scan signal is smaller, the power consumption is lower.

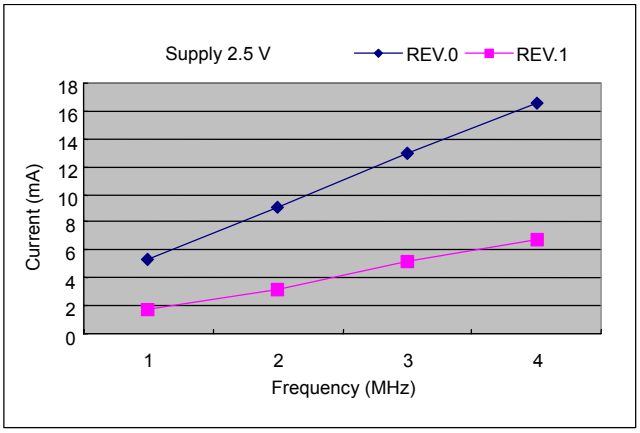

Fig. 15. Comparison of RAM writing current consumption in REV.0 and REV.1.

Table 1. Comparison of writing current consumption by the number of scans.

Number of scans	7	4	3	2
Current (μA)	192 μA	187 μA	167 μA	120 μA

Figure 16 is the module test environment. The basic signal is generated in a PC and the high-speed signal is generated in an FPGA board. Figure 18 is the display data.

VI. Conclusion

Currently, improvement in display resolution and panel size increases power consumption in driver ICs. In this paper, we proposed two methods that reduce the power consumption of access in an embedded graphic SRAM. The first method is a regeneration time method, which receives access signals from the external logic and regenerates the optimum time. This method can be applied in the embedded graphic SRAM. The second method removes the number of redundant scan signals. This method removes the number of redundant accesses and can be applied in a logic block. The efficiency of the proposed method is verified in the 0.22 μm process. The total power consumption in the module is under 5 mW at a 2.4 V supply. Power consumption is measured in a normal display. The module is efficient in handheld equipment.

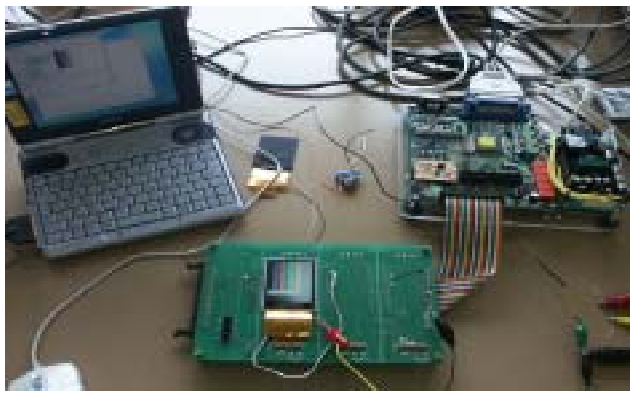

Fig. 16. Module test.

Fig. 17. Module display.

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Bo-Sung Kim received his MS at Sungkyunkwan University in Korea. He studied image processing, voice coding, MPEG2, MPEG4 and memory architecture. He was previously with Samsung's Advanced Institute of Technology where he developed a voice sensing algorithm. He is now a Junior Engineer in TomatoLSI. He has designed a 4-gray STN, a 260k two chip and a 260k TFT one chip.

Jae-Su Ko received his MS at Korea University and BS at Kyung Hee University in Korea. He worked for the R&D division in Samsung Electronics Co., Ltd. from 1995 to 2000. He designed an LCD Driver IC, which is Mono STN LDI, Gray scale STN LDI. He has worked for the R&D division in TomatoLSI Inc. from 2001 to now. He designed an LCD Driver IC which is Mono STN LDI, Gray scale STN LDI, Color STN LDI, Small TFT LDI.

Won-Hyo Lee received his MS at Sungkyunkwan University in Korea. He studied analog design. He has designed a mono STN, 4-gray STN 4096 color one-chip STN and a 260k TFT one chip. He is a Senior Engineer in TomatoLSI.

Kyoung-Won Park is a layout engineer. Previously, he was an engineer in Samsung Electronics Co., Ltd. He is experienced with mono STN, 4096 color STN, and 260k color one chip TFT layout. He is a Senior Engineer in TomatoLSI.

Soon-Yang Hong received MS at Sungkyunkwan University in Korea. He was at the R&D Center in Samsung Electronics Co., Ltd from 1989 to 1995. He was a Junior Engineer (Analog Product Design Development (VCR Signal Processor Y/C 1 Chip)) from 1996 to 1999 at the R&D Center in Samsung Electronics Co., Ltd. He was a Senior Engineer (LDI Product Design Development) in Circuit Design and VCR Signal Processor Luminance LSI design. He designed VCR Signal Processor Chrominance LSI, VCR Signal Processing Y/C 1Chip LSI design, LCD Driver LSI circuit design, Monochrome STN LDI, Gray Scale STN LDI, Color STN LDI, TFT LDI (Large Size, Small Size). He has established (1999.11.5) TomatoLSI, and has been Vice President & CTO.