High Performance RF Passive Integration on a Si Smart Substrate for Wireless Applications

Dong-Wook Kim, In-Ho Jeong, Jong-Soo Lee, and Young-Se Kwon

To achieve cost and size reductions, we developed a low cost manufacturing technology for RF substrates and a high performance passive process technology for RF integrated passive devices (IPDs). The fabricated substrate is a conventional 6˝ Si wafer with a 25 μm thick SiO_2 surface. This substrate showed a very good insertion loss of 0.03 dB/mm at 4 GHz, including the conductive metal loss, with a 50 Ω coplanar transmission line (W=50 μm, G=20 μm). Using benzo cyclo butene (BCB) interlayers and a 10 μm Cu plating process, we made high Q rectangular and circular spiral inductors on Si that had record maximum quality factors of more than 100. The fabricated inductor library showed a maximum quality factor range of 30-120, depending on geometrical parameters and inductance values of 0.35-35 nH. We also fabricated small RF IPDs on a thick oxide Si substrate for use in handheld phone applications, such as antenna switch modules or front end modules, and high-speed wireless LAN applications. The chip sizes of the wafer-level-packaged RF IPDs and wire-bondable RF IPDs were 1.0-1.5 mm^2 and 0.8-1.0 mm^2, respectively. They showed very good insertion loss and RF performances. These substrate and passive process technologies will be widely utilized in hand-held RF modules and systems requiring low cost solutions and strict volumetric efficiencies.

Manuscript received July 11, 2002; revised Dec. 6, 2002.

The authors worked with Telephus Inc., Daejeon, Korea.

Dong-Wook Kim (phone: +82 2 2131 8875, e-mail: xpert.kim@samsung.com) is with S1 Corporation, Seoul, Korea.

In-Ho Jeong (e-mail: ihjeong@telephus.com) is with Telephus Inc., Daejeon, Korea.

Jong-Soo Lee (e-mail: jslee@teltron.com) is with Teltron Inc., Daejeon, Korea.

Young-Se Kwon (e-mail: kwon@ee.kaist.ac.kr) is with KAIST, Daejeon, Korea.

I. INTRODUCTION

The silicon substrate is known to have many benefits—cheap material, good thermal conductivity, stable and mature process technologies—but its uses have been limited to the low frequency region in the fast growing and flourishing wireless market by large signal losses and RF signal leakage due to the conducting substrate and the parasitic substrate capacitance. There have been many attempts to use cheap Si wafers for the RF substrate. These attempts produced a method to control the doping density and give the Si substrate high resistivity in the high frequency region [1], a method to form a 9 μm SiO_2 layer on a Si substrate [2], a method to coat a 10 μm polyimide layer on a Si substrate [3], and so on. None of these approaches provided remarkable benefits in terms of cost effectiveness and microwave performance. The insulating property of a SiO_2 layer on a high conductive Si substrate is usually used for isolation, and effective operation of this SiO_2 layer in RF applications requires it to be thick so that it can isolate the underlying Si substrate capacitively. To reduce fabrication cost and decrease the time needed to grow thick oxide, a new method is required. Porous silicon techniques offer a potential solution. Such techniques electrochemically remove a large number of atoms from the lattice of the porous material, producing a honeycomb-like structure. Initial work applying a porous technique to RF applications took advantage of the oxidation process of the porous silicon layer [4]. More recently, the highly insulating property of porous silicon was used to alleviate the stresses generated as a result of the difference in thermal expansion coefficients of the oxidized porous layer and the Si substrate [5]. All these studies were done in university laboratories and they did not fully optimize their RF performances, partially

because the front side process could not support a high quality RF substrate.

This paper proposes a mass-producible 6″ Si substrate with a 25 μm oxide thickness for RF applications. We call this RF substrate a smart substrate, though previous studies used terms such as selectively oxidized porous silicon (SOPS) or OPS [4]. We also introduce a high performance passive process using Cu metal layers and benzo cyclo butene (BCB) interlayers to make the most of the high quality substrate. Compared to the conventional Al or Au process, our manufacturing process has a lower cost and higher performance. With both the substrate technology and the passive process technology, we fabricated high Q inductors and several IPDs, including a diplexer. We demonstrate their measured RF performances and discuss the co-integration of small sized RF IPDs and surface acoustic wave (SAW) filters.

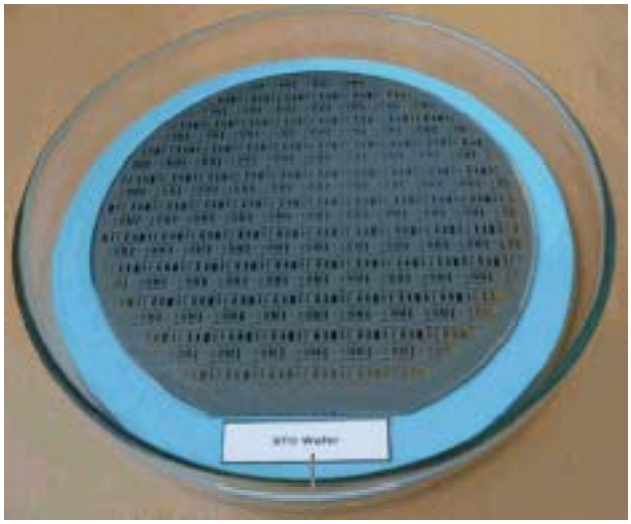

Fig. 1. A photograph of a 6″ Si smart substrate with a selective thick oxide definition.

II. SILICON SMART SUBSTRATE AND RF PASSIVE MANUFACTURING PROCESS

Silicon is the most stable and reliable semiconductor material in the world and has been used in many electronic applications. Unlike semi-insulating GaAs or InP, silicon has typically been forced to rely upon the insulating properties of SiO_2 for isolation. A thin SiO_2 layer cannot capacitively isolate devices on a Si substrate. In addition, the conductive signal loss of a conventional Si substrate with a thin SiO_2 layer is greater than that of GaAs. These factors make it difficult to use Si technology for RF applications. To overcome these limitations, we formed a very thick oxide layer on top of Si [6]-[8]. The reproducible and reliable oxide thickness was 25 μm, and the available maximum thickness was 35 μm. It takes very little time to make the thick oxide layer, and that lowers the manufacturing cost. This smart substrate is an RF substrate that can enjoy the full benefits of the Si material.

A uniform oxide layer of 25 μm or greater can be made on the whole surface of a 6″ silicon wafer. The thick oxide layer can also be manufactured selectively through a thin dielectric masking process. Figure 1 shows the smart substrate with selective thick oxide patterns. This substrate is very flat (surface roughness ≤ 18Å), flat enough to make a fine feature of 1 μm. The record oxide thickness and the processing time lead to a revolutionary low loss and low cost solution for the RF thin film substrate. The real processing time is typically less than 2 hours, and even though accompanying processes are needed, the total processing time is still less than 12 hours. The 25 μm thick oxide layer is formed with a control of ±2 μm over the whole wafer.

To take full advantage of the low loss characteristics of the Si smart substrate, we developed a passive integration process using Cu metallization and BCB interlayers. Cu metal is the optimal choice for low conductive metal loss and high-speed operations. A 10 μm Cu plating process was used for a low loss inductor fabrication and interconnection. NiCr was used for a precision resistor and SiNx dielectric material was employed as an interlayer insulator of metal-insulator-metal (MIM) capacitors. We used a total of three Cu metal layers for the NiCr contacts, the bottom and top metal formations of the MIM capacitors, a spiral inductor patterning, and element interconnections.

Photosensitive BCB materials were used as interlayers between the first Cu metal and the plated Cu metal. Photo-BCB was originally developed for use in microelectronics, such as multichip modules and flat panel displays. We adopted the photo-BCB for our process because it has a lot of attractive properties, such as processing compatibilities with existing IC manufacturing techniques, low moisture uptake, low cure temperature, low dielectric constant, and low RF loss. We used a BCB layer of 5 μm for the interlayer applications and 8 μm for the final passivation layer.

Using the Cu-BCB passive process, the insertion loss of the 50 Ω coplanar transmission line (W=50 μm, G=20 μm) fabricated on a high quality Si smart substrate with a 25 μm oxide thickness was 0.03 dB/mm at 4 GHz, including the conductive metal loss. The transmission line also showed high performance up to more than 10 GHz. The insertion loss was below 0.1 dB/mm up to 15 GHz. This was much superior to the insertion loss of the expensive high resistivity silicon, 7 kΩ-cm substrate. Table 1 shows a comparison of transmission line losses between the results of this work and other research.

Table 1. The insertion loss comparison of transmission lines obtained from results of this work and other researches.

Insertion loss (dB/mm)	Dielectric material & thickness	Signal line metal	Substrate	Ref.
0.17 @4 GHz	SiO_2 (0.9 μm)	Al (1 μm)	HRS (4 KΩ-cm)	IEEE EDL 1991 [9]
0.19 @4 GHz	Polyimide (10 μm)	Al (4 μm)	Silicon (20 Ω-cm)	IEDM 1995 [3]
0.2 @4 GHz	-	Al (1.25 μm)	HRS (10 KΩ-cm)	IEEE MGWL 1999 [10]
0.1 @10 GHz	SiO2 (0.1 μm) Polysilicon (0.6 μm)	Al (1 μm)	HRS (10 KΩ-cm)	IEEE MGWL 1999 [11]
0.05 @4 GHz	-	Au (5 μm)	Pyrex	Exp. Data
0.03 @4 GHz	thick oxide (25 μm)	Cu (10 μm)	Silicon (8 Ω-cm)	This work

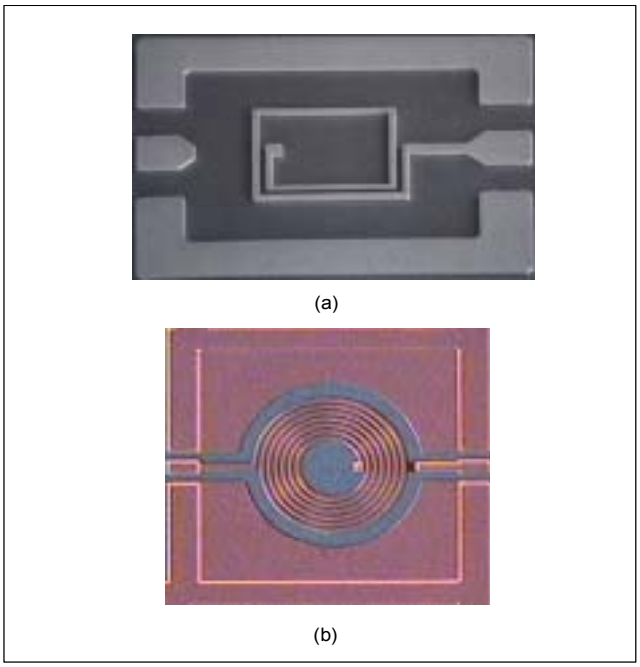

Fig. 2. Photographs of a microstrip-like rectangular spiral inductor and a CPW circular spiral inductor: (a) inner diameter= 200 μm, turns=1.5, W=10 μm, S=10 μm, (b) inner diameter=175 μm, turns=6.5, W=10 μm, S=10 μm.

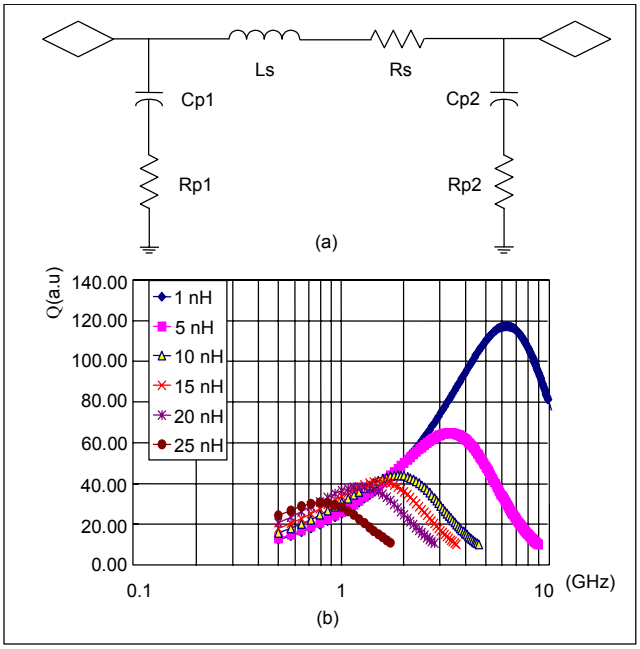

Fig. 3. The equivalent circuit model of a spiral inductor on a Si smart substrate and the frequency dependence of two-port quality factors extracted from the inductor model. The inner diameters (Di) and turn ratios (Nt) of the above inductors are as follows. 1 nH: Di=200 μm, Nt=1.5; 5 nH: Di=225 μm, Nt=3.5; 10 nH: Di=200 μm, Nt=5.5; 15 nH: Di=200 μm, Nt=6.5; 20 nH: Di=200 μm, Nt=7.5; 25 nH: Di=250 μm, Nt=7.5, where the line and spacing of the inductor trace are 10 μm and 10 μm.

III. HIGH QUALITY INDUCTOR AND PASSIVE LIBRARY

Fabricating the on-chip inductors were one of our major technological challenges. We used a 10 μm Cu thickness on a 6″ Si smart substrate with a 25 μm SiO_2 thickness. The fabricated inductors had a 10 μm line width and 10 μm spacing. They showed a maximum quality factor range of 30-120, depending on geometrical parameters and inductance values of 0.35-35 nH. The inductors also showed high quality factors in a broadband frequency range. For example, a Cu circular spiral inductor of 1.05 nH with 1.5 turns had a quality factor of more than 50 up to 16 GHz and a maximum two-port quality factor of about 120 at 7.75 GHz, which is the highest value that has been achieved on an Si wafer. Figure 2 shows photographs of a microstrip-like rectangular spiral inductor and a coplanar waveguide (CPW) circular spiral inductor with multi-turns on a Si smart substrate.

We measured 96 rectangular spiral inductors (microstrip-like) and 72 circular spiral inductors (CPW structures) and established an inductor library for them. Figure 3 shows the equivalent circuit model of the spiral inductor made on a Si smart substrate and the frequency dependence of the two-port quality factor estimated from the extracted model. The model includes shunt series resistor capacitor (RC) networks at both the inner and outer sides of the inductor. The shunt R expresses the conducting nature of the Si substrate underneath the thick SiO_2 layer. As the two-port quality factor is highly difficult to

measure directly, we extracted it from the equivalent circuit model that we accurately fitted to the measured data. Before modeling, we deembedded the parasitic effects with various dummy open-pad patterns. The model in Fig. 3 has a somewhat degraded accuracy in the narrow band because it is simple and fitted in the wide band region for expressing broadband measured data. The high order model, including the substrate leakage resistor and the parallel RC network instead of the resistor in the shunt network, is much better fitted to the measured data and has a better accuracy in a narrow band as well as a wide band. We are currently working on the deembedding procedure of the high-order inductor model and will soon report on it.

Figure 4 shows the maximum quality factor distribution of the microstrip-like rectangular spiral and the CPW circular spiral inductors with the inductance value and geometry variation. As the figure shows, for inductance values less than 10 nH, which are the values commonly used in RF integrated circuits (RFICs), the maximum quality factors are more than 40. Different geometry factors lead to different frequency characteristics and quality factor performances, although they have similar inductance values.

This substrate technology and high Q inductor technology have the potential to push Si applications well into the 10 GHz range and also to broaden the area of IPDs up to 10 GHz or above.

IV. SILICON INTEGRATED PASSIVE DEVICES FOR WIRELESS APPLICATIONS

MIM capacitors and thin film NiCr resistors for RF applications can also be integrated on Si smart substrates, because of their extremely flat surfaces. Using high quality passive devices, we fabricated a small-size low pass filter, a diplexer for antenna switch module (ASM) and front end module (FEM) applications, a wideband balun and a power combiner for high-speed wireless LAN and global system for mobile (GSM)/digital cordless system (DCS) mini base station applications. These devices could be wafer-level-packaged using PbSn solder ball bumping with 170 μm or 300 μm diameters for ultra small form factor devices or be finished with Ni/Au metallization for multi-chip modules.

Figure 5 shows a photograph and the measured data of an 1800 MHz low pass filter for the DCS Tx mode operation of the ASM and FEM modules. A low insertion loss of 0.36 dB and a high harmonic attenuation of more than 30 dB were

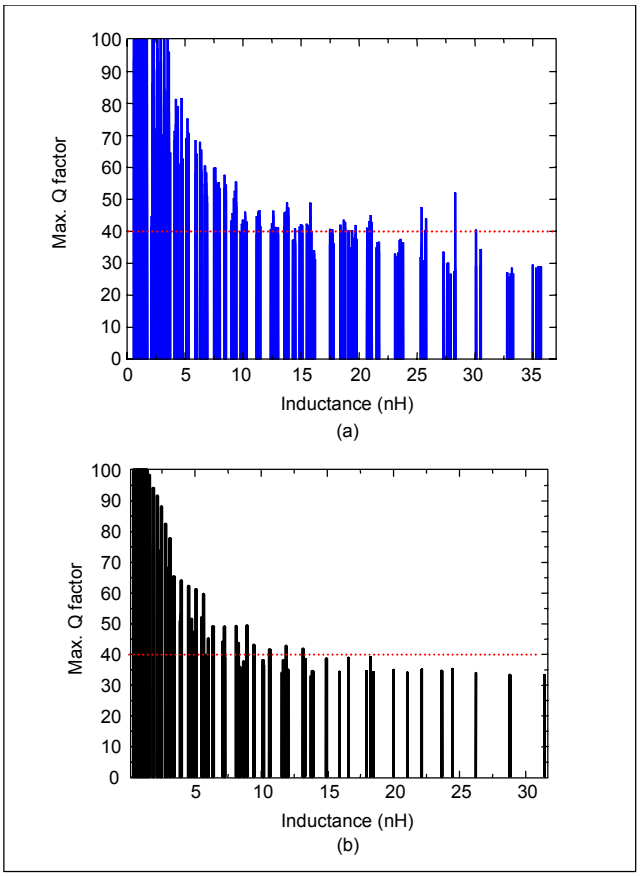

Fig. 4. Maximum quality factor distribution of (a) rectangular, (b) circular spiral inductors.

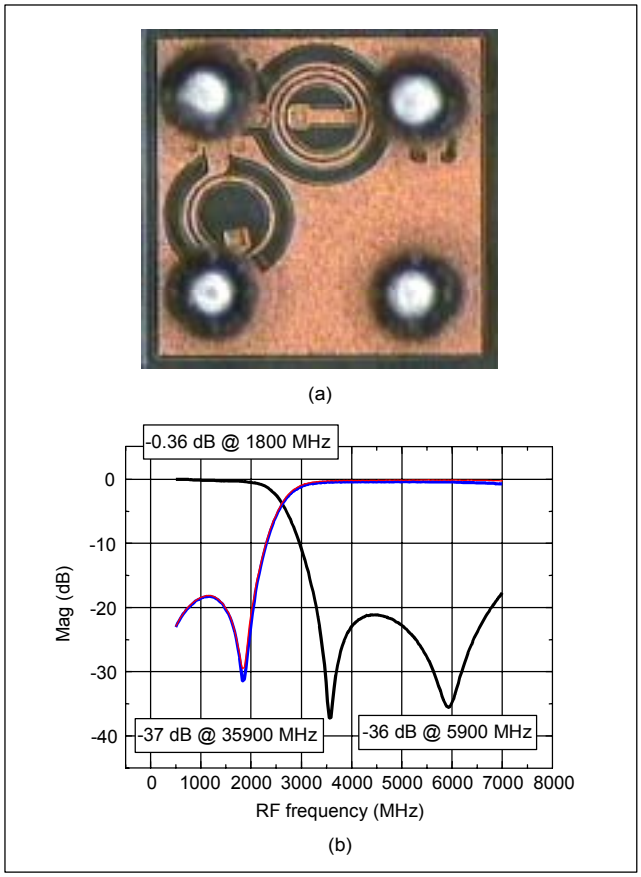

Fig. 5. The 1800 MHz low pass filter with bumped solder balls: (a) a photograph, (b) the measured data.

obtained. The size of the fabricated wafer-level-packaged filter was 1.0 mm^2 and corresponded to 78% of the minimum size of a conventional filter component. An additional 20% size reduction was achieved for a wire-bondable low pass filter for multichip module applications. Its size was 0.8 mm^2.

A photograph and the measured performance of another key component, the diplexer, are shown in Fig. 6. Insertion losses of 0.5 dB in the GSM band and 0.6 dB in the DCS band were obtained and the band rejection level was more than 25 dB. The size of the wafer-level-packaged diplexer was 1.50 mm^2, which was 65% of other conventional devices. For a wire-bondable diplexer, the size was 1.0 mm^2. These two RF IPDs (the low pass filter and diplexer) could be cost- and size-effectively applied to dual-band, tri-band ASM and FEM applications.

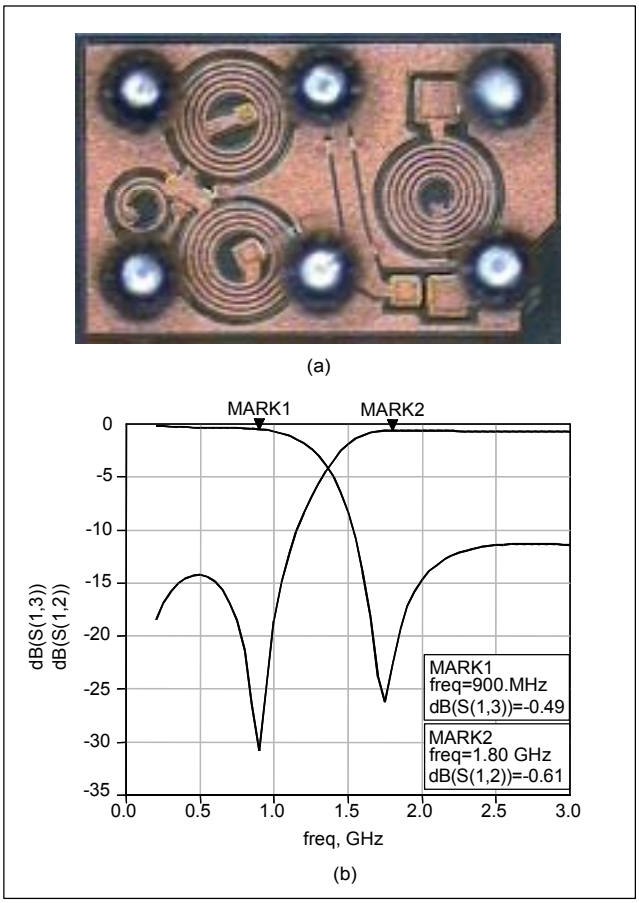

Fig. 6. GSM/DCS dual band diplexer with bumped solder balls: (a) a photograph, (b) the measured data.

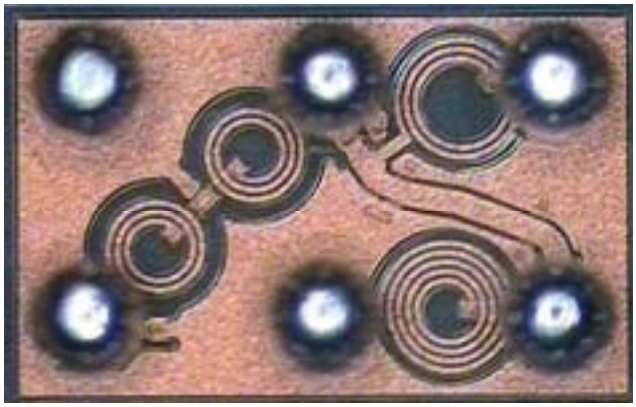

Fig. 7. The photograph of 5 GHz wideband balun.

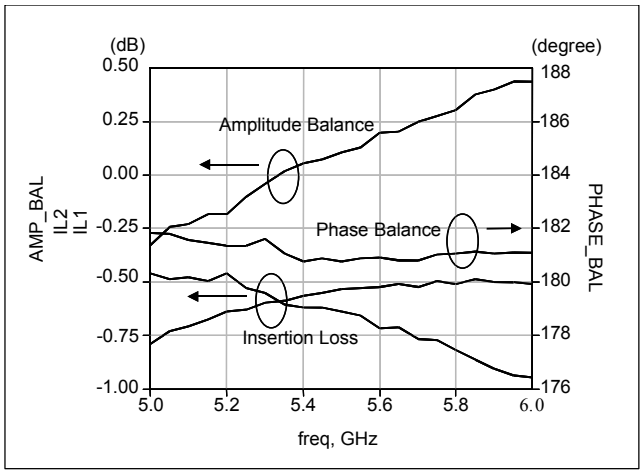

Fig. 8. The measured performance of wideband balun.

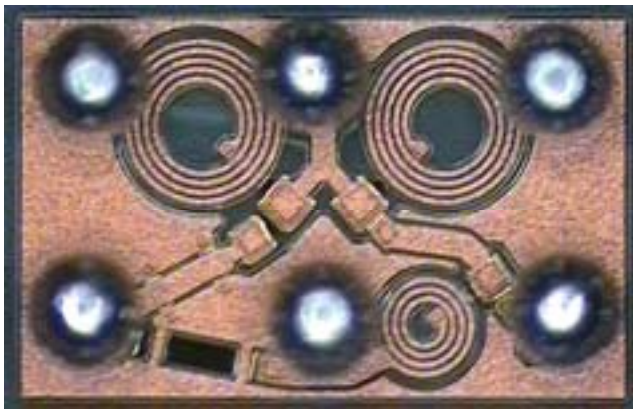

Fig. 9. The LC-type lumped power combiner/divider.

Figure 7 shows a photograph of the fabricated wideband balun for 5 GHz wireless LAN applications. The measured data are shown in Fig. 8. The insertion loss was 0.5-0.8 dB, and the obtained amplitude and phase imbalances were less than 0.3 dB and 2 ^{o} at 5.2-5.8 GHz, respectively. The size of the wafer-level-packaged 5 GHz balun was 1.50 mm^2 (63% of other conventional device sizes) and the size of the wire-bondable balun was 1.0 mm^2.

The fabricated LC-type lumped power combiner is shown in Fig. 9. The measured insertion loss was typically 0.5 dB at 1800

MHz and isolation was more than 25 dB. Second and third harmonic attenuations of 14 dB and 24 dB were achieved. The return loss was lower than –15 dB in 1500 MHz-2000 MHz. The wafer-level-packaged device was 1.5 mm^2.

All these Cu-based RF IPDs had current handling capability much superior to the Au-based devices or Al-based devices commonly used in the wireless semiconductor industry and also showed high RF performances. Therefore, the wafer-based RF IPDs will be the optimal choice for ASM or FEM applications of handsets and high-speed wireless applications that require lower cost and smaller size components.

V. DISCUSSION ON MODULE APPLICATIONS

RF IPDs on Si smart substrates could be applied to many wireless modules, such as ASM, FEM, and WLAN. In particular, the unique features of a small form and thick insulator on Si made it possible to integrate SAW filters, monolithic microwave integrated circuit (MMIC), and RF passive devices on a single die or in a single package. With the co-integration of SAW filters and Rx MMICs, the CDMA/PCS/AMPS dual band, tri mode receiver module was achieved on a small size Si smart substrate of 4 mm×3.6 mm and was packaged in a 7 mm×7 mm ceramic package. The fabricated dual band/tri mode receiver module is shown in Fig. 10. The measured data of the Rx module was very close to the combined data of the SAW filter's and LNA/Mixer MMIC's respective performances. The gain control of the CDMA band could change the pass band gain from 27 dB to 11 dB (low gain mode). More than a 30 dBc gain difference could be obtained from an embedded SAW filter. The measured data for the CDMA high gain mode, low gain mode, and AMPS mode is shown in Fig. 11.

Small-size RF IPDs can be utilized to implement a phase shifting function of the SAW duplexer module. Conventionally, the phase shifting network is composed of a quarter wavelength transmission line on a low temperature cofired ceramics (LTCC) substrate. The package size of the SAW duplexer module is mainly determined by the embedded phase shifting network in the LTCC structure. The RF IPDs can be integrated together with the SAW duplexer filter in a low cost high temperature cofired ceramics (HTCC) package, compared to the expensive LTCC package, and the package size is determined mostly by SAW filter size and its design. The size of the phase shifting RF IPD is expected to be 0.8 mm^2 and can be packaged with a lot of advanced packaging technologies.

This kind of embedded SAW module has the advantages of area saving due to the small-size RF IPD, additional cost reduction due to cheap HTCC packaging and the utilization of already established standard assembly facilities, easy design for multimode and multiband modules, expandability to other wireless key modules with SAW filters, versatile choice for package type, and so forth.

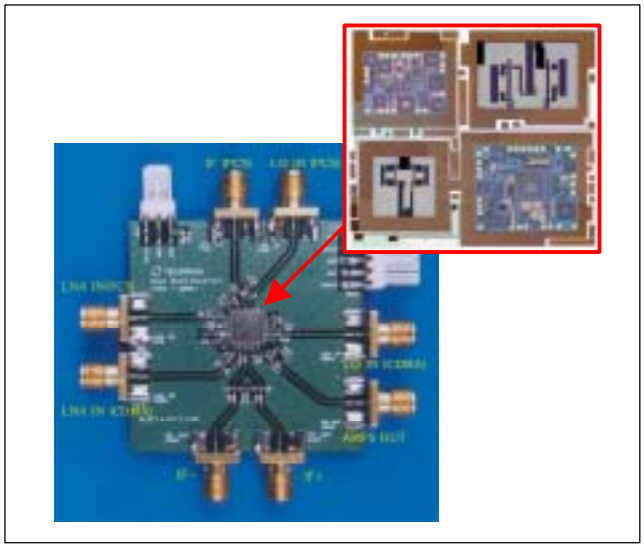

Fig. 10. CDMA/PCS/AMPS dual band, tri mode receiver module with built-in SAW filters on a Si smart substrate. The MMIC chip has low noise (LNA) and mixer functions and RF IPDs are also made on the substrate.

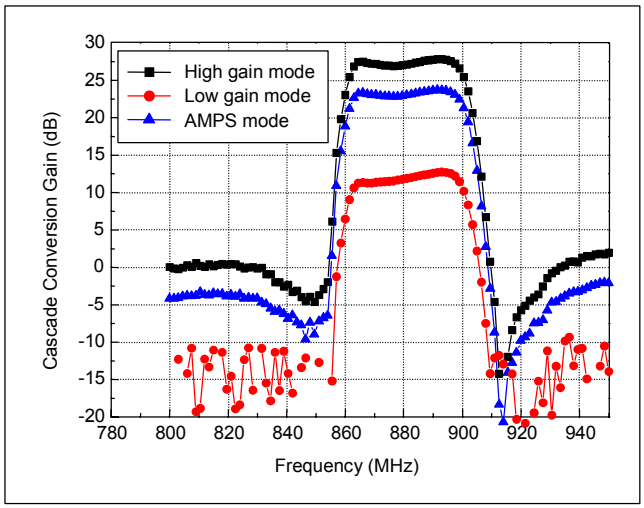

Fig. 11. The measured overall gain characteristics of CDMA and AMPS modes.

VI. CONCLUSIONS

There has been much research on RF passive integration on Si wafers to produce a low cost, mass-producible process. However, the research has not provided satisfactory solutions and the results have not been utilized in commercial industries. To meet the need of cost and size reduction, we developed a low cost manufacturing technology for a RF substrate and a high performance passive process technology for RF IPDs by

forming thick oxide on a Si wafer and using Cu metal and BCB interlayer material. The fabricated substrate with a 25 μm oxide thickness showed a good CPW transmission line loss of 0.03 dB/mm at 4 GHz, including a conductive metal loss. The transmission line loss was less than 0.1 dB/mm up to 15 GHz. With the well-developed substrate process and passive integration process, we obtained high Q inductors on the Si wafer, which showed a maximum quality factor range of 30-120, depending on inductance values of 0.35-35 nH. The inductors showed especially high quality factors in the broadband frequency range.

We also fabricated small-size RF IPDs for ASM or FEM applications and 5 GHz wireless LAN applications. The high power low pass filter had an insertion loss of 0.36 dB at 1800 MHz with an attenuation level of more than 30 dBc. The diplexer showed insertion losses of 0.5 dB at 900 MHz and 0.6 dB at 1800 MHz with an attenuation level of more than 20 dBc at the other band. The wideband balun showed good RF performance in the wideband of 5-6 GHz and had an insertion loss of 0.5-0.8 dB. Also the balun showed very small imbalances of phase and amplitude between two output ports. The power combiner had a 0.5 dB insertion loss and more than 25 dB isolation at 1800 MHz. All of the fabricated RF IPDs simultaneously showed very good RF performances and very high volumetric efficiencies. These RF IPDs can be widely utilized in applications of multiband/multimode ASM, FEM, and SAW duplexers, and other such applications.

Finally this thick oxide technology and the high performance passive integration technology will push the RF operating window of Si wafers well into 10 GHz and broaden the area of IPDs, which has been limited to several hundred MHz, up to more than 10 GHz. In addition, the technologies developed from our work will be widely utilized in hand-held phone modules and systems requiring a stringent size reduction and a tough cost reduction.

REFERENCES

[1] A.C. Reyes, "Silicon as Microwave Substrate," *IEDM Tech. Digest*, 1995, pp. 1759-1762.

[2] H. Sakai, "A New Millimeter-Wave IP-Chip on Silicon Substrate," *Asia Pacific Microwave Conf.*, 1994, pp. 291-294.

[3] B.K. Kim, B.K. Ko, and K. Lee, "Monolithic Planar Inductor and Waveguide Substrate on Silicon with Performance Comparable to Those in GaAs MMIC," *IEDM Tech. Digest*, 1995, pp. 717-720.

[4] Choong-Mo Nam and Young-Se Kwon, "High Performance Planar Inductor on Oxidized Porous Silicon (OPS) Substrate," *IEEE Microwave Guided Wave Lett.*, vol. 7, no. 8, 1997, pp. 236-238.

[5] Han-Su Kim, Dawei Zheng, A.J. Becker, and Ya-Hong Xie, "Spiral Inductors on Si p/p+ Substrate with Resonant Frequency of 20GHz," *IEEE Electron Device Lett.*, vol. 22, no. 6, 2001, pp. 275-277.

[6] Dong-Wook Kim, In-Ho Jeong, Chang-Yup Lee, Choong-Mo Nam, Tong-Ook Kong, Ho-Sung Sung, Ki-Joong Kim, Il-Do Yoon, Jong-Soo Lee, and Young-Se Kwon, "Ultra High Q Inductor and RF Integrated Passive Devices on Thick Oxide Si Substrate," 2002 *Pan Pacific Microelectronics Symp.*, Hawaii, USA, Feb. 2002, pp. 350-355.

[7] In-Ho Jeong, Choong-Mo Nam, Chang-Yup Lee, Jung-Hoon Moon, Jong-Soo Lee, Dong-Wook Kim, and Young-Se Kwon, "High Quality RF Passive Integration on Silicon Using 35 um Thick Oxide Manufacturing Technology," *The 52nd Electronic Components and Technology Conf.*, San Diego, USA, May 2002, pp. 1007-1011.

[8] Dong-Wook Kim, In-Ho Jeong, Ho-Sung, Tong-Ook Kong, Jong-Soo Lee, Chonng-Mo Nam, and Young-Se Kwon, "High Performance RF Passive Integration on Si Smart Substrate," 2002 *IEEE Int'l Microwave Symp.*, Seattle, USA, June 2002, pp. 1561-1564.

[9] A.L. Caviglia, R.C. Potter, and L.J. West, "Microwave Performance of SOI n-MOSFETs and Coplanar Waveguides," *IEEE Electron Device Lett.*, vol. 12, no. 1, Jan. 1991, pp. 26-27.

[10] Y. Wu, S. Gamble, B.M. Armstrong, V.F. Fusco, and J.A.C. Stewart, "SiO_2 Interface Layer Effects on Microwave Loss of High-Resistivity CPW Line," *IEEE Microwave and Guided Wave Lett.*, vol. 9, no. 1, Jan. 1999, pp. 10-12.

[11] H.S. Gamble, B.M. Armstrong, S.J.N. Mitchell, Y. Wu, V.F. Fusco, and J.A.C. Stewart, "Low-Loss CPW Lines on Surface Stabilized High-Resistivity Silicon," *IEEE Microwave and Guided Wave Lett.*, vol. 9, no. 10, Oct. 1999, pp. 395-397.

Dong-Wook Kim received his BS degree in electronic communications engineering from HanYang University, Seoul, South Korea, in 1990 and his MS and PhD degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST), Daejeon, South Korea, in 1992 and 1996. From 1991 to 2000, he worked as a Member of Technical Staff with LG Electronics Institute of Technology, Seoul, South Korea, where he was involved in developing microwave and millimeter wave circuits and modules. From 2000 to 2002, he was a Principal Engineer and General Manager of Telephus Inc., where he led the product development division to develop Si Integrated Passive Devices and Multi-Chip Module for microwave and millimeter wave applications. On September in 2002, he joined S1 Corporation, a company of Samsung Group. Since then, he has been involved in the development of wireless security systems. His areas of interest are low cost passive integration technology, RF and millimeter wave integrated circuit design, multi-chip modules

based on low cost passive integration processes, system-in-a-package, microwave sensors and wireless systems for security applications. Dr. Kim is a member of IEEE and IMAPS (International Microelectronics and Packaging Society).

In-Ho Jeong was born in Daegu, the Republic of Korea, in 1969. He received his MSEE and PhD degrees from the Korea Advanced Institute of Science and Technology, Daejeon, Korea, in 1997 and 2001. He worked on RF MEMS for his PhD study. Currently he is with the Telephus Inc. as a Senior R&D Engineer. His research interests include RF MEMS technology and Integrated Passive Devices for wireless communications.

Jong-Soo Lee was born in Seoul, Korea in 1971. He received his BSEE, MSEE and PhD degrees in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST) in 1994, 1996, and 2001. He was a Research Engineer in DaimlerChrysler Research Center, Ulm, Germany in 2000 for study of GaN power amplifiers. He won a best student paper award at 2000 ECTC (Electronic Components and Technology Conference), Las Vegas, supported by Motorola. He joined Telephus Inc. in Korea in 2000. His working area at Telephus includes passive devices modeling for MCM-D technology, design of passive circuits like filters and resonators, and design of RF modules integrated with passive circuits, and SAW-based filters like duplexers or diplexers and RFIC. His major interests are from active devices such as Si BJT or BiCMOS and GaAs (InP) MESFET, HEMT or HBT to design of RF subsystems or modules like transceiver modules including diplexers, LNAs, filters and mixers.

Young-Se Kwon received the BS degree from Seoul National University, Seoul, Korea, in 1968, the MS degree from Ohio University, Athens, in 1972, and the PhD degree from the University of California, Berkeley, in 1977, all in electrical engineering. From 1977 to 1979, he was a Research Associate in the Department of Electrical Engineering, Duke University, Durham, NC. He joined the Department of Electrical Engineering at the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1979, first as an Assistant Professor, and currently as a Professor. His main research has been focused on the development of AlGaAs/GaAs based opto-electronic integrated circuits (OEIC). His recent interest includes the development of MMIC's using standard GaAs MESFET and FECFET technology, optical devices, and opto-electrical packaging technology.