Buried Contact Solar Cells using Tri-crystalline Silicon Wafer

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Tri-crystalline silicon wafers have three different orientations and three-grain boundaries. In this paper, tri-crystalline silicon (tri-Si) wafers have been used for the fabrication of buried contact solar cells. The optical and micro-structural properties of these cells after texturing in KOH solution have been investigated and compared with those of cast mult- crystalline silicon (multi-Si) wafers. We employed a cost effective fabrication process and achieved buried contact solar cell (BCSC) energy conversion efficiencies up to 15% whereas the cast multi-Si wafer has efficiency around 14%.

Keywords: Tri-crystalline silicon (Tri-Si), Multi-crystalline silicon (Multi-Si), Buried contact solar cell (BCSC); Anti-reflection (AR) coating; Solar cell

1. INTRODUCTION

Nowadays, fabrication costs of crystalline silicon solar cells are occupied by wafer cost between 55 and 65 % [1,2]. Anyhow, crystalline silicon wafers are by far the dominant absorber materials for today's production of solar cells and modules due to their good price/performance relation and they're proven environmental stability. These wafers are mainly produced either by a solar-optimized Czochralski (Cz) growth method yielding crystalline silicon (c-Si) with low defect density or by a directional solidification or a ribbon growth method yielding large grained multi-crystalline (mc-Si) wafers with higher defect density. To further improve the price/performance relation of Cz solar cells, tri-crystalline silicon (tri-Si) is being developed as a high quality wafer material that combines both the high diffusion length of minority carriers of up to 1300 ㎛ of c-Si and the productivity of mc-Si. More than 1000 ㎛ LID (light induced defect-free) diffusion length could be reached with specially doped tri-crystals. This paper carried out a systematic investigation on the structural and optical properties of tri-crystalline silicon wafers with respect to c-Si wafers for solar applications. Tri-crystalline silicon is a promising candidate for achieving low cost and high efficiency solar cells. Small fraction of grain boundary gives higher lifetime than multi-crystalline silicon. Due to its high mechanical stability, tri-crystalline silicon allows both quasi-continuous pulling and thin slicing with higher mechanical yields. Ultra-thin wafer could contribute to the reduction of the amount of silicon consumption and thereby lowering the solar cell cost. Tri-Si is a crystal compound consisting of three mutually tilted mono-crystalline silicon grains. The crystal compound has a (110)-surface orientation in all grains in contrast to the standard (100) orientation of wafers for today's solar cell production. The yield of a 200 ㎛ thick tri-crystalline (110) silicon wafer is almost the same as that of a 300 ㎛ thick standard wafer[3]. Buried contact solar cell (BCSC) offers the possibility of combining low cost and high performance[4,5]. Part of front metal contact is buried in a groove, resulting in low shading loss of the metal contact. (110) Silicon has been used to increase the optical path length of thin silicon devices by exposing the (111) face by a photolithographic technique at the rear surface[6]. In this work, the processes to make cost effective high efficiency cells were developed using tri-crystalline silicon wafer. We compared the efficiency performance of cells fabricated on tri-crystalline silicon with those of multi-crystalline wafers single crystalline Cz-wafers. Chemical etching of tri-crystalline silicon by an anisotropic etching solution was studied. Computer simulation was done using SUNRAY[7] in order to investigate the effect of encapsulation on the performance of textured tri-crystalline silicon.

2. EXPERIMENTAL

Boron-doped tri-Si, multi-Si and Cz c-Si wafers, each with a thickness of 350 ㎛ and resistivity of 1-3 Ωcm were used for the fabrication of solar cells. These three kinds of wafers were etched in HF : HNO_3 (1 : 10) to a thickness of 330 ㎛ to remove saw damage. Texturing of tri-Si was conducted in a 30% KOH solution for 30 and 60 mins with appropriate isopropyl alcohol as surface activation agent. A P_2O_5 solid source was used for emitter formation and heavy diffusion in the groove. Silicon dioxide was grown by pyrogenic oxidation to mask the top surface during phosphorous heavy diffusion and metal plating into the grooves.

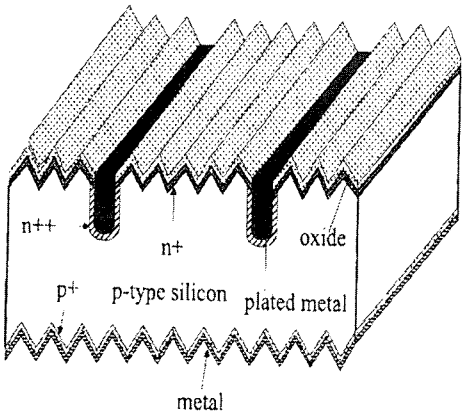

Fig. 1. Schematic diagram of buried contact solar cell with V-grooved surface[4,5].

Aluminum was evaporated over the rear surface and sintered at 980 ℃ to provide a back-surface field. Finally, the cells were annealed at 400 ℃ for 20 mins in forming gas (4 % H_2 in Ar) ambient. A schematic diagram of buried contact solar cell is shown in fig. 1. Computer simulation, using SUNRAY software, was carried out to investigate the effects of V-grooves, composed of (111) faces, on the reflectance of completed solar cells before and after encapsulation. A carrier generation function calculated by SUNRAY was introduced to device simulator PC1D in order to estimate the efficiency enhancement of encapsulated cells.

3. RESULTS AND DISCUSSION

Figure 2 shows the SEM image of textured surface of tri-crystalline wafers. The uniform texturing of the surface is found to be an advantage of tri-Si over multi-crystalline silicon.

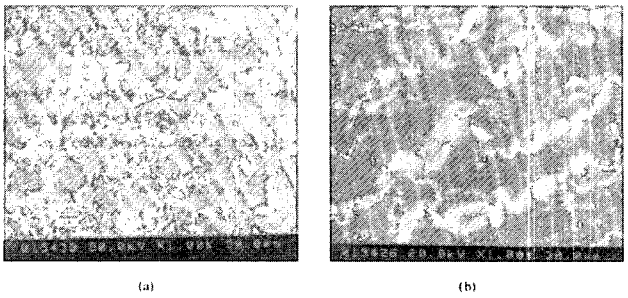

Fig. 2. SEM images of tri-Si etched in 30% KOH solutions with appropriate isopropyl alcohol at 70 ℃ for 30 mins(a) and 60 mins(b).

The etching rate of single crystalline silicon in anisotropic etching solution, such as KOH, decreases in the order of (100) > (110) > (111). For example, the etching ratio of (110) and (111) planes in a mixture of 35 % KOH solution is about 600: 1 [8]. The roughness as in Fig. 2, therefore, is originated from the difference of etching rate between (110) and (111) planes. After texturing, V-grooves with an angle of 110° are found to appear over the (111) faces, resulting in a facet of 35° [9] The average pitch of the groove increases with etching time from 7.5 ㎛ for 30 mins to 8.6 ㎛ for 60 mins. The relationship between (110) orientation and (111) faces and the facet angle are shown in Fig. 3.

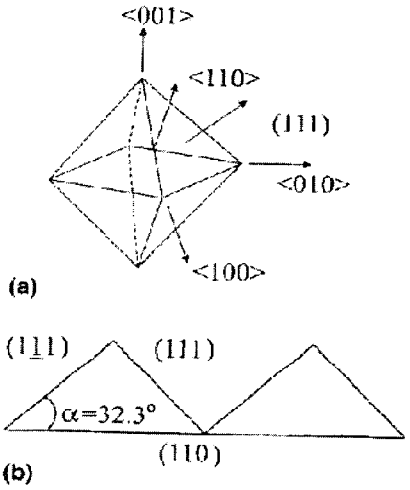

Fig. 3. Orientations of <110> and <111>(a) and facet angle used for simulation using SUNRAY(b).

On the textured surface, the number of reflection depends on the facet angle. Reflected light from (111) face does not bounce from the wafer because the facet angle is less than 45° and the reflectivity of tri-crystalline wafers, after texturing, cannot be lowered. Fig. 4 shows the reflectance of flat and textured tri-Si wafers before encapsulation, as calculated by the computer simulation

program SUNRAY. In the simulation, the reflectance was calculated for 350 μm thick silicon wafers with a 109 nm thick silicon dioxide anti-reflection (AR) coating. As predicted by simple calculation, the reflectance of wafers with a V-groove of facet angle 35° is the same as that of flat wafers. The simulation of optical reflectance with the SUNRAY program for the flat and textured tri-Si after encapsulation is shown in Fig. 5.

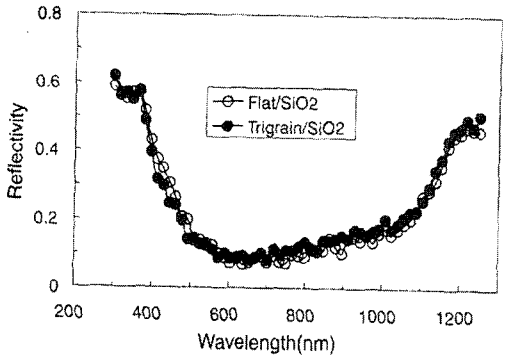

Fig. 4. Reflectivities of trigrain wafer textured (•) and flat wafers (○), which were encapsulated after oxidation.

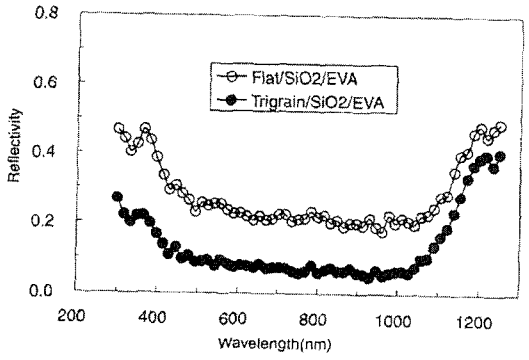

Fig. 5. Reflectivities of textured (•) and flat wafers (○), which were encapsulated after oxidation.

The cells are encapsulated under glass by 3 mm thickness of ethylene vinyl acetate (EVA) of refractive index 1.5 (assumed to be same as that of silicon dioxide). Reflection from the front surface of the glass was neglected in the simulation. The reflection of a cell which has a V-groove of facet angle 35° decreases significantly, whereas the reflectance of a flat wafer increases after encapsulation. When the cells are encapsulated, reflected light from the surface of cell is reflected again into the cell at the air/glass interface. Furthermore, encapsulation of textured wafers decreases reflectivity at short and long wavelengths when SiO_2 / TiO_2 was used for the anti-reflection layer, as shown in fig. 6. The thicknesses of TiO_2 and SiO_2 were 43 and 20 nm, respectively, This clearly indicates that the efficiency of solar cells can be enhanced when the textured cells are encapsulated for module fabrication.

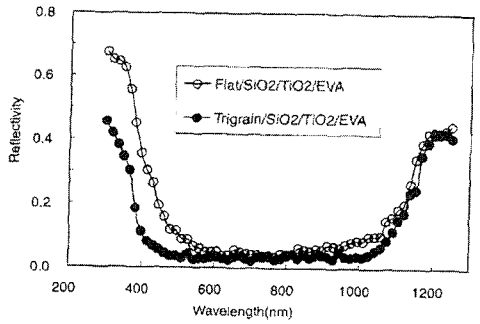

Fig. 6. Reflectivites of textured (•) and flat wafers (○) which were encapsulated after SiO_2 / TiO_2 coating.

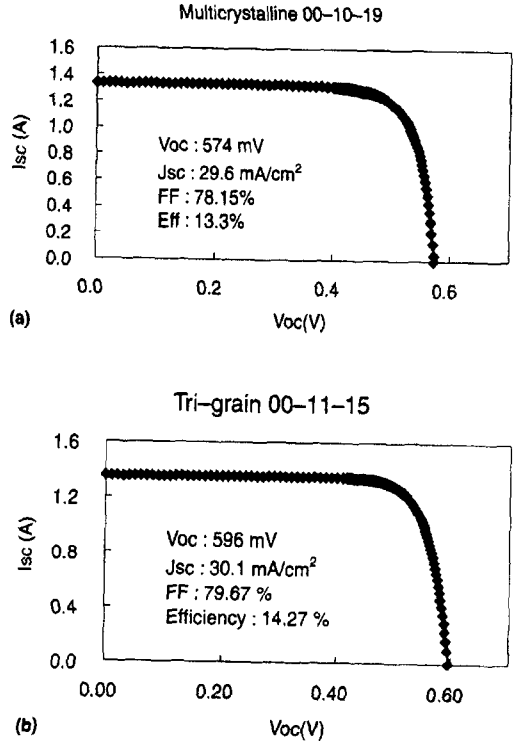

Fig. 7. Current-voltage characteristics of solar cells made on multi-crystalline silicon wafer(a) and tri-crystalline silicon wafer(b).

Figure 7 shows the I-V characteristics of cells fabricated on multi-crystalline and tri-crystalline wafers. The open circuit voltage of the cell fabricated using tri-crystalline was higher than multi-crystalline wafer due to higher carrier lifetime. Efficiencies of 14.27 and 13.3 % were obtained for tri-crystalline silicon wafer and multi-crystalline wafer, respectively.

Table 1. Measured current-voltage parameters for 45 ㎠ BCSC cells fabricated on Multi-Si, Tri-Si and CZ-Si wafers before encapsulation.

Wafer	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	E_{ff} (%)
Multi-Si	591·0	29·9	0·804	14·22
Tri-Si	609·3	30·8	0·802	15·05
CZ-Si	628·8	30·7	0·809	15·59

Efficiencies were measured under the AM1·5 spectrum (100 mW/cm^2) at 25°C with the SPI-CELL TEST 150 system.

Table 2. Effective lifetime of wafers measured in alcoholic iodine solution (0.3M iodine in ethanol) by μW-PCD method.

Wafer	Oxygen content (ppma)	Carbon content (ppma)	Effective lifetime (μs)	Effective lifetime after gettering (μs)
Multi-Si	1·2–1·3	2·43–2·50	19·8	29·8
Tri-Si	13·0–13·6	1·11–1·35	26·5	41·6
CZ-Si	16	<0·1	62·8	70·2

Table 3. Output parameters of Tri-Si solar cells simulated by PC1D for various surface structures.

Cell structure	J_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)	Efficiency (%)
Flat/SiO_2	32·34	654·0	79·7	16·85
Flat/SiO_2/EVA	29·1	651·1	80·0	15·16
Flat/SiO_2/TiO_2	34·24	655·5	79·4	17·83
Flat/SiO_2/TiO_2/EVA	34·61	655·8	79·4	18·03
Texturing/SiO_2	32·24	653·9	79·6	16·79
Texturing/SiO_2/EVA	35·07	656·2	79·4	18·26
Texturing/SiO_2/TiO_2	36·36	657·2	79·2	18·93
Texturing/SiO_2/TiO_2/EVA	36·40	657·2	79·2	18·95

Electron–hole pair generation for each surface structure was calculated by SUNRAY and put into the PC1D for simulation.

Table 1 shows the output parameters of 45 ㎠ BCSC fabricated on multi-crystalline wafers, tri-Si and Cz c-Si wafers. Efficiencies of 14.22, 15.05 and 15.59 % were obtained for multi-Si, tri-Si and Cz-Si wafers respectively. It was found that the efficiencies for the three kinds of wafers were mainly determined by the open-circuit voltage. All the wafers were untextured, and the short-circuit current densities of the cells are found almost to be the same. The shading loss due to the front metal finger and pad was measured as 10.8 %, which corresponds to a finger with a thickness of 65 ㎛. The sheet resistance of the heavily diffused layer under the front metal contact was estimates as 5-10 Ω/□, and that of the emitter as 150-200 Ω/□. The relatively low short-current may be attributed to the highly reflective surface of untextured wafers and the non-optimized aluminum sintering process for the back-surface field. The efficiency of textured tri-Si wafer was almost the same as that of untextured tri-Si. It seems that the change of open-circuit voltage was caused by the difference in carrier lifetime of each wafer. Table2 shows the effective carrier lifetime of multi-Si, tri-Si and Cz c-Si wafers. Measurement of the effective minority-carrier lifetime by microwave-PCD (photo-conductive decay) analysis revealed that the lifetime of tri-Si is higher than that of multi-crystalline silicon wafer, even though tri-Si contains significant oxygen impurity. Table3 shows the output performances of cells fabricated on tri-Si wafers. The results were simulated by PC1D in order to study the effects of encapsulation at several surface conditions. The simulation clearly indicates that the short-circuit current density of textured cell with SiO_2 anti-reflection layer can be enhanced by 2.8 mA/㎠ after encapsulation. Encapsulation of textured cells is expected to increase the short-circuit current density by about 1.8 mA/㎠, even for cells with a SiO_2 / TiO_2 double AR coating. The absolute value of the enhancement depends on the reflectance of glass, because reflection from the front surface of the glass was not included in the simulation indicating that the performance of modules with textured tri-Si wafers is much higher than that of modules with flat wafers, regardless of AR coating layers.

4. CONCLUSIOSN

Tri-Si, multi-Si and Cz-Si wafers have been used for production of high-efficiency solar cell. Efficiencies of 14.22, 15.05 and 15.59 % have been obtained for multi-Si, tri-Si, and Cz-Si wafers, respectively. The solar cells fabricated on tri-Si showed higher open-circuit voltage as compared with cells on multi-crystalline wafer, due to the longer lifetime. The surface of tri-Si etched in KOH solution showed a V-groove with facet angle 35°. Calculation using PC1D demonstrated that the short-circuit current density of textured cells, with SiO_2 as AR coating layer can be enhanced by 2.7 mA/㎠ after encapsulation in EVA.

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