A Layout-Based CMOS RF Model for RFIC's

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In this paper, a layout-based CMOS RF model for RFIC's including the capacitance effect, the skin effect, and the proximity effect between metal lines on the Si surface is proposed for the first time for accurately predicting the RF behavior of CMOS devices. With these RF effects, the RF equivalent circuit model based on the layout of the multi-finger gate transistor is presented. The capacitances between metal lines on the Si surface are modeled with the layout. And the skin effect is modeled to the equivalent ladder circuit of metal line. The proximity effect is modeled by adding the mutual inductance between cross-coupled inductances in the ladder circuit representation. Compared to the BSIM 3v3 and other models, the proposed RF model shows better agreements with the measured data and shows well the frequency dependent behavior of devices in GHz ranges.

Keywords : Layout, CMOS, RF, Skin Effect, Proximity Effect, Model.

1. INTRODUCTION

Recently, as the deep submicron CMOS technology is progressed, the application area of CMOS is enlarged to radio frequencies in the GHz range and thus many commercial RF products are developed for highly integrated RF CMOS communication systems. Especially, with the advantages of the low-cost and the high integration, the RF CMOS technology is more important for single chip RF system ICs [1].

For designing CMOS RFIC's, an accurate MOSFET model which is valid for all bias from dc to RF is required. However, the existing CMOS models were not fully accurate in the RF region. Therefore, it was difficult to predict the RF behavior of devices. To overcome these inaccuracy, some advanced models such as the effective gate resistance model [2] or the CMOS RF modeling for GHz communication IC's [3], etc.[4] have been proposed. All of them add a gate resistance and a substrate coupling network to the core BSIM 3v3 or analyze the gate resistance as the distributed gate and channel resistances. But in those models, the gate resistance was obtained by curve fitting or extracted from measured data for obtaining a good agreement with experiments.

Since RF CMOS transistors are usually large devices and thus implemented as multi-finger devices due to the limited width, the effect due to the layout, the skin effect and the proximity effect which are very important in GHz ranges should be included in the RF CMOS model. Existing models do not consider these important effects. As the result, they could not predict accurately the RF behavior of devices such as the varying of trans-conductance with frequencies in GHz ranges.

In this paper, a layout-based CMOS RF model for RFIC's including the skin effect and the proximity effect is proposed for the first time. The proposed model is verified by comparing the simulation results with the measured data and other models.

2. MULTI-FINGER GATE LAYOUT AND RF CMOS EQUIVALENT CIRCUIT

A layout example of the typical RF multi-finger device is presented in Fig. 1. This Fig. 1 represents the layout for 4-finger gate structure. Where L_f is the length of a single finger and W_f is the width of a single finger. Therefore, the total finger width is represented as eq.(1),

$$W_{eff} = N_f \cdot W_f \tag{1}$$

where N_f is the number of fingers.

In usual RF CMOS process, the gate is produced with

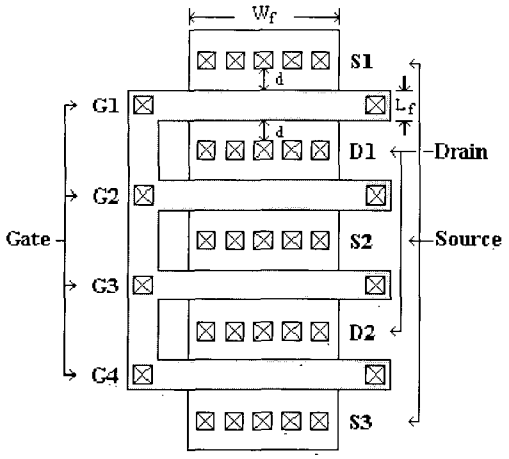

Fig. 1. The layout of multi-finger MOSFET.

the poly-Si, and the drain and the source are produced with the metal. Therefore, there are capacitances between metals and the poly-Si, C_{gsm} and C_{gdm}, on the Si surface. These capacitances can be neglected in DC or low frequency operations because their impedances are infinite or very high. However, on RF operation in GHz ranges, impedances of these capacitances are not very high, and thus the effect of these capacitances should not be neglected.

These capacitances between metal lines can be represented as next eq.(2):

$$C_{gsm} = C_{gdm} = \frac{\varepsilon_i \cdot W_f \cdot t_m}{d} \tag{2}$$

where ε_i is the dielectric constant of material between metal lines, and SiO_2 is used in usual CMOS process. And t_m is the metal thickness and d is the distance between each metal lines. Then, using the λ-based design rule, the eq.(2) may be represented for $d=3\lambda$ as next:

$$C_{gsm} = C_{gdm} = \frac{\varepsilon_i \cdot W_f \cdot t_m}{3\lambda} = \frac{\varepsilon_i \cdot W_{eff} \cdot t_m}{3\lambda \cdot N_f} \tag{3}$$

In addition to the effect of capacitances between metal lines on the Si surface, it should be included some other effects such as the skin effect and the proximity effect for RF IC applications. These effects are mainly investigated for the on-chip spiral inductors in silicon-based RF IC's. As operating frequencies enter the GHz range, it is found that the resistance and the inductance of metal lines are strongly dependent on the frequency due to the non-uniform current distribution in the conductor [5]. For a single metal line, as the frequency goes up, the AC current is pushed toward the surface of the conductor by the skin effect. To capture this skin effect, a parallel branch is added in equivalent circuit of metal line.

And, the magnetic field generated by neighboring metal lines further changes the current distribution and results in a higher current density at the edges of the metal lines. This proximity effect causes the increase of resistance and inductance by frequency in the metal lines together with the skin effect. This magnetic interaction between the external field and the internal current on the spiral inductors is modeled by adding the mutual inductance between cross-coupled inductances in the ladder circuit representation [6].

Using the ladder circuit representation and including the capacitance effect, the skin effect, and the proximity effect, we represent the 3-dimensional model structure of RF MOSFET with a single gate finger and neighboring drain and source fingers for the first time in Fig. 2. Then, the frequency dependences of resistance and inductance of metal lines are obtained to next eqs.(4) and (5):

$$R_j(\omega) = \frac{R_{j0}R_{j1}(R_{j0}+R_{j1})+\omega^2 R_{j0}L_{j1}^2}{(R_{j0}+R_{j1})^2+\omega^2 L_{j1}^2} \tag{4}$$

$$L_j(\omega) = L_{j0} + \frac{L_{j1}R_{j0}^2}{(R_{j0}+R_{j1})^2+\omega^2 L_{j1}^2} \tag{5}$$

where the subscript j represents the each electrode of gate, drain, or source of the MOSFET.

From eqs.(4) and (5), the DC resistance and the DC inductance at $\omega=0$, R_{jdc} and L_{jdc}, are represented as follows:

$$R_{jdc} = \frac{R_{j0}R_{j1}}{R_{j0}+R_{j1}} \tag{6}$$

$$L_{jdc} = L_{j0} + \frac{L_{j1}R_{j0}^2}{(R_{j0}+R_{j1})^2} \tag{7}$$

The inductance at $\omega=\infty$, $L_j(\infty)$, is represented as $L_j(\infty)=L_{j0}$. In addition, the empirically optimized condition between $R_{j0}L_{j0}$ and $R_{j1}L_{j1}$ can be expressed as [7]:

$$\frac{L_{j0}}{L_{j1}} = \alpha \cdot \frac{R_{j1}}{R_{j0}} \tag{8}$$

Where α is optimized to 0.315 for single circular wire. From eqs.(6), (7), and (8), resistances and inductances of the equivalent circuit are derived as follows:

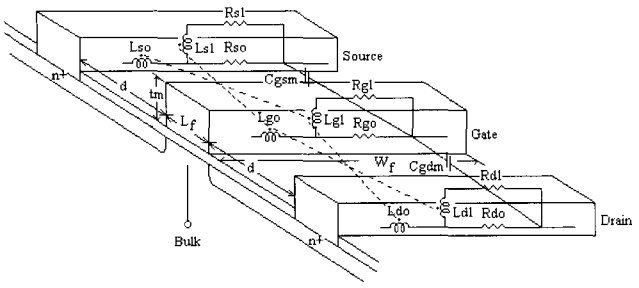

Fig. 2. 3-Dimensional model structure of single-finger MOSFET.

$$R_{j0} = R_{jdc}/(1 - \sqrt{\alpha}) \quad (9)$$

$$L_{j0} = L_{jdc}\cdot(1 - \sqrt{\alpha}) \quad (10)$$

$$R_{j1} = R_{jdc}/\sqrt{\alpha} \quad (11)$$

$$L_{j1} = L_{jdc}/\sqrt{\alpha} \quad (12)$$

$$L_{jkm} = k\sqrt{L_{j0}L_{k1}} \quad (13)$$

With these model parameters, the RF equivalent circuit model for 4-finger gate MOSFET's of Fig. 1 is represented as Fig. 3, where R_{db}, R_{sb}, and R_{sub} are the drain-bulk resistance, the source-bulk resistance, and the substrate resistance, respectively. C_{db} and C_{sub} are the drain-bulk capacitance and the substrate capacitance, respectively. And diodes, Dd and Ds, are the external junction diodes in the Drain and the Source, respectively In addition, L_{gdm}, L_{dgm}, L_{gsm}, and L_{sgm} represent the mutual inductances between cross-coupled inductances due to the proximity effect, respectively. The multi-finger transistor is concentrated in single elements. Since capacitances between metal lines of single-finger structure on the Si surface, C_{gsm} and C_{gdm}, are all parallel in the multi-finger structure, respectively, the total capacitance of each one is directly proportional to W_f and N_f.

3. MODEL VERIFICATION

In order to verify the accuracy of proposed model, y-parameters of N_f=10, W_f=12 ㎛, L_f=0.36 ㎛ NMOS were simulated with this model and the BSIM 3v3 model for V_g=1V and V_d=1V and compared with the measured data and the simulation results of Enz's model[4]. The results were shown in Fig 4. This Fig. 4 shows that y-parameter values of the proposed model are in better agreement with the measured data[4] than the BSIM 3v3 model or the Enz's model, except for Im{y11}. The maximum difference of Im{y11} between

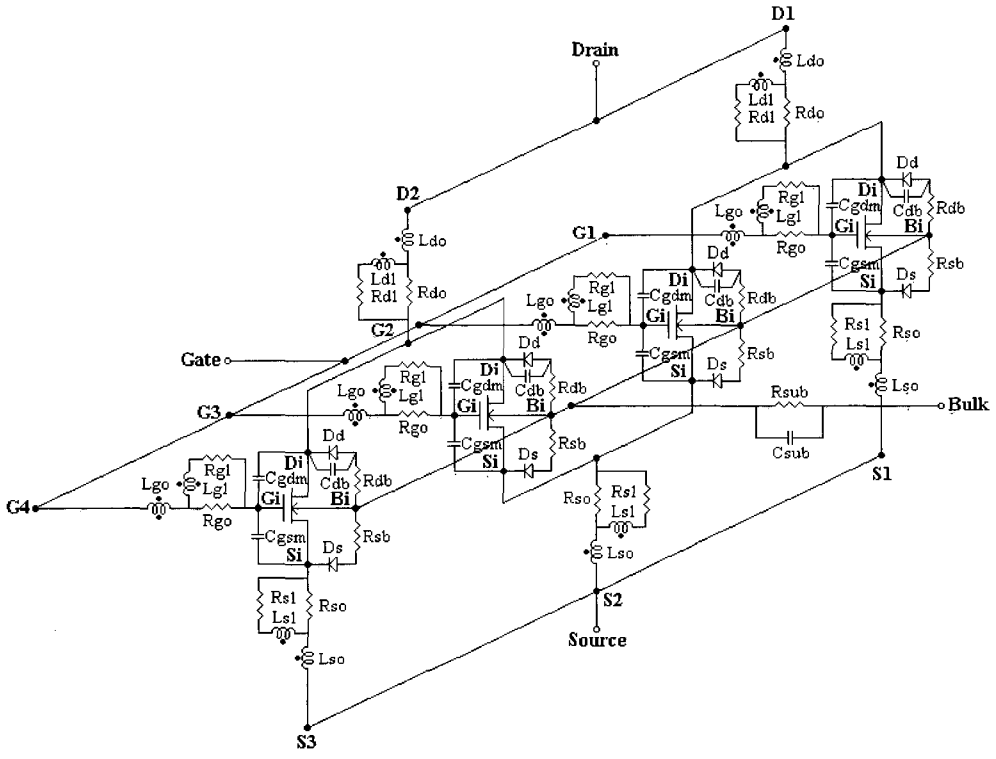

Fig. 3. RF equivalent circuit model for 4-finger gate MOSFET's.

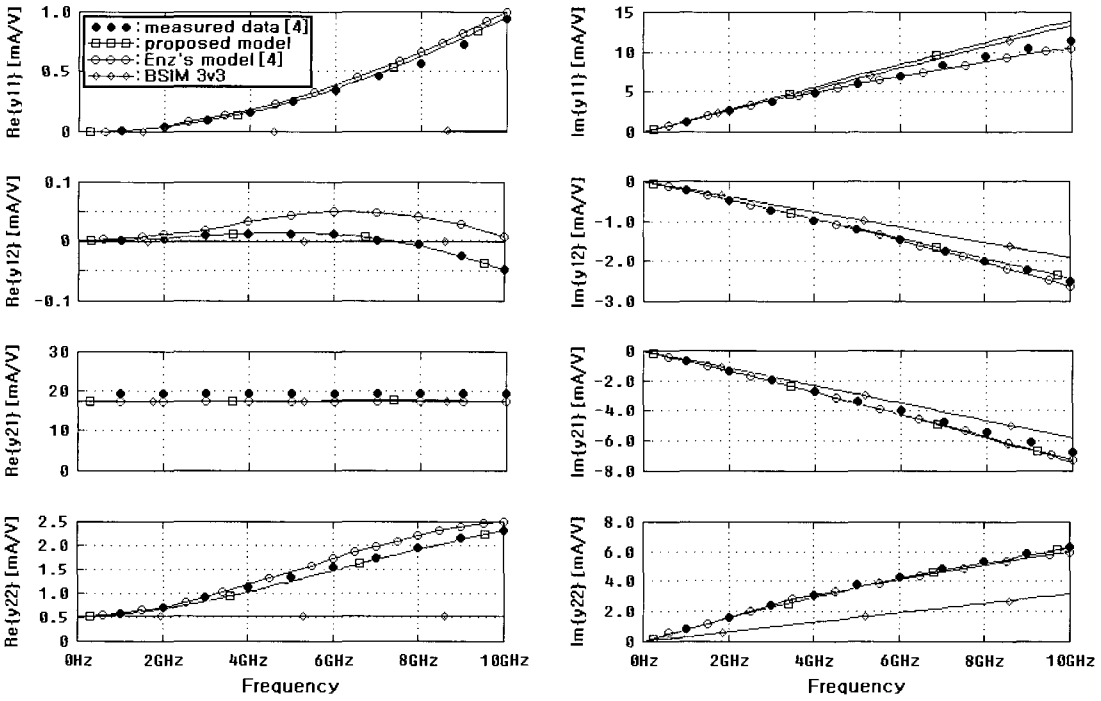

Fig. 4. y-parameters of N_f=10, W_f=12 ㎛, L_f=0.36 ㎛ NMOS.

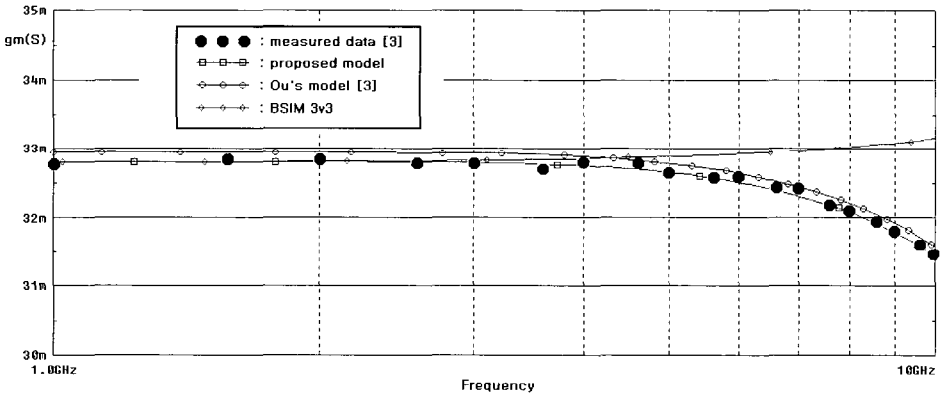

Fig. 5. Transconductance of 160/0.35 ㎛ NMOS.

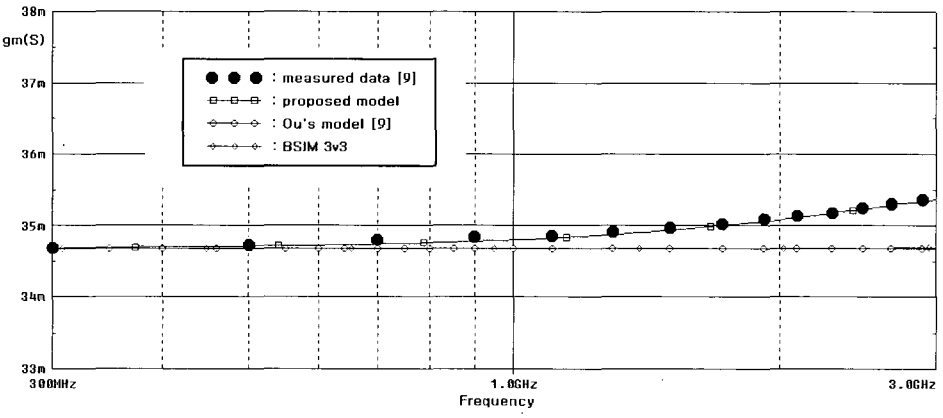

Fig. 6. Transconductance of 240/0.35 ㎛ NMOS.

the proposed model and the measured data is about 2mA/V at 10GHz, which is compared with the maximum difference about 1mA/V at 10GHz between the Enz's model and the measured data. This discrepancy maybe due to the intra-device substrate coupling effect. Except for Im{y11}, the proposed model shows the excellent agreement with the measured data.

In addition, the transconductance of NMOS was simulated with this model and the BSIM 3v3 model, and compared with the measured data and the simulation results of other models. As a first example, the transconductance of 160/0.35 ㎛, 16-finger gate NMOS with R_g=9Ω and R_{sub}=90Ω was simulated for V_g=2v and V_d=2v, and the result was shown in Fig. 5 with the measured data and the simulation results of Ou's model [3]. And as a second example, the transconductance of 240/0.35 ㎛, 24-finger gate NMOS with R_g=9.5Ω and R_{sub}=50Ω was simulated for V_g=0.9v and V_d=2v, and the result was shown in Fig. 6 with the measured data and the simulation results of Ou's other model[9]. The simulations were performed with SPICE parameters of the MOSIS 0.35 ㎛ process.

Compared to the BSIM 3v3 and other models, the proposed model shows better agreements with the measured data in Fig. 4, 5 and 6. And clearly the proposed RF model shows well the frequency dependent behavior of devices in GHz ranges.

4. CONCLUSIONS

A layout-based CMOS RF model for RFIC's has been proposed for the first time for accurately predicting the RF behavior of CMOS devices. Including the capacitance effect, the skin effect, and the proximity effect between metal lines on the Si surface, a new RF equivalent circuit model for multi-finger gate MOSFET's has been developed. Compared to the BSIM 3v3 and other models, the proposed RF model shows better agreements with the measured data and shows well the frequency dependent behavior of devices in GHz ranges. Therefore, this new RF model may allow designers to simulate and design non-linear CMOS RF circuits with the accuracy.

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