

논문 2003-12-1-07

Design of charge pump circuit for analog memory with single poly structure in sensor processing using neural networks

Yong-Yoong Chai*, and Eun-Hwa Jung*

Abstract

We describe a charge pump circuit using VCO (voltage controlled oscillator) for storing information into local memories in neural networks. The VCO is used for adjusting the output voltage of the charge pump to the reference voltage and for reducing the fluctuation generated by the clocking scheme. The charge pump circuit is simulated by using Hynix 0.35um CMOS process parameters. The proposed charge pump operates properly regardless to the temperature and the supply voltage variation.

Key Words : charge pump, VCO, analog memory, neural networks

I. Introduction

Rapid advances in communication and computer network make it possible to gather the information from various types of data fields: text, voice, and image etc. Neural networks with parallel, distributed and adaptive information processing systems, represent one of the approaches to enhance the computational capabilities in real-time information processing⁽¹⁾⁽²⁾. The neural networks are well suited for solving problems in sensor processing which can be defined as pattern recognition.

The neural networks are different from the conventional method in terms of the number of processing unit. They demand a large number of processing units. Remarkable advances of VLSI technologies have made it possible for the compact electronic systems to possess high functional capabilities.

Nevertheless, the weight controllability of the local memories in neural networks has a difficulty to realize it due to the complexity of the analog processing. Here, the weight means a local memory variable of a specified mathematical data type that is assigned to each input connection in neural networks.

The analog memory⁽³⁾⁽⁴⁾ is considerably well suited for representing the weight in neural networks. In conventional digital memory, several bits are required to represent just on-state, whereas the analog memory requires just one cell to characterize the state. In addition to the enhancement of the storage density, the analog memory also contribute to simplify a typical signal processing system implemented with peripheral devices such as A/D and/or D/A converter.

The double poly structure usually has been used in the analog memory. Lately, the paper describing a flash using single poly structure has been introduced⁽⁵⁾. The structure is intere-

* 계명대학교 전자공학과(Dept. of Electronic Engineering, Keimyung University)

<접수일자 : 2002년 10월 15일>

sting in terms of cost effective. However, the structure demands two different programming schemes: F-N tunneling and Hot-electron injection. Due to that fact, the charge pump circuit for generating several high programming voltages is required. This paper describes new charge pumps that are suitable for eliminating the limitations and offering versatile voltages depending on the operation.

II. Charge pump with VCO

The Charge pump is a circuit that can pump charge upward to produce voltages higher than their supply voltage. The charge pump has been used in the nonvolatile memories, such as EEPROM and flash memories, for the programming of the floating devices.

The programming voltages used in altering the data in the non-volatile memories are versatile depending on the operations: writing, erasing, and reading. Most MOS charge pumps are based on the circuit proposed by Dickson⁽⁶⁾. The charge pump circuit had obtained the voltages by modifying the driving frequency and the number of stages comprised of capacitors and MOSs. The charge pump has operated well in normal circumstance. But, as the supply voltage decreases, the magnitude of the clock voltage is decreased accordingly. Furthermore, the influence of the body effect in the charge pump cannot be neglected. Especially at the high-voltage nodes near the output, the increase in the threshold voltage can lower the voltage pumping gain significantly.

The charge pump utilizing VCO suggested in this paper is shown in Fig. 1. The circuit can operate with a 3.3 V

supply.

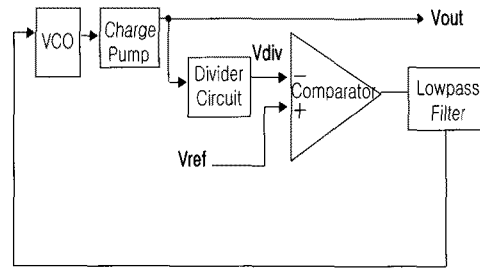


Fig. 1. A block diagram of charge pump using VCO.

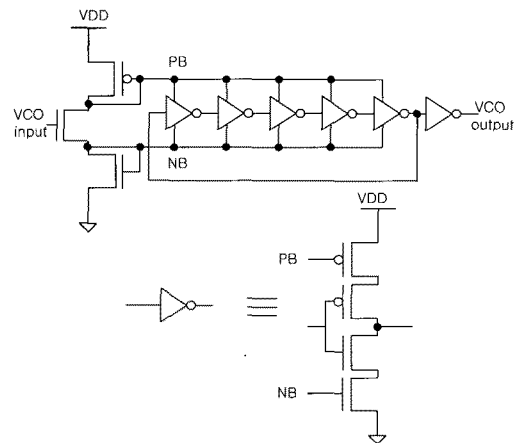


Fig. 2. A circuit diagram of VCO.

The reference voltage (V_{ref}) and the voltage (V_{div}) obtained by dividing the supply voltage are the signals into the positive and the negative input of the comparator shown in Fig. 1. When the output of the comparator is logically "1", then VCO generates the clock driving the charge pump. However, it will end up with the output of the comparator being logically "0". Then, the output of the comparator will repeat "1" and "0". Consequently, the operation of the VCO becomes to be very unstable. It leads to a sharp noise into the whole circuit, and affects the performance of the system. In order to reduce the noise, a lowpass filter is inserted between the VCO and the

comparator.

The output from the lowpass filter is inserted into the input of the charge pump. The output voltage of the charge pump is determined according to the V_{ref} . The divider circuit is used for reducing the output of the charge pump, by which the magnitude of the output is compared with the V_{ref} . Fig. 2 is a circuit diagram of the VCO altering the output frequency depending on the magnitude of the input voltage of the VCO⁽⁷⁾. Its operation is similar to a ring oscillator. Thus, the VCO frequency is a linear function of the control voltage. The VCO output frequency, f_{clk} , V_{cont} is related to the VCO input voltage,

$$f_{clk} = \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \cdot V_{cont} + f_0 \quad (1)$$

Here, f_0 is the current frequency.

As the output of the charge pump is lower than the reference voltage, the operating frequency will increase. Otherwise, the frequency will decrease.

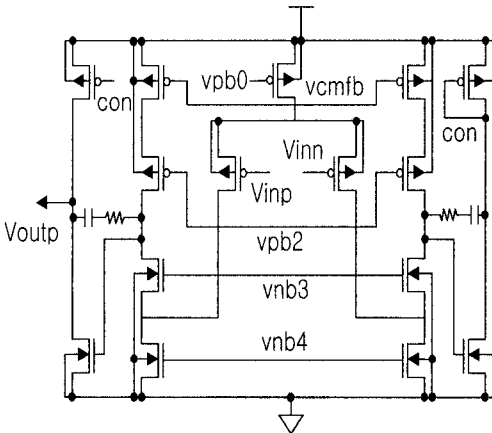


Fig. 3. A circuit diagram of comparator.

The comparator is shown in Fig. 3. The comparator is comprised of a folded cascode amplifier. The advantage of the

folded-cascode amplifier is that the minimum voltage limits the CMR(Common Mode Range) across the input differential amplifier.

Fig. 4 is a circuit diagram of one stage of a charge pump circuit⁽⁸⁾⁽⁹⁾. The charge pump circuit comprises multi-stages of booster stage CPs connected in series. A clk_a and a clk_b are applied to each booster stages CP_1 to CP_n . Each of the booster stages is identically configured.

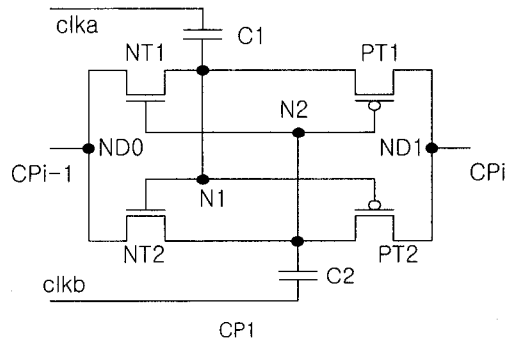


Fig. 4. A circuit diagram of one stage of charge pump.

In the first charge pump, the source of NMOS transistor NT_1 is connected to the node ND_0 , and the drain to the clk through the pumping capacitor C_1 . Similarly in the second charge pump, the source of NMOS transistor NT_2 is connected to the node ND_0 , and the drain to the clk_b through pumping capacitor C_2 .

Both charge pumps operate in a complementary manner, and raise potential of the second node relative to potential of the first node by transferring charge from the first node to the second. Each charge pump comprises a pumping capacitor, a NMOS transistor and a PMOS transistor. In each charge pump, the NMOS transistor is used to charge the pumping capacitor with charge input through the first node,

and the PMOS transistor is used to discharge the pumping capacitor to send charge to the second node.

The operation of the charge and discharge will continue until the magnitude of the V_{div} is higher than that of the V_{ref} . As soon as the V_{div} is higher than the V_{ref} , the output of the comparator will be abrupt. Then the operation of the VCO is suspended, and the output of the charge pump is not escalated anymore.

III. Results

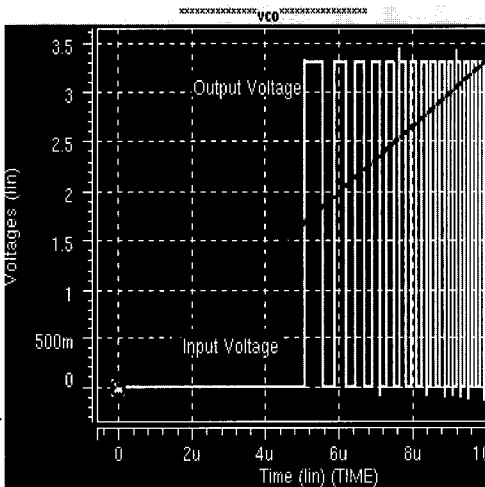


Fig. 5. A simulation result of VCO.

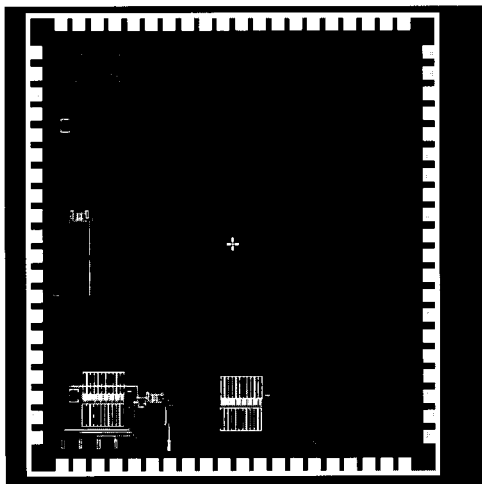


Fig. 6. A layout of charge.

Fig. 5 is the simulation result showing the changes of the clock frequency according to the magnitude of the control voltage. The result shows that the VCO modifies its frequency in accordance with the magnitude of the input voltage

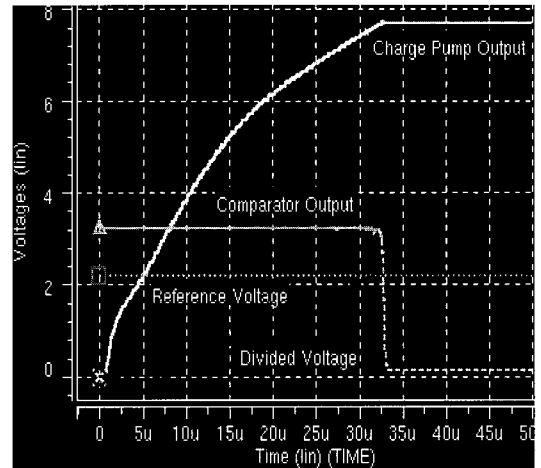


Fig. 7. A simulation result of charge pump.

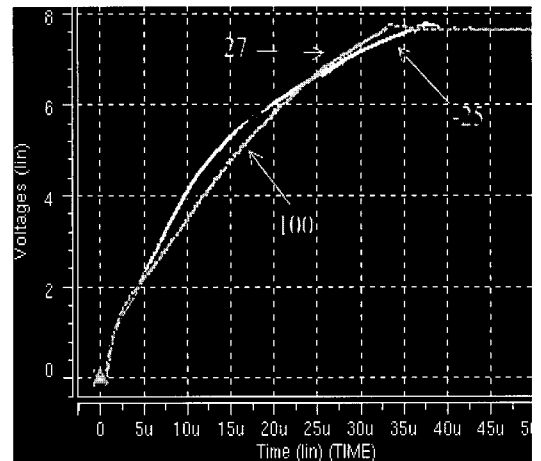


Fig. 8. Corresponding outputs on three different temperatures.

The layout of the charge pump and the simulation result of the charge pump are shown in Fig. 6 and Fig. 7, respectively.

As shown in Fig. 7, the output of the

comparator continues to be high until the V_{div} overcomes the V_{ref} . However, the output of the charge pump abruptly stops to increase as soon as the output of the comparator is off. Fig. 8 shows the variation of the outputs from the charge pump on three different temperatures (-25°C , 27°C , 100°C). It indicates that the temperature variation does not influence the output voltage of the charge pump.

IV. Conclusion

The charge pump proposed in this paper is simulated with Hynix 0.35um CMOS process parameters. The charge pump is designed to adjust the output voltage according to the reference voltage. Thus, the proposed charge pump with VCO can generate a variety of programming voltages depending on the reference voltage. Moreover, the temperature and the supply voltage variation do not influence the output voltage of the charge pump because the output of the charge pump depends only on the V_{ref} .

The charge pump circuit for generating several high programming voltages can be applied to a sensor system using the neural networks implemented with the analog memory.

Acknowledgements

The present research has been conducted by the Bisà Research Grant of Keimyung University in 2001, and the IDEC.

References

[1] J. Huang and M. Hagiwara, A Multi-Winner Associative Memory, IEICE Trans. INF & SYST., vol.

E82-D, No.7, pp. 1117-1124, July 1999.

[2] T. Shibata and T. Ohmi, Neuron MOS Binary-Logic Integrated Circuits, IEEE Trans. on Electron Devices, Vol 40, No. 3, pp. 570-576, March 1993.

[3] P. Hasler, T. Stanford, B.A. Minch, and C. Diorio, An Auto-zeroing Floating Gate Second-Order Section, Proceedings of IEEE International Symposium on Circuits and Systems, Monterey, 1998.

[4] R. R. Harison, P. Hasler, and B.A. Minch, Floating-gate CMOS analog memory cell array, Proceedings of IEEE International Symposium on Circuits and Systems, Monterey, 1998.

[5] Richard J. McPartland and Ranbir Singh, 1.25Volt, Low Cost, Embedded Flash Memory for Low Density Applications, IEEE 2000 Symposium on VLSI Circuits Digest of Technical Papers.

[6] John F. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," IEEE J. Solid-State Circuits, vol. 11, pp. 374-378, June 1976.

[7] R. Jacob Baker, Harry W. Li, and David E. Boyce, CMOS Circuit Design, Layout, and Simulation, IEEE Press, Piscataway, 1997.

[8] Jahanshir J. Javanifard., and Marc E. Landgraf, "Charge pump circuit for providing multiple output voltages for flash memory," U.S. Patent 5483486, Jan. 1996.

[9] Kazuhiko Fukushima, Atsuo Yamaguchi, "Charge pump circuit," U.S. Patent 6107864, Aug. 2000.

 著 者 紹 介

**Yong-Yoong Chai**

Date of Birth: Aug. 16,
1958

1978~ 1985 Sogang
Univ. Electronics Engr.
(Bachelor)

1988~ 1991 Oklahoma

State Univ. Electrical Engr. (Master)

1991~ 1994 Oklahoma State Univ. El-
ectrical Engr. (Ph. D)

1985~ 1988 LG Telecommunication Ltd.

1995~ 1997 Samsung Semiconductor Ltd.

1998~ Present Keimyung Univ. Electr-
onics Engr. (associate professor)

Main Interest Field : Analog Memory,
Mixed Signal VLSI

**Eun-Hwa Jung**

Date of Birth: Jan. 15.
1979

1997~ 2001 Keimyung
Univ. Electronics Engr.
(Bachelor)

2001~ Present Kei-

myung Univ. Electronics Engr. (Master)

Main Interest Field : Mixed Signal
VLSI