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Design of a CMOS On-chip Driver Circuit for Active Matrix Polymer Electroluminescent Displays

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Abstract

A CMOS driving circuit for active matrix type polymer electroluminescent displays was designed to develop an on-chip microdisplay on the single crystal silicon wafer substrate. The driving circuit is a conventional structure that is composed of the row, column and pixel driving parts. 256 gray scales were implemented using pulse amplitude modulation method. The 2-transistor driving scheme was adopted for the pixel driving part. The layout was carried out considering the compatibility with the standard CMOS process. Judging from the layout of the driving circuit, it turns that it is possible to implement a high-resolution display about 400 ppi resolution. Through the HSPICE simulation, it was verified that this circuit is capable of driving a VGA signal mode display and implementing 256 gray levels.

Keywords : active matrix, polymer EL display driving circuit, CMOS logic, MEH-PPV, pulse amplitude modulation

1. Introduction

Polymer Electroluminescent Display (PELD) is one of the most promising flat panel display technologies. I has many advantages, such as simple structure, high resolution, large viewing angle and low driving voltage. Especially, the active matrix (AM) type is more attractive than passive matrix type. This property results from the fact that AM type driving circuit can have lower peak current and voltage because it is able to continue providing current after the addressing period [1].

Although the AMPELD, which that is driven by thin film transistor (TFT) on the glass substrate, has attracted many researchers [2,3], the MOSFET on the single crystal silicon wafer is superior to the TFT on the glass substrate. This is because the MOSFET has higher current driving capability, higher speed, lower parasitic element, and lower leakage current [4-6].

In this work, after the fabrication of the polymer light emitting device for the driving circuit, the driving circuit for the VGA mode monochrome AMPELD on the silicon substrate was designed using CMOS logic, in order to implement the micro-display that is characterized by high resolution and high gray scale.

2. Fabrication of Polymer Light Emitting Diode and its Model

To design a display driving circuit, it is a polymer light emitting diode (PLED) model must be used for the circuit simulation. In order to provide design parameters, PLEDs were fabricated and their electrical modeling was achieved.

For PLEDs, the MEH-PPV (Poly(2-methoxy-5-(2-ethylhexyloxy)-1, 4-phenylene vinylene)) was used as a

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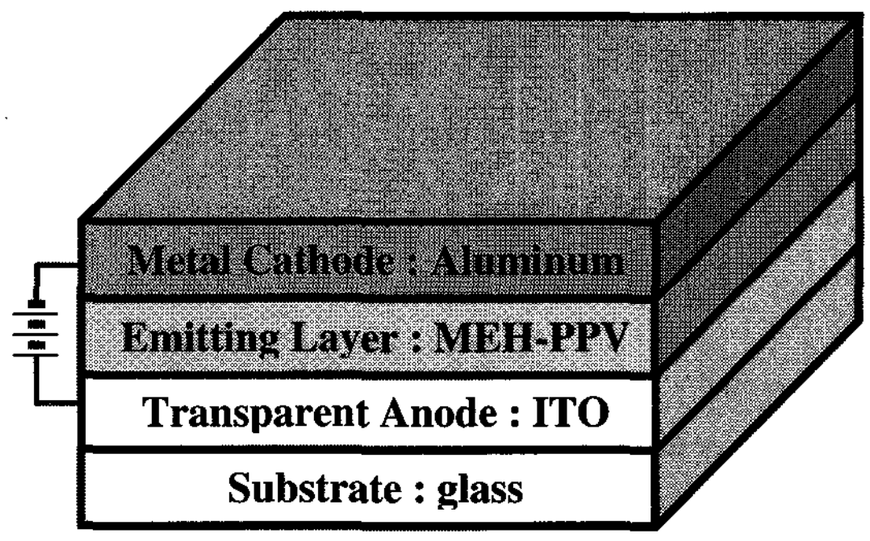
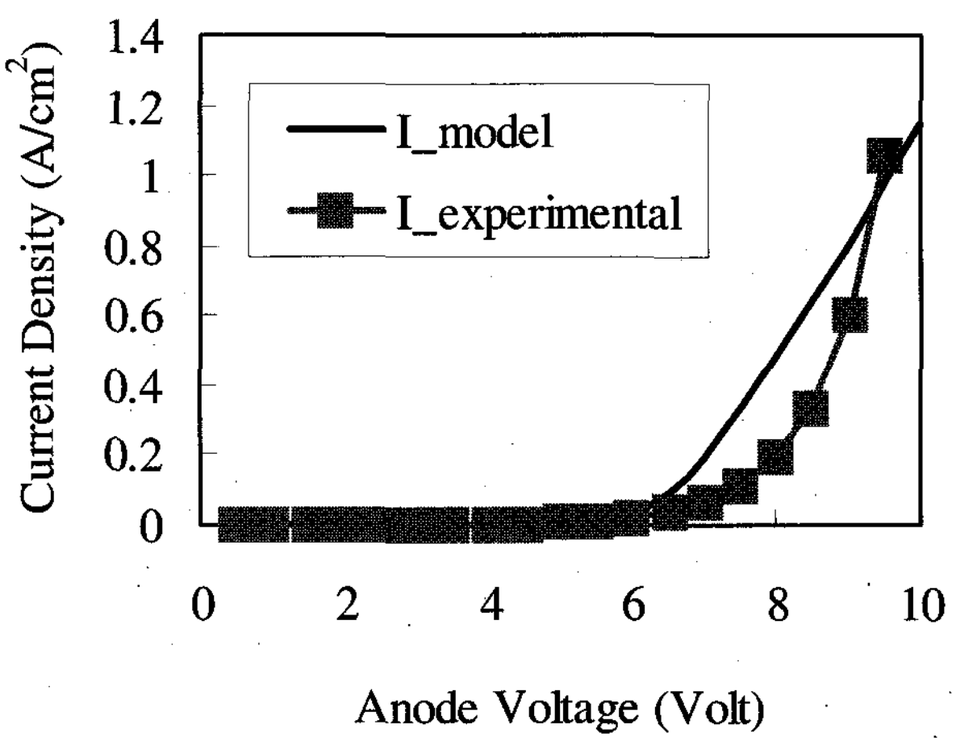
light emitting material. Its structure was ITO/MEH-PPV/Al having no transporting layer, as shown in Fig. 1 (a). MEH-PPV was spin-coated on the ITO glass substrate that was patterned by the photolithography, and the metal layer was evaporated using the shadow-masking method. Considering the compatibility with the standard CMOS process aluminum (Al) was used as the metal cathode.



(a)



(b)

Fig. 1. (a) The structure of the fabricated polymer light emitting diode (Aluminum/MEH-PPV/ITO) (b) the I-V characteristics of the fabricated polymer light emitting diode and its electrical model for the circuit simulation.

From the fabricated PLED, the current-voltage characteristic was obtained using the 4155A semiconductor parameter analyzer. The filled dots in Fig 1 (b) are the experimental data for the fabricated PLED. The turn-on voltage is about 5 V and the voltage range of the light emission is about 5~10 V. The solid line in Fig 1 (b) shows the I-V curve of the electrical model that is generated by properly combining and modifying the existing diode model. Since the circuit simulation tool does not support the PLED model, this electrical model was used, especially for the pixel driving circuit design so that more accurate implementation of the gray scale.

Although there exist some discrepancy in the current value between the measured and model-simulated data, it does not affect the gray scale much as the light intensity is proportional to the current flowing through the PLED. In other words, if the circuit is designed to control the PLED current directly, the error in the current value for the specific voltage between the experimental data and the simulation data would not cause any problem, but may merely cause slight difference with respect to the PLED voltage.

3. Circuit Design and Simulation Result

The circuit design was performed at the transistor level using CMOS logic and its validity was verified by HSPICE simulation. The MOSFET level 3 model was used for the circuit simulation. The layout of the designed circuit was accomplished using the conventional 1.5㎛ CMOS design rule. Double metal, single poly layer, and n-well technologies were used for implementing 5 V CMOS devices.

3.1 The system configuration

Fig. 2 shows the overall system configuration of an active matrix PELD driving circuit. The circuit is composed of three parts: row, column, and pixel driving circuit on the same substrate.

After the circuit using a standard CMOS process as shown in Fig. 3 is fabricated, the light emitting polymer (LEP) thin film can be formed by spin coating method and the ITO layer can be deposited. It is through these processes, the CMOS on-chip polymer EL display on a silicon substrate can be implemented.

Since the circuit is fabricated using bulk CMOS technology with a relatively small minimum feature size, very small pixel can be implemented. This means that the display fabricated through this method is benefcial as a high resolutioin display with small size.

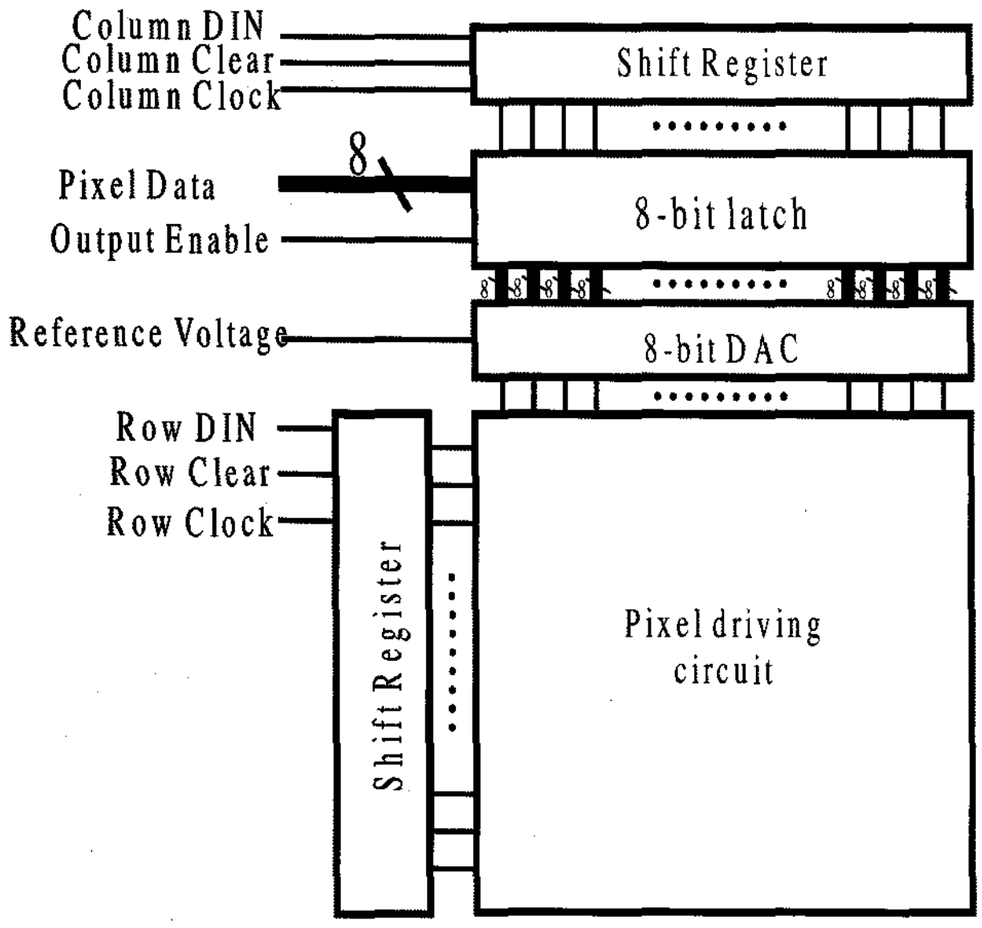


Fig. 2. The system configuration of polymer electroluminescent display driver circuit. It is composed of the row, column, and pixel driving circuit.

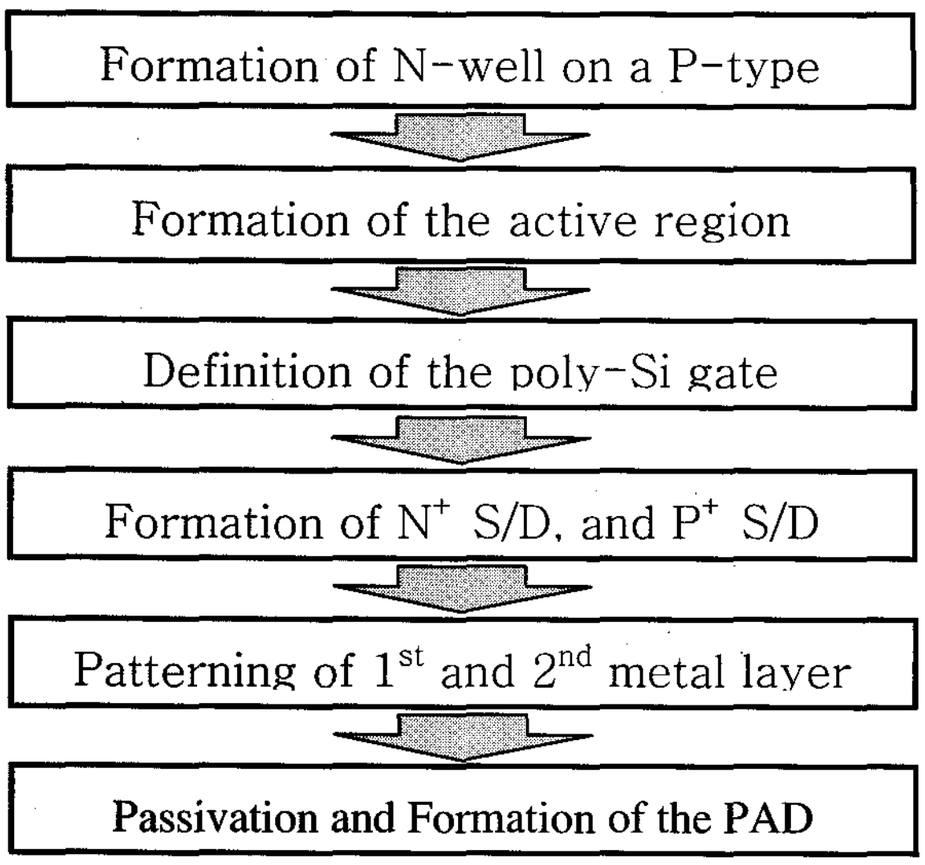


Fig. 3. The flow chart of the standard CMOS fabrication process.

3.2 The row and column driving circuit

Shift registers in the row and column driving circuits are the serial chain of pseudo-static two-phase dynamic D flip-flop [7], as shown in Fig. 4. The shift register in the row driver selects each row one after the other, and the one in the column driver enables each latch to store the pixel data.

The 8-bit latches in the column driving circuit hold each pixel data entering the column driver during the row addressing time. When the 'Output Enable' signal (Fig. 2) is arrived, all of the pixel data that are stored in each latch are supplied to each column.

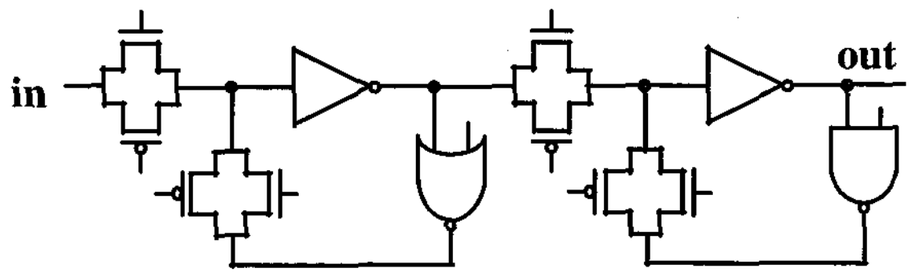


Fig. 4. The pseudo-static two-phase dynamic D flip-flop.

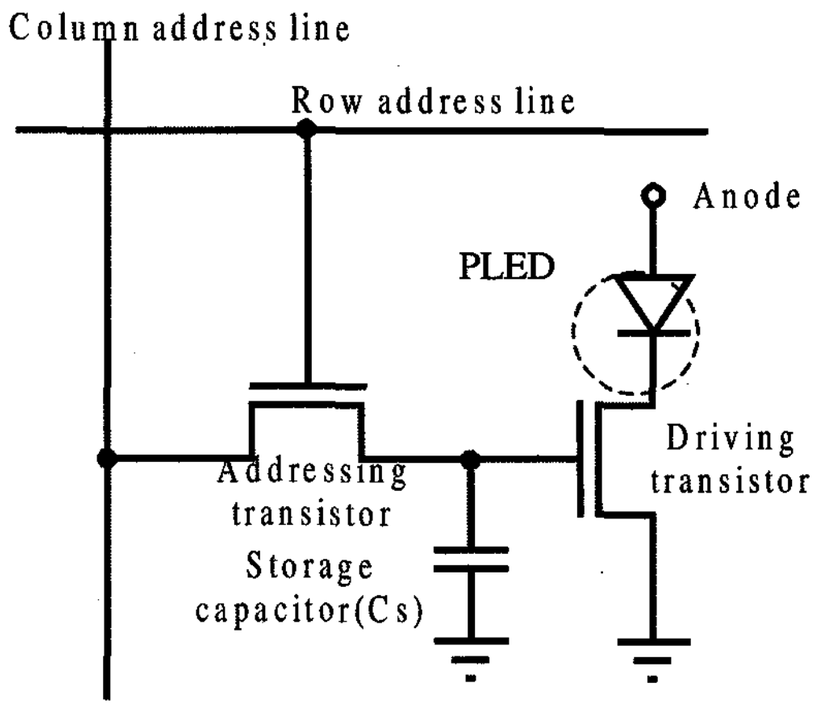
To implement 256 gray levels using the PAM (Pulse Amplitude Modulation) method, the 8-bit digital-to-analog converter (DAC) was used [8]. As a DAC circuit, the R-2R ladder type one implemented using PMOSFET was adopted due to its simplicity and effectiveness.

Such type of driving circuit has a weak point in that it consumes a larger silicon area than the analog data driving circuit type that has a common DAC because of the 8 bit latches and 8 bit DACs in each column line. But the DAC circuit in this type of driving circuit does not need to be so fast because the latch in each channel is able to hold the pixel data during one row time. It also allows us to design the DAC circuit more easily.

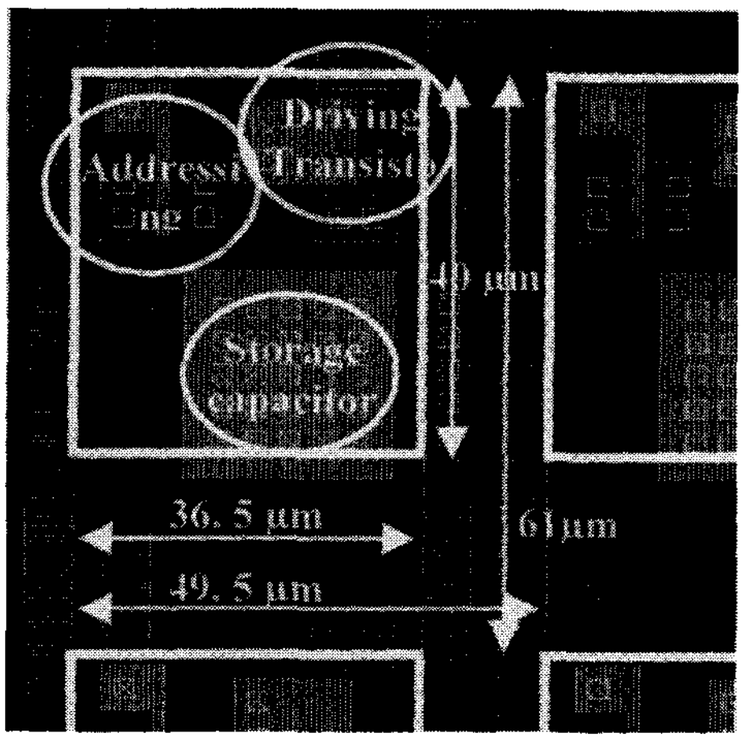
3.3. Pixel circuit design

Fig. 5 (a) shows the schematic diagram of the pixel-driving circuit including the circuit model of the PLED. It is composed of 2 transistors and 1 storage capacitor. This structure is conventional and relatively simple [9]. Fig. 5 (b) shows the layout of the pixel circuit. The pixel size is small enough to implement 400 ppi display with high resolution. The aperture ratio is about 48 %, this value is higher than that of the recent TFT-PELD which adopts bottom emission method [2]. But, as a top emission method display, has comparatively low value, which is the result of by the 1.5 μm design rule of the standard CMOS process.

In order to maintain compatibility with the standard CMOS process, the 2nd metal layer was used as the metal cathode electrode of the PLED, and the PAD layer was used to form a hole so as to connect the cathode and polymer, as shown in Fig. 6. Therefore, it is possible to implement on-chip polymer electroluminescent display by spin coating the light emitting polymer and the deposition of transparent common anode (ITO) after the circuit fabrication.



(a)



(b)

Fig. 5. (a) The pixel driving circuit, and (b) its layout pattern. It is composed of 3 parts, an addressing transistor, a driving transistor and a storage capacitor.

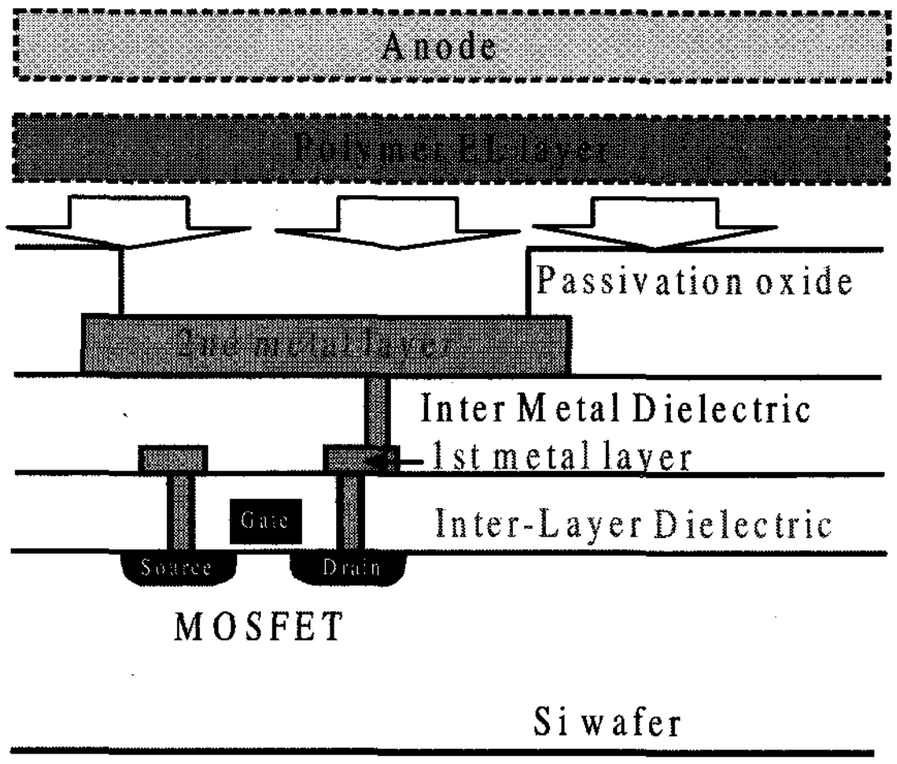
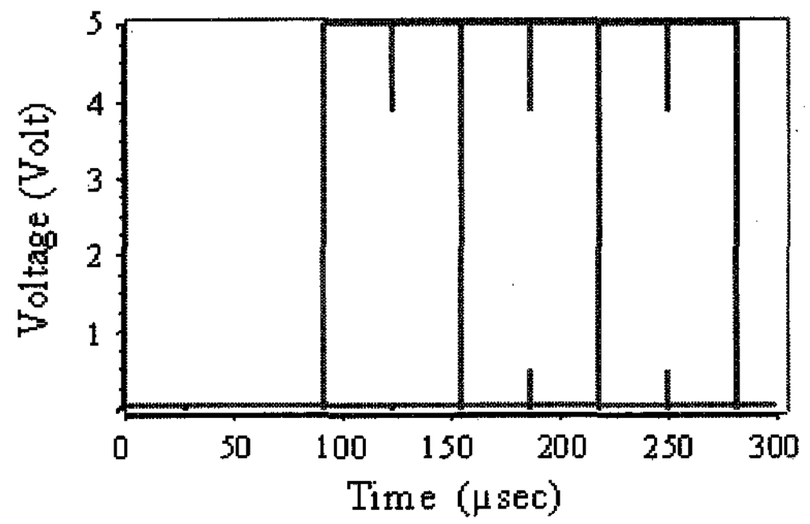


Fig. 6. From the light-emitting layer forming process after the standard CMOS circuit fabrication process, the CMOS on-chip polymer EL display can be implemented.

3.4. Simulation result

Through the HSPICE simulation, the proper performance of AMPELD driving circuit was verified. Because the circuit drives VGA mode signal, the shift register in the row driver operates on 28.8 kHz, while the one in the column driver operate on 25.2 MHz. Fig. 7 (a) shows that the shift register in the row driving circuit selects each row at an appropriate speed. Fig. 7 (b) shows that the one in the column driver satisfies the operation speed specification 25.2 MHz.



(a)

(b)

Fig. 7. The simulation results of (a) the shift register of the row driving circuit, and (b) the one of the column driving circuit.

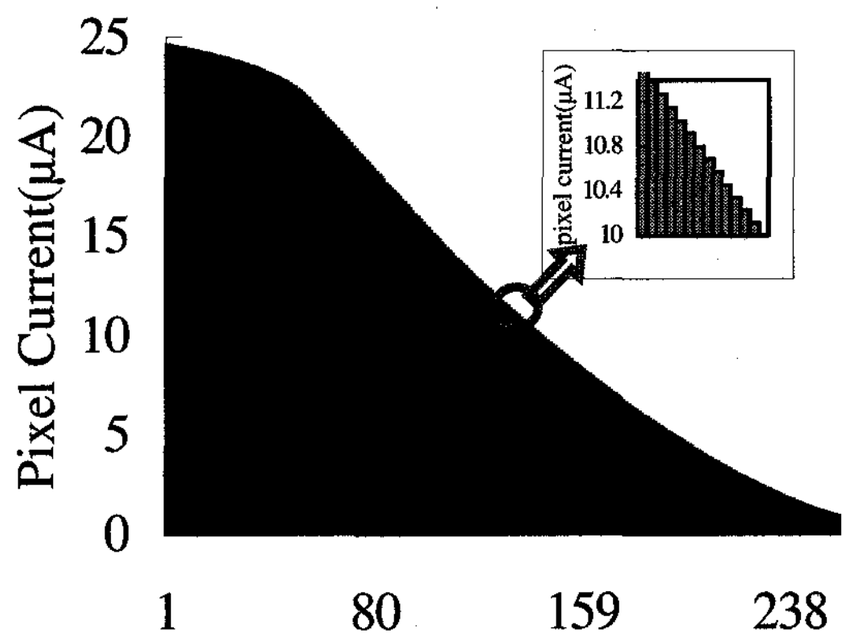


Fig. 8. The characteristics of the digital-to-analog converter. The driver circuit can implement 256-gray scale well.

Fig. 8 shows the current that flows through the PLED when the 8-bit input code of the DAC circuit decreases from hexadecimal FF to 00. The driver circuit provides relatively linear 256-gray scale. The inset shows the local linearity of the gray scales. However, the curve is not a straight line, which is due to the nonlinearity of the PLED itself.

To implement the gray scale more accurately, it must be considered whether the threshold voltage of the driving transistor can be varied. From the simulation, it was predicted that the threshold voltage variation under 5 mV could guarantee the accurate implementation of a gray level.

4. Conclusions

A driving circuit for the CMOS on-chip active matrix polymer ELDs is designed using the CMOS logic in order to maintain its compatibility with the conventional 1.5 μm CMOS process. For the driving circuit design, the polymer light emitting diode was fabricated and characterized. Using the HSPICE simulation, the designed circuit was confirmed to drive VGA mode displays, and enables 256 gray levels and high resolution of 400 ppi successfully.

Acknowledgement

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