論文2002-39SD-9-3

연결선 특성과 신호 무결성에 미치는 밑층 기하구조 효과들

(Underlayer Geometry Effects on Interconnect Line Characteristics and Signal Integrity)

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요 약

실리콘 기판과 교차하는 금속 선의 밑층 기하구조를 고려한 연결선로의 특성이 정교하게 고안된 패턴을 가지고 실험적으로 분석되었다.이 작업에서, 여러 종류의 밑층 기하구조에 따른 전송선로을 위한 테스트 패턴들을 고안하 였고,신호 특성과 반응은 S-parameter 와 TDR을 통해 측정되었다. 사용된 패턴은 두개의 알루미늄 선과 한 개의 텅스텐 선을 가지는 deep-submicron CMOS DRAM 기술을 가지고 설계되고 제작되었다. 패턴위에서 측정되 결과 분석으로부터, 라인 파라메터들 (특히 라인 커패시턴스와 저항) 과 그것들에 의한 신호 왜곡에 대한 밑층 구조에 의한 효과는 무시 할수 없음을 발견하였다. 그러한 결과는 고속 클럭과 데이터 라인 같은 글로벌 신호 선이나 패키지 리드의 스큐 발렌스의 심도있고 유용한 이해에 도움이 된다.

Abstract

Characteristics of interconnect lines considering underlayer geometries of a silicon substrate and crossing metal lines are experimentally analyzed through elaborately devised patterns. In this work, test patterns for transmission lines having several kinds of underlayer geometries were devised, and the signal characteristics and responses are measured by S-parameter and time domain reflection meter (TDR). The patterns were designed and fabricated with a deep-submicron CMOS DRAM technology having 1 Tungsten and 2 Aluminum metals. From the analysis of measured results on the patterns, it is founded that the effects of underlayer line structures on line parameters (especially line capacitance and resistance) and signal distortions occurred from them cannot be negligible. The results provide useful and insightful understanding in the skew balance of package leads and global signal lines such as high-speed clock and data lines.

Key Words : *interconnect, s-parameter, substrate effect, current return path*

Ⅰ. Introduction

To enhance the performance of the high-speed integrated circuit systems, interconnect lines on a chip and a package are becoming one of key design factors. In order to minimize signal distortion and skew due to propagation delay and dispersion, the exact electrical properties of interconnects must be considered in on-chip and off-chip devices in high frequency operation. Therefore, since the signals, especially in clock signal, tend to exhibit the short

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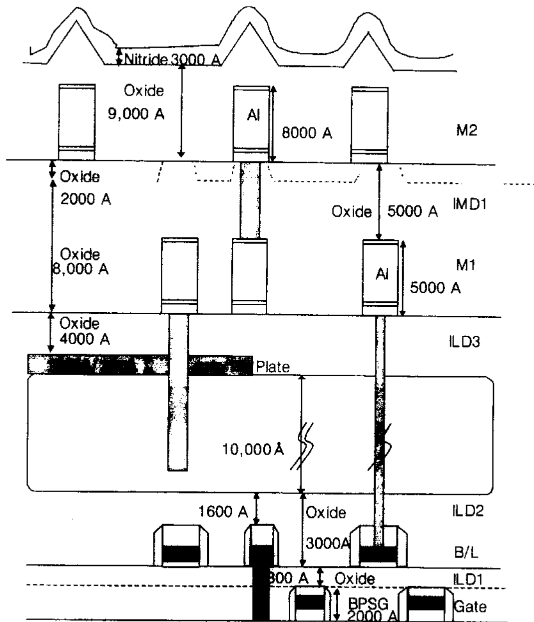
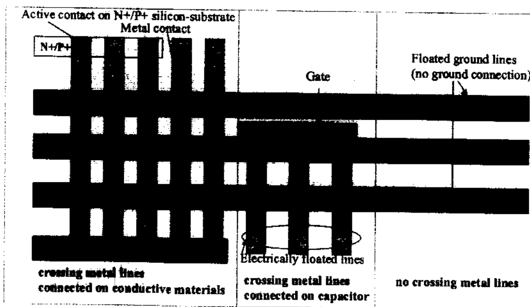
接受日字:2002年4月17日, 수정완료일:2002年8月13日

rising and falling times, it is necessary to analyze and model the complicated real line systems with high frequency characteristics of the interconnects through measurements. Among the problems associated with the high performance interconnect lines, the crosstalk noise between the intralayer lines on silicon substrate are studied.[1] But the underlayer geometry effects on the signal fidelity are not sufficiently investigated with S-parameter measurements and high-speed performances points.[2] Figure 1 (a) shows cross sectional geometries of metal lines and underlayer interconnects for a deep-submicron (DSM) CMOS DRAM technology having 1 Tungsten and 2 Aluminum metals. Generally, the topological structures of lines on real chips can be tentatively distinguished into three categories based on the existence of under metal layers and ground contacts as shown in figure 1(b). The first group consists of the structures of underlayer metal lines having at least one ground contact at one end. The second group consists of the structures having floated underlayer lines such as dummy patterns and signal lines that are connected between a gate and an isolated drain/source. The last group is devised for the structures having no underlayer metal lines on silicon substrate. Package leads also have the underlayer structures consisting of the similar underlayer geometries as referred in Fig. 1. Therefore, the results can be applied to MCM (Multi-Chip Module) lines and package leads for analyzing of the characteristics.



(a)



(b)

그림 1. deep-submicron CMOS DRAM technology을 위한 간단한 신호선 토폴로지, (a) 단면 (b) 정면도

Fig. 1. Brief signal line topologies for a deep-submicron CMOS DRAM technology, (a) a cross-sectional view and (b) a top view.

For analyzing and understanding the effect of realistic underlayer geometries on such signal lines, five basic structures of underlayer geometries were devised with a DSM DRAM technology. The S-parameter measurements were performed with an HP 8720B two ports network analyzer in frequency range from 300MHz to 20GHz. The de-embedding method was performed with[3] and TDR test was also performed for analyzing the measured delay responses as referred in.[4]

II. Experiment Preparation and Measurement

For the characterization of the interconnects, as shown in figure 2, the effects of underlayer geometries on the parameters of the upperlayer interconnects were observed with three patterns: crossover metal 1 lines (TP1) connected with ground,

(TP2) stayed at floating line states, and (TP3) connected with imperfect ground having finite resistance as silicon substrate. And the other two structures have the grounded shielding lines (TP4) and the isolated shielding lines (TP5) without crossing metal 1 line structures, respectively.

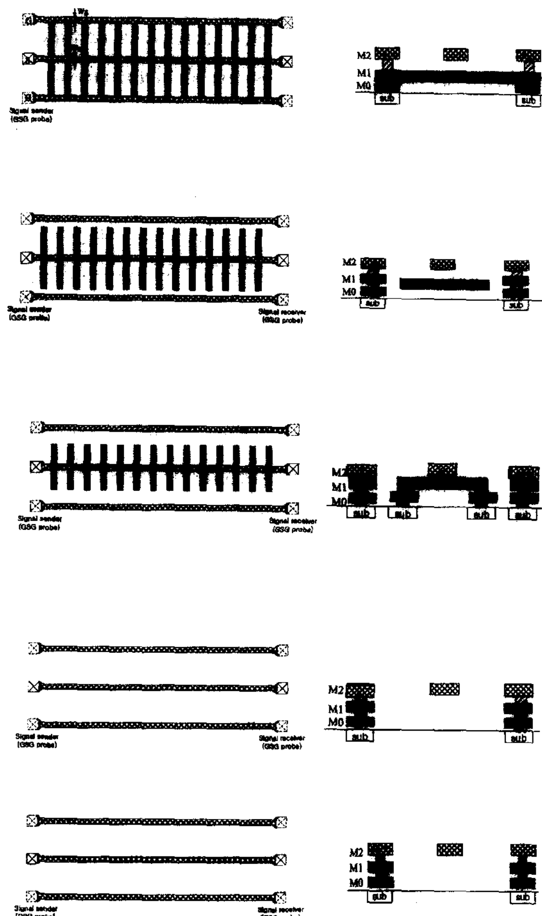


그림 2. GSG probe를 사용을 위한 다른 밑층 기하구조을 가지는 단일 선 측정 패턴들. 중앙 신호선 (Ws)과 접지 선들(Wg)의 너비는 각각 4μm와 20μm로 고정되어 있다.

Fig. 2. Single line test pattern structures having different underlayer geometry structures for the use of GSG probes. Widths of Single center signal lines (Ws) and ground lines (Wg) are fixed at 4μm and 20μm, respectively.

For this work, we devised the patterns of a MIS coplanar structure where two ground lines are connected to the silicon substrate (except for TP5 for floating silicon substrate effect) and the signal line is located at the center between these ground lines. The widths of signal and ground metal 2 lines are fixed at 4μm and 20μm, respectively. The space of all the patterns between signal line and ground lines is fixed, and the patterns were fabricated with a 1-poly and 3-metal (1 Tungsten and 2 Aluminum) DSM DRAM CMOS technology. The measurements at the high frequency were performed on the patterns through the network analyzer, TDR/T, and coplanar microwave probes with 50 Ω terminated impedance. The pad-to-pad pitch is fixed at 150 μm. The pitch of underlayer lines is 10μm, and the width and space of the lines are 1um and 9um respectively.

Ⅲ. Measurement Results

After subtracting the capacitive effects of the contact pads from the S-parameters, the complex characteristic impedance and complex propagation constant were extracted. Figure 3(a) and 3(b) show the real and imaginary parts of the characteristic impedance and the attenuation constant of each pattern as a function of frequency, respectively. Figure 3(c) shows the propagation constants affected by underlayer patterns. In the measured results, characteristic impedances of TP1 have smallest impedance values than those of other patterns. The existence of crossover metal 1 lines also makes effects on the attenuation constant and the phase velocity. Figure 3 clearly shows that the line characteristics of the upper signal lines are dependant on the crossing underlayer metal lines and their connected ground types. Most notice that attenuation constant of TP1 has the smallest level over all frequency ranges. Phase velocity of TP 2 and TP3 shows no difference between imperfect ground and floating line while frequency increases. TP4 and TP5 have a similar characteristic from this standpoint of phase velocity and attenuation constant.

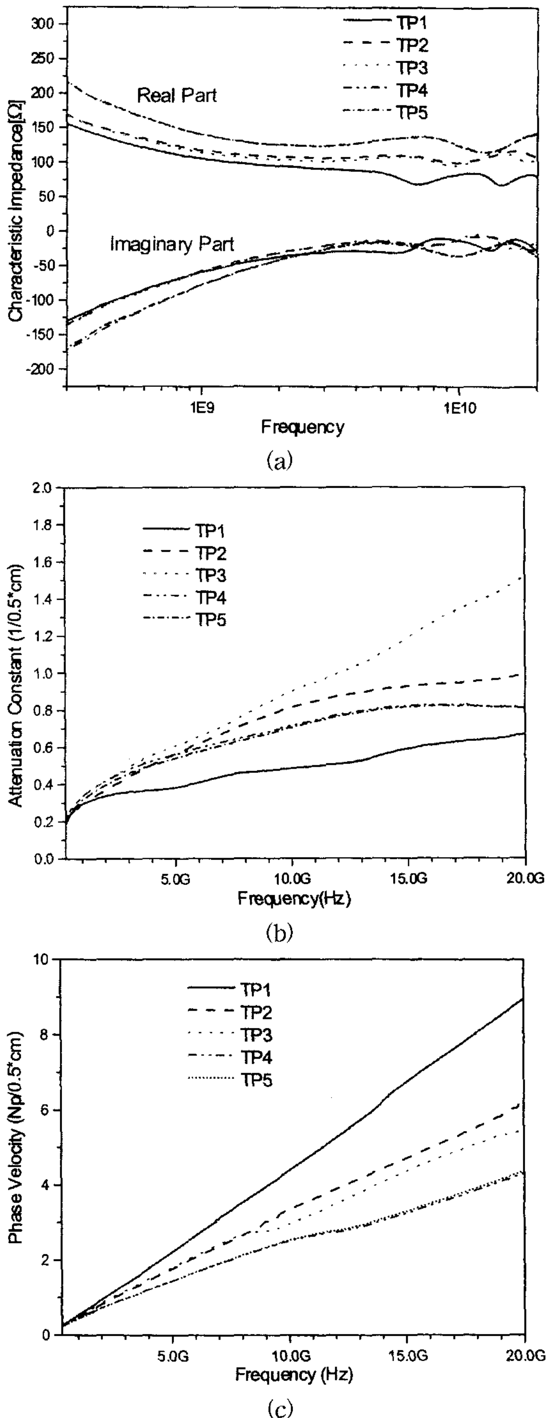


그림 3. 다섯 가지 다른 밑 구조를 가지는 신호선들을 위한 (a) 측정된 콤플렉스 특성 임피던스 상수, (b) 감쇄, (c) 전파 상수

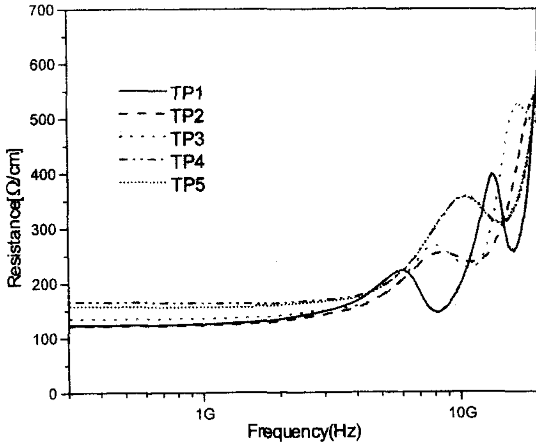
Fig. 3. (a) Measured complex characteristic impedance constant, (b) attenuation, and (c) propagation constant on signal lines having five different underlayer structures.

As a result, imperfect ground can be one of major factor on the signal attenuation by dissipating the accumulated charge on crossing underlayer metal line. Also, the TP1 has the largest phase velocity by the increased crossover capacitance, which can induce from the $(LC)^{1/2}$ flight time delay. Briefly summarizing, the line characteristics of the patterns can be sorted into the three groups according to typical underlayer geometries for all frequencies.

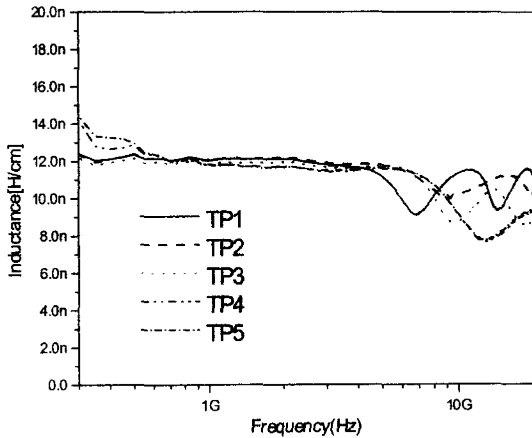
The line parameters (R′, L′, C′, and G′) were also extracted and analyzed from the results of S-parameter measurement. Figure 4 shows the measurement results of resistance (R′) and inductance (L′) for each pattern in frequency domain. The measured resistance of signal line is 99~102 Ω for the line length of 1 cm. But the extracted resistance of the patterns from S-parameter measurement is larger than that from DC measurement since the S-parameter-based measured resistance includes not only the additional AC resistance factors by metal skin effect and proximity effect but those by current return paths as following[4,5]:

$$R' \cong Rs + \alpha^2 Rg + (1-\alpha)^2$$

where Rs, Rg, and Rm are resistance of signal line, total ground lines, and effective path on substrate, respectively. The α is defined as the ratio of the current through ground lines over signal lines as shown in ref[5] As a result, resistances of TP4 and TP5 can have larger resistance values than those of TP1 and TP2, and TP3 owe to Rm occurred by return currents through substrate. The increased resistance also affects the signal properties by increasing RC delay, as shown in Fig. 8. The resonance of resistance shows the frequencies over 6GHz for all patterns. In case of inductance, the values are measured to 12nH/cm for all patterns. Inductances of patterns also have the similar resonant frequencies to the resistances shown in Fig. 4(b).



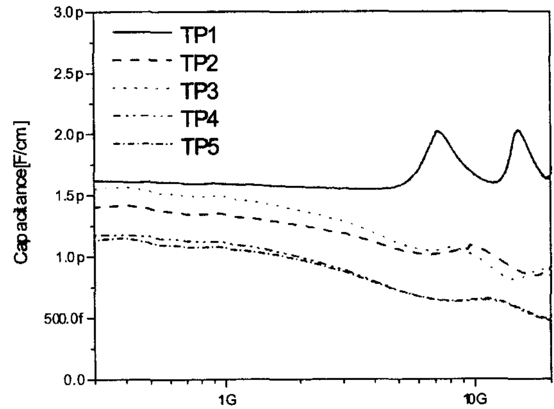
(a)



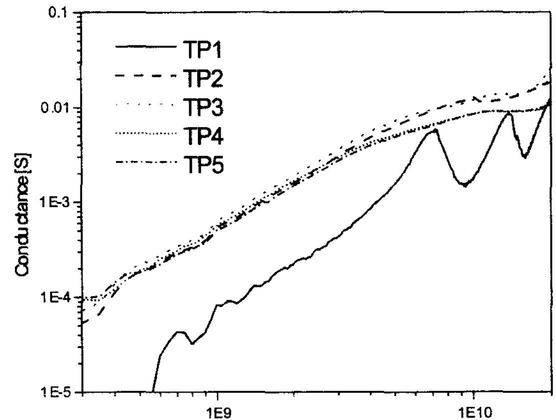
(b)

그림 4. (a) 저항 과 (b) 인덕턴스
Fig. 4. (a) Resistance and (b) inductance.

Figure 5 shows the characteristics of admittances for each pattern as a function of frequency. The capacitances in figure 5(a) are strongly affected by underlayer structures as frequency increases. TP 2 and TP3 have the similar capacitance values in the range of high frequency over 5~6GHz. At low frequency, however, TP3 has similar capacitance values of TP1. TP4 and TP5 also show similar phenomena. These results mean that imperfect ground can act as floating in the range of high frequency. TP1 does not show the frequency-dependant characteristic in capacitance under the resonant frequency of ~6GHz. In the case of conductance, TP1 has the lowest level for all frequency. The loss (G′) in silicon substrate or underlayer metal lines shows almost the same characteristics as TP2(=TP3), TP4(=TP5), and TP1. The capacitance (C′) also shows the frequency-dependant decrease for patterns having the imperfect ground and substrate except for TP1. In figures 5(a) and 5(b), we found that the signal characteristics on five geometries also can be affected by frequency-dependant admittances.



(a)



(b)

그림 5. (a) 커패시턴스와 컨덕턴스
Fig. 5. (a) Capacitance and (b) conductance.

Ⅳ. Transient Responses

Figure 6 shows a brief diagram for extracting and verifying the S-parameter-based line parameters at high frequency range. The verification of line

parameters is required to compare the signal responses by TDR/TDT with the SPICE circuit simulations using the S-parameter-based extracted line parameters. Figure 7 shows the measurement environment of time transient responses. In this configuration, the axial cables between TDR meter and device under test (DUT) have the impedance of 50 Ω and a length of 1m. Test source impedance and termination impedance are fixed at 50 Ω respectively. The transient input rising time (10%-90%) and amplitude of TDR meter are given by the specification, about 65 psec and 250mV, respectively. Figure 8 shows the transient responses of the measured signal for the different underlayer geometry patterns (TP1~TP5) on the 0.5cm input signal line with the rising time of 65psec. Scaled input is measured on the shorted de-embedding pad pattern. The measured and simulated results in figure 8 also show several signal responses by different underlayer geometries. Signal transient response of TP1 shows the long delay time since flight delay of a pattern is proportional to inductance and capacitance as shown in figure 5(a). However, the measured resistance of TP1 is smallest value and its slew rate has the steepest value than those of other patterns. As shown in figures 3, 4 and 5, the line parameters make the fast responses in case of TP1 and TP2, however rising times of response signals show the slow values because of their large resistances. The response difference between TP1 and TP5 shows a value around ~22psec. The figures show that the signal responses can categorized to three groups: TP1, TP2/TP3, and TP4/TP5. In conclusion, the frequency-dependant admittance can make a big disturbance of signal integrity according to underlayer geometries, and imperfect ground effect of crossing metal 1 lines can make the worst signal properties than that by silicon substrate effect. Therefore, real signal lines can show the worse signal properties as expected through the SPICE simulations since imperfect grounding of crossing metal 1 lines can deteriorate the signal characteristics.

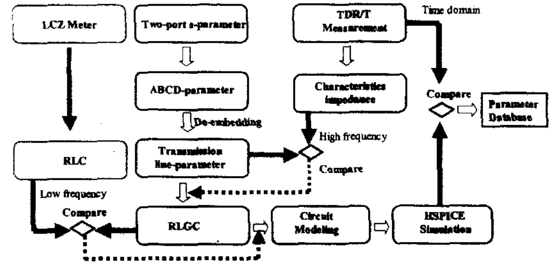


그림 6. 전기 상수 추출 및 검증을 위한 간단한 표준 다이아 그램

Fig. 6. Brief standard diagram for extracting and verifying electrical parameters.

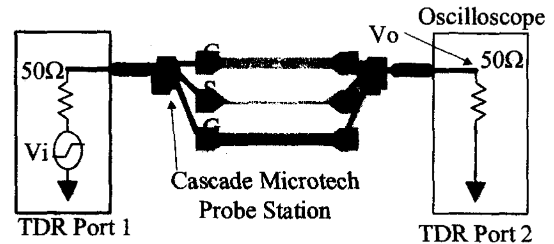


그림 7. 회로의 시간 전이 반응을 위한 테스트 환경

Fig. 7. Test configuration for time transient responses of circuit.

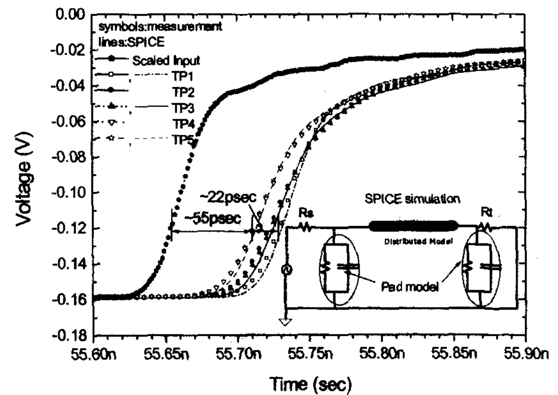


그림 8. 5mm 길이의 신호선에서 65psec의 상승 시간을 가지는 신호를 위한 측정 및 시뮬레이션 신호 전이 반응

Fig. 8. Measured and simulated signal transient responses at 5mm long line for the input signal having the rising time of 65psec.

V. Circuit Implementations

Figure 9 shows a process-dependant empirical

expression for capacitances of metal 2 lines as a function of densities of underlayer metal lines. Typical value of a coefficient factor "A" in term of (-expression was obtained around 2.45~2.5 for this tested process. Effects of metal 1 line density on the capacitance C2 are clearly increasing and maximized near about 20% as shown in figure 10. The wire density is defined as

$$wire\ density = \frac{\sum W_i}{\sum (W_i + S_i)} \quad \text{and} \quad lg = \sum (W_i + S_i)$$

where Wi and Si are width and space of crossing underlayer metal lines at i-section of an upper global line with length of lg. The wire density can be expressed through a concept of the effective density.

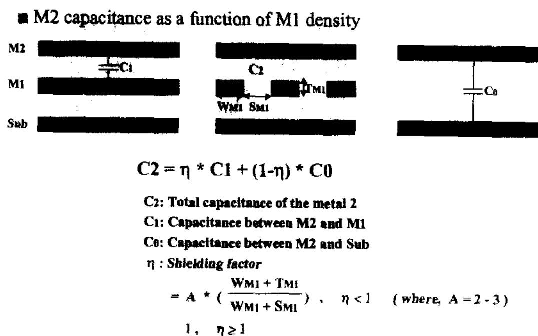


그림 9. 밑층 금속 선의 밀도 함수로 표시된 윗층 금속 선의 효과적 커패시턴스

Fig. 9. Effective capacitance of upper metal layer (M2) as a function of densities of underlayered metal lines.

As shown in figure 10, the metal 1 lines having at least the wire density of 20% can electrically shield the metal 2 lines from silicon substrate or poly lines in the given process. The coefficient "A" in a shielding factor is obtained to 2.46 for the best fitting. Generally in commercial high-density DRAM chips, metal 1 density on global data lines does not be exceeded over 20%. However, it is hard to clearly define or obtain the wire density in real chips so that designers must consider the timing margins having line skews by underlayer effects. For this, we must clearly understand the frequency-dependant line characteristics at the range of high frequency. The analysis of test patterns shows that the global lines having underlayer wire densities over 20% can be separately modeled to constant inductance and capacitance within interested frequency ranges about 5~6GHz.

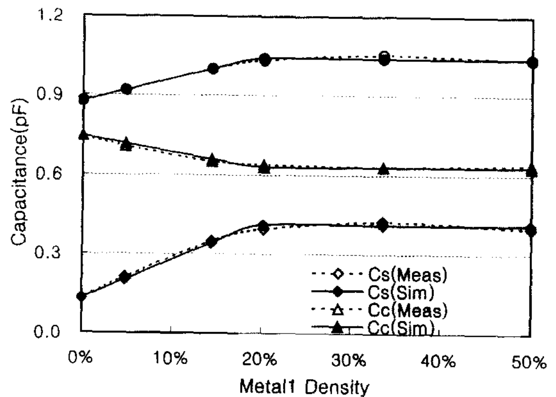


그림 10. 커패시턴스 대 금속 1 밀도. 시뮬레이티드 결과는 TCAD 툴에 의해 가지고 얻어진다.

Fig. 10. Capacitance vs. metal 1 density. The simulated resulted are obtained with TCAD tool.

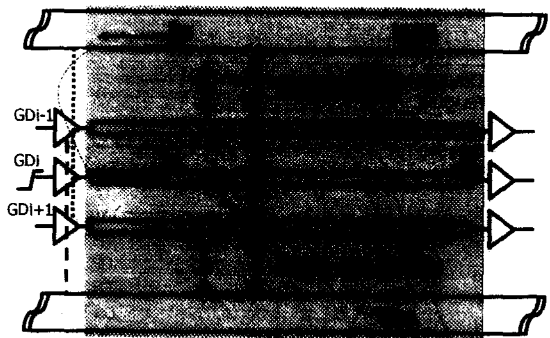


그림 11. 글로벌 데이터 라인을 위한 검증 구조, Gdi, i=1,...,n. Vdd 와 Vss 선들은 전류 회귀 패스로 동작한다고 가정하였다. Dp(i) 와 Dg(i)는 각각 i-th 신호선과 power Vdd 선 혹은 ground Vss 선 까지의 거리이다. Pm 은 글로벌 선의 금속 피치이다.

Fig. 11. The evaluated structures for global data lines, Gdi, i=1,...,n. We assume that the Vdd and Vss lines are current return-paths. Dp(i) and Dg(i) are distances from the i-th signal line to power Vdd line and ground Vss line, respectively. Pm is the metal pitch of global lines.

Figure 11 and 12 show the simulated structures of global lines and their results according to underlayer geometries and line models. We calculated the loop inductance (*Leff*) with self inductances (*L*) and mutual inductances (*M*) between signal line and ground line as a current return path. It can be expressed as follows:

$$Leff = L_s + L_g - 2M_{s-g}$$

where s/g in Ls, Lg and Ms-g denotes signal/ground(or power) lines.[5,6]

Figure 12 clearly shows the effects of models and underlayer geometries on signaling of global lines. On global data lines and clock lines having 5mm length and 800Mbps~1.06Gbps, the signal uncertainty by interconnect model and underlayer geometry can make the 10~15% skews in process of data transportation. From the simulated results, it is found that the skews between different paths having the same line lengths can be reduced through considering the proper RLC model and the underlayer lines density. As a result, we can avoid the maximized skews.

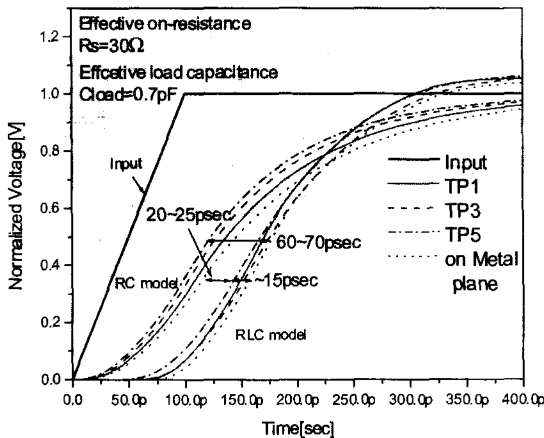


그림 12. 그림 11에서 보여준 데이터 라인의 시뮬레이션 결과. 글로벌 데이터 선들은 TP1, TP3, 과 TP5에 기초하여 시뮬레이션되었다. 모든 길이는 5mm 이다

Fig. 12. Simulated results of data lines as shown in Fig.11. The global data lines are simulated based on line parameters of TP1, TP3, and TP5. All length is 5mm.

Ⅵ. Conclusion

The transmission line characteristics are evaluated for achieving the accurate signal properties on global lines of DRAM chips. We proved that the underlayer geometries, which are difficult to test with conventional SPICE simulation, deteriorate the signal integrity as signal slew and flight delay. In order to demonstrate these underlayer effects, the test patterns were designed and fabricated with a DSM DRAM CMOS technology. The time-domain signal transient test and S-parameter measurement were performed on the patterns. Through this work, it is shown that the time-domain signal transient responses on real chips can be accurately characterized with the underlayer geometries and frequency-variant RLC characteristics into account. Consequently, designers should consider the additional time margins according to loop inductance and underlayer uncertainty in real global line geometries.

References

[1] Myunghee Sung, et al "An Efficient Crosstalk Parameter Extraction of Embedded Microstrip Structures on High-Speed MCM," Proc 49th Electronic Components and Technology Conf, San Diego, California, pp. 475~479, 1999.

[2] Bendik Kleveland, and et al, "Line Inductance Extraction and Modeling in a Real Chip With Power Grid," IEDM 99, pp. 901~904.

[3] Y. Eo and W. R. Eisenstadt, "High-speed VLSI Interconnect Modeling based on S-Parameter Measurements," IEEE Trans. Comp., Packag., Manufact. Technol. B, Vol. 16, pp. 215~225, Mar. 1995.

[4] Y. Eo, and et al, "S-Parameter-Measurement-Based High-Speed Signal Transient Characterization of VLSI Interconnects on SiO_2-Si Substrate," IEEE Trans. Comp., Packag.,

Manufact. Technol.. Vol. 23, pp. 470~479, AUGUS. 2000.

[5] J.-K Wee, and et al, "Modeling the Substrate Effect in Interconnect line Characteristics of High-speed VLSI Circuits," IEEE Trans. Microwave Theory &Tech., Vol. 46, No. 4, pp. 1436~1443, Oct. 1998.

[6] F. W. Grove, Inductance Calculation Working Formulas and Tables, New York, Dover, 1962.

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