Virtual ground monitoring for high fault coverage of linear analog circuits

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Abstract— **This paper explains a technique to improve the fault coverage of oscillation-test [1-5] for linear analog circuits. The transient behavior of the virtual ground is monitored during oscillation to extract information of the circuit. The limitation of the oscillation-test is analyzed, and an efficient signature analysis technique is proposed to maximize the fault coverage. The experimental result proves that the parametric fault coverage can be significantly increased by the proposed technique.**

Index Terms — **analog circuits, mixed-signal circuits, built-in self test (BIST), oscillation-test, signature analysis.**

I. INTRODUCTION

The oscillation-test methodology (OTM) [1-5] has been proposed as a vectorless scheme for manufacturing test, both as a general defect-oriented technique, as well as oscillation built-in self-test (OBIST) scheme. The basic idea is to convert a circuit-under-test (CUT) into a circuit that oscillates. Faults in the CUT which cause the oscillation frequency to deviate from its nominal value by greater than a given tolerance band can be detected. Using this technique, no application of test vectors is required during manufacturing test. This vectorless testing concept is appealing since the generation of on-chip pure sinusoidal stimulus requires significant hardware overhead. Therefore, oscillation test seems a promising solution for the test stimulus problem.

However, there is a limitation on using the OTM for parametric fault coverage since the oscillation frequency alone cannot generate sufficient information to identify many faults. Research [3] shows that the oscillation frequency cannot achieve sufficient high fault and yield coverage, and it proposes to measure the amplitude of the oscillation as well as the oscillation frequency. In [3], the oscillation amplitude was measured only at the primary output of the CUT, and an on-chip amplitude measurement technique was not developed. The oscillation amplitude at the primary output of the circuit could be sensitive only to the faulty components adjacent to it. The oscillation amplitude may not be sensitive to the faulty components that are not adjacent to the primary output. In order to achieve high parametric fault coverage, there should be an efficient technique to monitor the internal nodes as well as the primary output.

In our experiments in section III, it will be shown that the monitoring of internal nodes can significantly increase the fault coverage with minimum hardware overhead.

Significant testing time could be another drawback of oscillation test methodology since the accurate calculation of oscillation frequency requires a long measurement time. The testing time of oscillation-based test would be on the order of seconds if we do not apply efficient signature analysis technique. Direct measurement of oscillation frequency could take a second or more. Also, it has been found that each different oscillator structure is more sensitive to a set of components, and it has been suggested that more than one from the CUT should be constructed in order to increase the fault coverage [2,3]. This will even further increase testing time. If a large circuit

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is partitioned into several small circuits that oscillate, the total testing time using oscillation-based test could be more than several seconds, which is prohibitively long for go/no-go tests in production

In this paper, the application of the time-division multiplexing (TDM) comparator scheme [6] for the parametric fault coverage of OTM is extensively researched. We show how the fault coverage can be significantly increased while requiring less test time. The main focus of this paper is to analyze the behavior of the CUT in oscillation-test mode, and show how our technique can be used to extract maximum information to improve the fault coverage. We prove that the internal nodes of CUT need to be monitored for higher parametric fault coverage. Especially, the virtual ground of analog circuits can be useful to detect fault indirectly.

II. Review of TDM Comparator BIST Scheme

This section reviews the BIST technique using the TDM comparator and counters [6]. The basic concept of this scheme can be easily explained for linear systems. For example, the output response of a linear system will be sinusoidal for a sinusoidal test input and only the amplitude and phase will be changed by the linear system. If there is a fault in the system, then the amplitude will be faulty and the comparison with the reference voltage will generate a different sequence of ones and zeros. If we assume that the amplitude is reduced by faults, then the number of ones will decrease and the accumulated value in the counter will also decrease.

Figure 1 shows the proposed BIST scheme using the TDM comparator. The output response of a CUT will be compared with the reference voltage 1 and 2, and the comparison results will be accumulated into each counter according to the clocks, $\Phi 1$ and $\Phi 2$, (time-division multiplexing). Each counter will have unique value as a signature for the CUT. Reference voltages can be decided during the BIST design phase allowing a designer more flexibility to analyze the output. Several comparator circuits are available and most of them can be used to implement the proposed BIST scheme.

As a simple implementation of this BIST scheme, only the primary output of the CUT may be compared

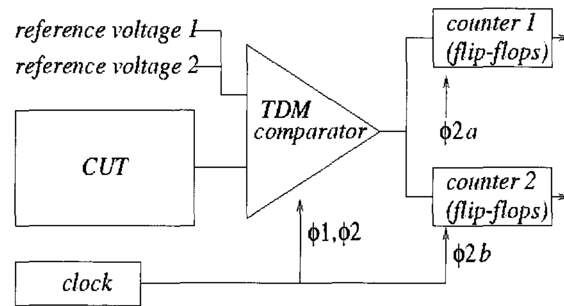

Fig. 1. TDM BIST Scheme.

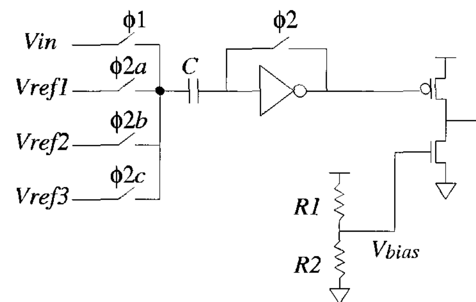

Fig. 2. Time-Division Multiplexing Comparator.

with reference voltages. However, testability of the circuit can be enhanced by observing internal nodes as well as the primary output. The TDM comparator can be used to observe internal nodes by simple modification. In figure 2, only the $\Phi 2$ clock was divided into 3 time slots and multiplexed to select the reference voltages, and the output response *Vin* was connected only from the primary output of the CUT. The $\Phi 1$ can be also divided into 3 time slots and multiplexed to select internal nodes of the CUT. Only two more switches are required to modify the TDM comparator in figure 2. The internal signal from each internal node is compared with its respective reference voltage and is accumulated into its respective counter to generate a signature. The selection of internal nodes is achieved through the following steps.

- Indirectly measure the oscillation frequency using a TDM counter. Most catastrophic faults and many parametric faults can be detected with this indirect frequency measurement.
- Find the undetected parametric faulty components.
- Monitor internal nodes near the undetected faulty components.

III. Observation of the Oscillation Behavior

In this section, an interesting circuit behavior during the oscillation will be investigated, which will give essential information to increase the parametric fault coverage. Figure 3 shows an analog integrator, which is a basic analog building block and also a part of our benchmark circuit for experiments. Equation 1 shows the well-known integrator equation from figure 3. Because of the high gain of the opamp, the negative input, Vx, can be treated as a virtual ground. In the ideal case, the integrator output follows equation 1 if a circuit design is done to limit the signal swing so that the deviation from the ideal equation is minimized.

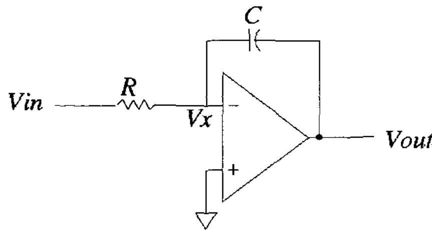

Fig. 3. Integrator.

$$V_{out}(t) - V_x(t) = \frac{1}{RC} \times \int [V_{in}(t) - V_x(t)]dt \quad (1)$$

The practical opamp will always have the maximum output swing, which is decided by the power supply rails and the architecture of the opamp's output stage. During oscillation, the signal swing can be out of the operation range, and the signal will be clipped by the opamp maximum output swing. If a clipping of the signal happens, the voltage input to the virtual ground will deviate from the ideal small-signal behavior. In other words, the negative input of the opamp fails to be a virtual ground showing large-signal behavior, which is called as a *virtual ground explosion* in this paper. This phenomenon is always observed from circuit simulation of CUT in oscillation-test mode.

$$A_f(s) = \frac{A(s)}{1 - A(s)\beta(s)} \quad (2)$$

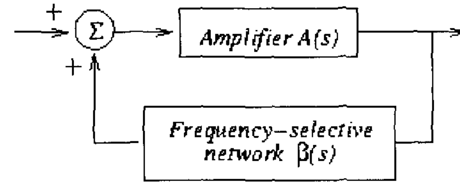

Fig. 4. Feedback loop for oscillation.

In order to rigorously understand why the virtual ground explosion occurs, it will be better to review the oscillation theory. The usual practice to explain the circuit oscillation is to use the location of poles in the s-domain [8]. In figure 4, when the circuit $A(s)$ is located in the closed feedback loop, the transfer function of the feedback system is like equation 2. The loop gain is defined as $A(s)\beta(s)$, and the denominator of equation 2 becomes the characteristic equation. It is apparent that the feedback loop changes the location of the poles in the system, and the characteristic equation determines their locations. The stability test can be done by assuming a pair of poles at $s=\sigma_0 \pm j\omega_n$ from the characteristic equation. The location of poles determines the time-domain signal as in equation 3. It can be easily seen that if σ_0 is a positive value, which means that poles are in the right-half plane, the time-domain signal will be a growing sinusoid.

$$v(t) = e^{\sigma_0 t}[e^{+j\omega_n t} + e^{-j\omega_n t}] = 2e^{\sigma_0 t}\cos(\omega_n t) \quad (3)$$

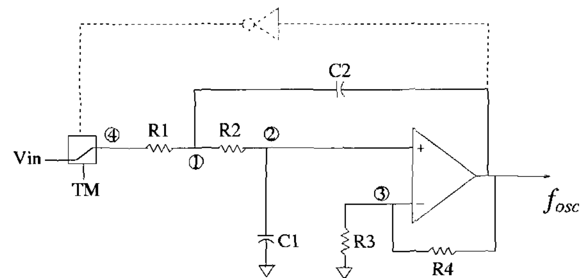

Fig. 5. Sallen-Key filter. (R1=R2=3.2kΩ, R3= 4.86kΩ, R4=8.84kΩ, C1=C2=50nF)

Zarnik et al. have proposed a technique [5] on how to convert active RC circuits to oscillators. They have analyzed several analog filters to move the poles on the $j\omega$ axis by increasing or decreasing passive component

values. Basically, their technique is to increase the quality factor, Q, of the circuit to infinity. One of the examples in their paper was the Sallen-Key low-pass filter, which is also shown in figure 5, whose component values are from [2]. The system transfer function of the Sallen-Key filter can be expressed as in equation 4 where $K = (R_3 + R_4)/R_3$.

$$\frac{V_{out}}{V_{in}} = \frac{\frac{K}{R_1 R_2 C_1 C_2}}{s^2 + s\left(\frac{1}{R_2 C_1} + \frac{1}{R_1 C_2} + \frac{1}{R_2 C_2} - \frac{K}{R_2 C_1}\right) + \frac{1}{R_1 R_2 C_1 C_2}} \quad (4)$$

$$K = \frac{R_1 C_1 + R_1 C_2 + R_2 C_1}{R_1 C_2} \quad (5)$$

In order to move Q to infinity, the filter gain K has to be tuned to a specific value as shown in equation 5. In this condition, a pair of poles will move on $j\omega$ axis, and the filter will oscillate as in equation 6. The time-domain oscillation signal in equation 6 was calculated by the Inverse Laplace transform from the system transfer function, and it clearly shows a limitation in Zarnik's scheme. From equation 6, the oscillation frequency and the amplitude can be found as in equation 7 and 8, respectively.

$$V_{osc}(t) = \frac{K}{\sqrt{R_1 R_2 C_1 C_2}} \sin\left(\sqrt{\frac{1}{R_1 R_2 C_1 C_2}}\, t\right) \quad (6)$$

$$f_{osc}(t) = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}} \quad (7)$$

$$Amplitude_{osc} = \frac{K}{\sqrt{R_1 R_2 C_1 C_2}} = \frac{R_1 C_1 + R_1 C_2 + R_2 C_1}{R_1 C_2 \sqrt{R_1 R_2 C_1 C_2}} \quad (8)$$

For example, in the case of the Sallen-Key filter in figure 5, the oscillation frequency will be 994.7 Hz, if the poles are moved on $j\omega$ axis by applying Zarnik's technique. The problem is, however, the amplitude of the oscillation will be extraordinarily high according to equation 8. For the Sallen-Key filter, Zarnik's technique will generate an oscillation amplitude of 18750V, which is not possible in general analog integrated circuits. In a real circuit, of course, the oscillation signal will be saturated at the power supply rails instead of growing up to 18750V.

When the oscillation is saturated at the supply rails, the input transistor pair of the opamp cannot operate in the normal operating range and it will fail as an opamp. The key point is that the saturation is very likely to happen in most cases, and the virtual ground explosion will occur as the signal swing is saturated. Even more important point in oscillator design is that moving the poles on $j\omega$ axis is not a reliable technique. It is almost impossible to have a perfect match in equation 5. Very small variation of the resistors or capacitors will move the poles into the left-hand plane (LHP) or into the right-hand plane (RHP). Since it is not a digital filter, the analog circuit components will have specification margins. Even a very small variation in a component, which may be in the margin, will cause the oscillator to exponentially decrease to zero, or exponentially increase and saturate by the power supply rails. In other words, it is not possible to allow a tolerance of analog circuits.

Because of this, the general oscillator design technique is to move the poles into the RHP, and use a limiter or an automatic gain control (AGC) circuit to control the maximum amplitude [8]. Since the poles are in the RHP, the oscillation amplitude increases, but eventually power supply rails limit the maximum amplitude. It can be explained as the poles begin in the RHP and eventually move to the imaginary axis to stop the growth. It is well explained in [7] that the oscillation frequency in the small signal analysis is usually a higher value than the real oscillation frequency since the large-signal behavior such as the nonlinear current drive and capacitance of each node determines the oscillation frequency.

Most of the previous oscillation test papers have used the technique to move the poles into the RHP, and let the power supply rails operate as a limiter. In these cases, if we simply try to measure the amplitude at the primary output, the parametric faults cannot change the maximum amplitude, which is already the power supply rail, and cannot be detected. The saturation is a usual phenomenon in oscillator design, and the direct measurement of the oscillation amplitude is not possible in most cases. In most oscillation test, the feedback circuit such as an inverter is used to minimize the hardware overhead such as an AGC circuit, or the direct feedback connection is used [1-4]. Therefore, the virtual

Table 1. Tolerance bands.

	osc. frequency (Hz)	Osc_counter	node1	node2
Nominal	419	2385	216	624
Tolerance	398-438	2281-2514	193-228	556-704

ground explosion is almost certain to happen in oscillation test. Also, if the maximum amplitude of the oscillation is controlled to be below the power supply rail so that no clipping of the oscillation signal happens, it will be even better to apply our TDM comparator, and the amplitude measurement will be easier. However, maximum amplitude control is not a practical technique as was proven with the Sallen-Key filter above.

Since the virtual ground explosion happens in most cases of the OTM, our method can have extra information from it to increase the fault coverage. Without the internal node monitoring to observe the virtual ground explosion, we figured out that it is extremely difficult to measure the amplitude even if we assume a dedicated high-resolution analog-to-digital converter (ADC) for the amplitude measurement. If we only measure the oscillation output at the primary output without internal node monitoring, the parametric fault coverage will be limited, since the amplitude of the primary output of the circuit is already clipped to the power supply rails. Thus, maximizing the fault coverage for parametric faults will not be easy without monitoring the internal nodes and observing the virtual ground explosion.

IV. EXPERIMENTAL RESULTS

The state variable filter in figure 6 is used to demonstrate how the fault coverage can be significantly increased by applying our monitoring technique. The state variable filter is converted to an oscillator by controlling test mode (TM) switch. The bandpass output (BPO) signal has nominal oscillation frequency of 419Hz, and its amplitude is clipped by the power supply rails as explained in previous section. The virtual ground node is monitored to improve the fault coverage, and the TDM comparator output is shown in table 1. The *osc_counter* is the monitored value of the primary output, and node1 and node2, which are represented as circled numbers in figure 6, are the virtual grounds of the state variable filter.

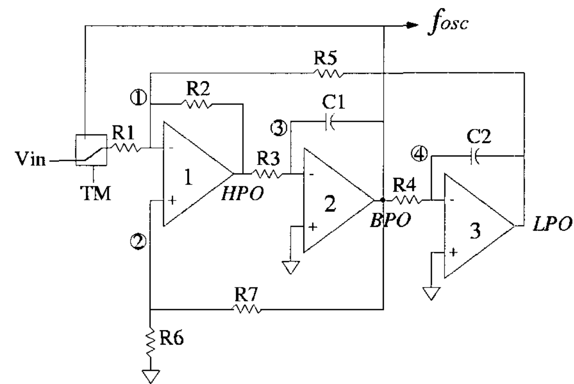

Fig. 6. Testable state variable filter. (R1=R2=R3=R4=R5 =10kΩ, R6=1kΩ, R7=12kΩ, C1=C2=20nF)

The frequency of clocks *Φ1* and *Φ2* is 3MHz and the measurement is done for only one oscillation cycle of the CUT, which takes 2.4ms. However, the required test time for the conventional direct measurement of the oscillation frequency needs to be much longer. We assumed a frequency measurement time of 1.0s for the conventional scheme since we need sufficient time to detect the small deviation of frequencies. Thus, our approach makes a significant difference in test time, which will result in significant reduction of manufacturing test cost.

The tolerance band is shown in table 1 to represent the allowable component variations of the analog circuit. For these experiments, we use a single-component fault, in which we assume that a single perturbed component causes the output to go beyond its tolerance value. The allowable component deviations are assumed to be ±5% around the nominal value of each component. Parametric faults were injected assuming ±20% variation of each circuit component. Experimental results in table 2 show the signatures for the injected faults. The first column

Table 2. Parametric fault coverage for ±20% variation. (* denotes undetected faults.)

	faulty value	osc. freq.	Osc_counter	node1	node2
R1	12kΩ	250	3997	263	1859
	8kΩ	477	2092	160	461
R2	8kΩ	* 406	2458	**0**	575
	12kΩ	* 428	2333	**265**	656
R3	8kΩ	457	2186	223	599
	12kΩ	389	2566	178	639
R4	8kΩ	463	2157	156	528
	12kΩ	385	2594	246	710
R5	8kΩ	491	2033	274	468
	12kΩ	330	3027	168	967
R6	0.8kΩ	* 400	2496	214	**0**
	1.2kΩ	* 435	2294	218	**724**
R7	9.6kΩ	441	2266	212	725
	14.4kΩ	* 402	2486	217	**0**
C1	16nF	466	2143	198	605
	24nF	384	2600	208	623
C2	16nF	471	2199	161	496
	24nF	381	2622	242	731

shows the component in the circuit, and the second column shows the faulty values. The third column is the traditional direct oscillation frequency measurement from experiments. The fourth column is the *osc_counter* value to estimate the frequency indirectly. The internal nodes are also monitored to improve the fault coverage. The traditional oscillation-test has limitation in detecting five faults in this case, and the proposed technique successfully detected all of them. The bold-faced numbers in fourth column show the detected signature values that go out of the tolerance band, which means that the faults are successfully detected.

Unlike the stuck-at faults in digital domain, the small parametric variation in analog circuit is extremely difficult to detect. In our experiments, all catastrophic faults were detected as expected, and also we achieved 100% fault coverage for the ±20% variation of components. Table 3 summarizes the maximum variation that our technique can detect. Compared to the traditional oscillation frequency measurement, the proposed scheme shows significant improvement in fault detectability. Especially, traditional scheme cannot detect large variations in R_2, R_6 and R_7, while our scheme has improved the testability of these components. Further increase of fault coverage is possible by more internal node monitoring in our scheme, while the traditional techniques requires to partition the CUT into several smaller circuits to enhance testability. It is easy to understand that our proposed virtual ground monitoring scheme is more efficient than the circuit partitioning since the circuit partitioning requires more hardware overhead and test time. The hardware overhead of this scheme for internal node monitoring would only be the two extra switches for the TDM comparator in the analog block. An extra counter would be the hardware overhead in the digital block.

Table 3. Fault Coverage for the state variable filter.

	traditional.	proposed.
R1	-5% ~ +5%	-5% ~ +5%
R2	-31% ~ +52%	-5% ~ +5%
R3	-11% ~ +14%	-11%~ +14%
R4	-9% ~ +12%	-9% ~ +8%
R5	-5% ~ +6%	-5% ~ +6%
R6	-22% ~ +24%	-5% ~ +13%
R7	-18% ~ +23%	-13% ~ +5%
C1	-9% ~ +11%	-9% ~ +11%
C2	-8% ~ +10%	-8% ~ +10%

V. CONCLUSION

In this paper, we have demonstrated how to efficiently increase the parametric fault coverage of the oscillation test. By monitoring the virtual grounds of analog circuits, we can have sufficient information to detect most of the parametric faults. The TDM comparator scheme measures the oscillation frequency as well as the oscillation amplitude. In general, the maximum output signal swing of the opamp will limit the oscillation amplitude, which makes the amplitude measurement a difficult problem. We have showed that this problem can be solved by measuring the internal nodes during the virtual ground explosion state. For the state variable filter in our experiments, we have demonstrated that the parametric fault coverage for ±20% faults can be increased up to 100% with significantly less test time.

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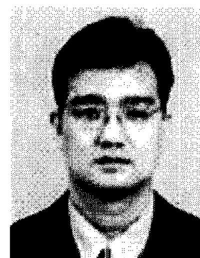

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