Technology of MRAM (Magneto-resistive Random Access Memory) Using MTJ(Magnetic Tunnel Junction) Cell

Wanjun Park, I-Hun Song, Sangjin Park , and Teawan Kim

Abstract - **DRAM, SRAM, and FLASH memory are three major memory devices currently used in most electronic applications. But, they have very distinct attributes, therefore, each memory could be used only for limited applications. MRAM (Magneto-resistive Random Access Memory) is a promising candidate for a universal memory that meets all application needs with non-volatile, fast operational speed, and low power consumption. The simplest architecture of MRAM cell is a series of MTJ (Magnetic Tunnel Junction) as a data storage part and MOS transistor as a data selection part. To be a commercially competitive memory device, scalability is an important factor as well. This paper is testing the actual electrical parameters and the scaling factors to limit MRAM technology in the semiconductor based memory device by an actual integration of MRAM core cell. Electrical tuning of MOS/MTJ, and control of resistance are important factors for data sensing, and control of magnetic switching for data writing..**

Index Terms — **MRAM(Magneto-resistive Random Access Memory), GMR(Giant Magneto-resistance), MTJ(Magnetic Tunnel Junction).**

I. Introduction

Semiconductor memory devices those are currently used in most electronic applications have very distinct attributes, therefore, each memory could be used only for limited applications. For example, DRAM is a high-speed and high-density memory, but has disadvantages of high power and volatility. FLASH memory is a non-volatile memory with low power, but has disadvantages of bad endurability and low speed. SRAM is high speed and low power memory, but has relatively low density. To implement all the advantages into a universal memory device, there have been trying new types of memory technologies such as FeRAM, MRAM, and OUM.

FeRAM is ahead of other technologies with well-defined architecture and integration technique. MRAM and OUM are in the early development stage. The advantage of those two technologies is scalability. For MRAM, actually, magnetic materials have been well proven by long time using and can be controlled magnetic properties as small as super-paramagnetic limit, several tens of nano-meter size. It is implicit that MRAM technology doesn't be limited by material itself.

II. GMR Technology

The introduction of giant magneto-resistance(GMR) that was discovered in magnetic/non-magnetic multilayer in 1988 [1], has been a major impetus to attribute magneto-resistive random access memory (MRAM), new technology of memory device. Once having the GMR technologies, two magnetization states, magnetization parallel and anti-parallel, are controllable and the resistance difference between two states reaches within a comparable range of commonly using semiconductor memory technology. The major impact of MRAM is its long storage lifetime by non-volatility, low cost and lack of any wear-out mechanism.

Manuscript received August 19, 2002; revised September 24, 2002.
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Honeywell Corporation has successfully demonstrated MRAM with the memory elements of core cell of a current-in-plane (CIP) spin valve structure that is not effective for high MR value, density capability, and operating speed [2].

To overcome those discrepancies, a different approach has been introduced to MRAM by exploiting another manifestation of spin-polarized transport. This approach is using spin dependent tunneling technology through an oxide barrier between two ferromagnetic thin films where the magnetization controls by exchange biasing due to introduce an anti-ferromagnetic layer. The magnetic tunnel junction (MTJ) quickly generates the memory elements of core cell with MOS transistor as a switch to select a data location.

The advantages of MTJ for MRAM core cell are high magneto-resistance(MR) and resistance compatibility with the semiconductor devices. With current-perpendicular-to-the plane(CPP) structure of MTJ, every electron passes through all the magnetic layers whose magnetization states are well controlled by the exchange-bias spin valve(EBSV). Employing of an oxide barrier allows MTJ to make series connection with MOS transistor without MR loss by the channel resistance of MOS transistor. Fortunately, very thin layer of AlO_x as a barrier material and its interfaces with ferromagnetic layers don't have lots of scattering centers of spin flip

Application of MTJ allows a simple core cell architecture that is very close to those of semiconductor memory. This architecture scheme opens a potential technology of universal memory by MRAM for both of stand alone and embedded memory application. IBM and *Motorola have recently demonstrated* MRAM technology with compatible performances and some reasonable density [3][4].

Successful demonstration by the previous work ensures that MRAM technology is a strong candidate of universal memory among the other new memory technologies with the comparison topics such as power consumption, speed, scalability, retention, endurance, and density. However there are still some fundamental issues to attain a real memory device.

In this paper, we simplify the cell structure to test fundamental limitation of MRAM technology as well as core cell performance. Now the selected issues will be listed and discussed in detail.

III. MRAM ARRAY ARCHITETURE

A basic array cell structure of MRAM is series connection of MOSFET and MTJ with two current flowing lines for generating external magnetic field (Fig. 1). One current line (digit line) is isolated from MTJ and the other line (bit line) shares a data sensing line of MTJ. For data writing, a cell is selected by a crossing point of the digit and bit line. The vector sum of magnetic fields generated from current flowing controls magnetization direction of free layer – parallel state and anti-parallel state. On the other hand, data reading needs a switch to select a desired cell of array. MRAM is a resistive device unlike the other memory devices using capacitor for data storage unit where data reading is eventually to sense about 20~30% of resistance difference between magnetization parallel and anti-parallel state of MTJ.

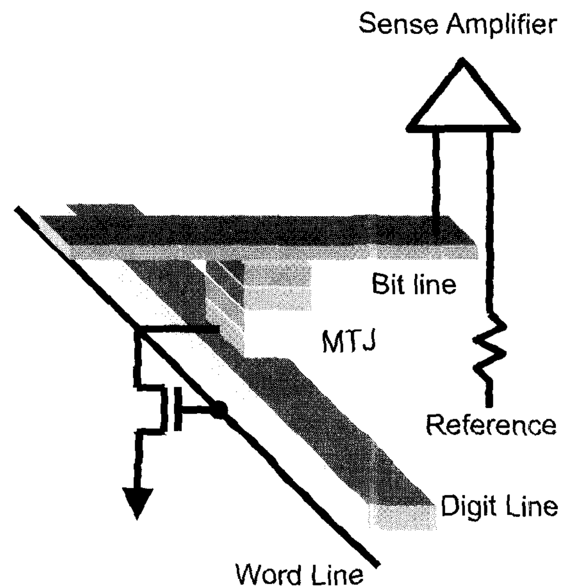


Fig. 1. A basic array cell structure of MRAM.

The most obvious solution for data sensing scheme may be using a reference cell where the stored cell information, either high resistance state (R_H) or low resistance state (R_L), is read by detecting the resistance difference between a MTJ cell and a reference cell. Resistance of this reference cell is simply given by $(R_H+R_L)/2$. At the beginning stage of MRAM

development, twin cell architecture was employed to minimize noise factors by using adjacent cell as a reference [3]. Another approach saved the cell area by sharing each column of cell array in a bank unit with a reference column [4].

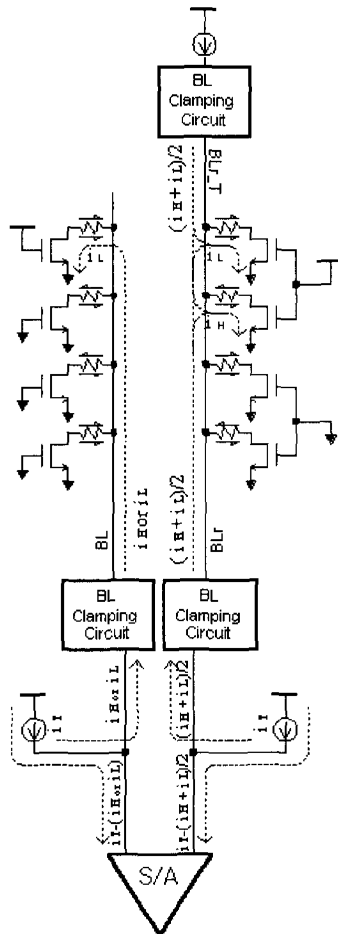
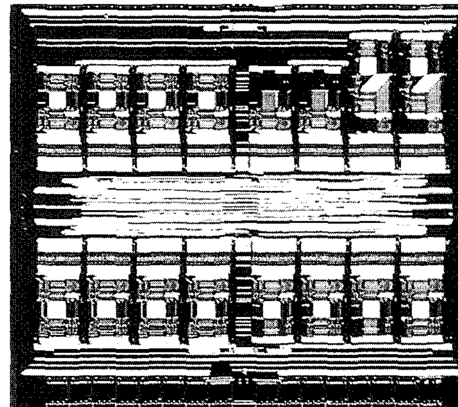


Fig. 2. Schematic of novel reference cell proposed in Ref. [5]

The MTJ resistance is very sensitive by little change of the barrier thickness with small process variation. This makes the above reference cell resistance to be larger than the medium value, resulting in incorrect sensing. New sensing scheme may be proposed as shown in Fig.2, the reference cell consists of a pair of memory cells connected in parallel and an additional bit-line clamping circuit to draw half of the current flowing into the reference cell [5]. The voltages at the bit line and the bit line bar nodes are clamped to 0.4V to maintain high MR ratio during sensing operation. A memory cell is selected by driving a W/L and selecting a column. Then, differential sense amplifier compares the cur-rents flowing into bit line and bit line bar nodes. The cell current flowing into sense amplifier is either i_H (R_H) or i_L (R_L) depending on the memory state. And the half of the reference cell current, $(i_H+i_L)/2$, flows into the sense amplifier and the other half flows into the additional clamping circuit. Thus, the reference current is generated so that the output of the reference cell current always remains at the midpoint between cell currents of high (i_H) and low (i_L) states. Fig. 3 shows the 64Kb MRAM test chip applying the new sensing scheme in BL clamping circuits.



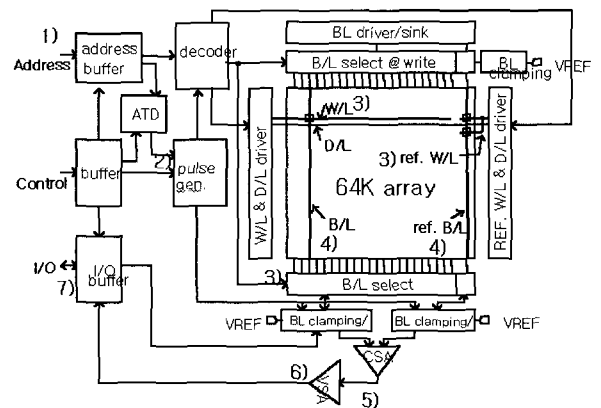
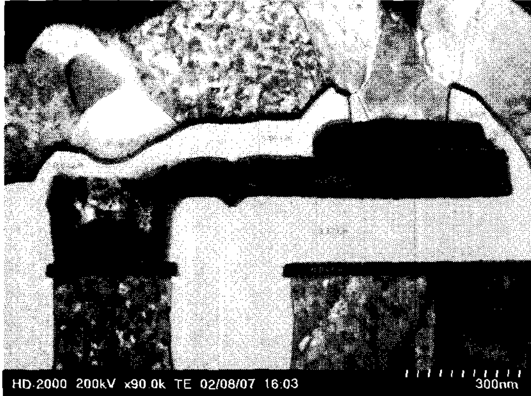


Fig. 3. 64Kb MRAM test chip image and block diagram (See reference [5] for more details).

VI. Electrical Properties of Core Cell for MRAM Array

MRAM core cell attributes to a hybrid technology of the CMOS and the MTJ process where the MTJ is connected to the MOS transistor in series. Fig. 4 shows

an example of the MTJ that is composed of two crossing lines – a digit line and a bit line, and a patterned multilayer stack composed of a Ru or Ta buffer, IrMn as an antiferromagnetic layer, CoFe as a pinned layer, plasma oxidized AlO_x as a tunnel barrier, Py(NiFe) as a free layer, and a capping layer.



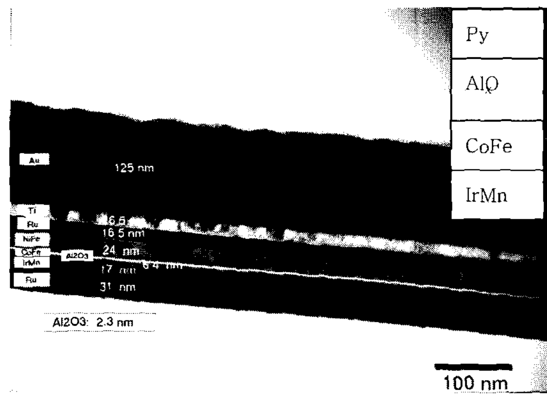


Fig. 4. TEM Images of MTJ with two writing lines and multilayer stack for MTJ.

The tested MTJs show 23~34% of MR, and 1K~2M $\Omega\mu m^2$ of AR (Area times Resistance). Since AR is a well-defined parameter by applying barrier thickness, a desired resistance value of the MTJ can be obtained from the choice of a certain barrier thickness. For example, AR is about $1K\Omega\mu m^2$ for the MTJ with 9Å of Al layer for a tunnel barrier that is a thickness limit to control MR without performance degradation in a usual Al sputtering and plasma oxidation process.

The NMOS transistors whose channel resistance is in the range between 200 to 2000Ω were chosen among many different sizes by consideration of the MTJ resistance. In general sense, less resistance of core cell is desired for operational speed of actual device. However, the MOS transistor itself has resistance and this resistance becomes a factor of MR drop. So the MTJ resistance should be chosen for significantly large value where the contribution of the MOS is negligible. The most of resistance attributes to the MTJ after the threshold voltage (0.8 V). The output current or resistance is separated by the applying magnetic field that generates magnetization parallel (for H_{ex} = 120 Oe) and antiparallel state (for H_{ex} = -120Oe). Fig. 5 shows that I_{gs}-V_{ds} characteristics of the MRAM core cell where the MOS resistance is not negligible for the core cell after the threshold voltage. The MOSFET size, W/L= 0.8μm/0.2μm, is more realistic for the actual core cell layout, however the narrow width induces higher channel resistance and encroaches MR on the core cell

Simple architecture for data reading is attributed to a key role for density consideration. The critical factors for this issue are high MR, uniform resistance over the entire core cell arrays, and appropriate resistance tuning between the MOS transistor and the MTJ.

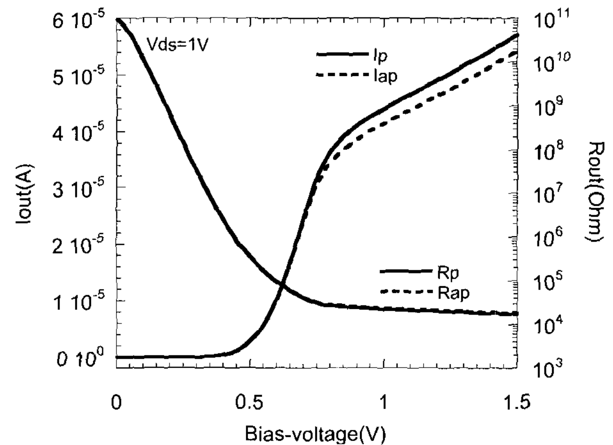


Fig. 5. I_{gs}-V_{ds} characteristics of the MRAM core cell where the MOS resistance is not negligible for the core cell after the threshold voltage.

Once MTJ structure and size are fixed by processing consideration, the dominant effects for maintaining high MR are MR bias dependence and appropriate choice of cell operation condition (below 0.6 volt for the tested cell here).

An estimation of direct margin for data sensing will be estimated by a difference in output current or resistance between parallel and antiparallel state. The I-V characteristics for the array cell are shown in Fig. 6 where the resistance difference decreases by larger bias

voltage. MR and resistance drop by bias dependence is inherent property of MTJ. The bias dependence on resistance is originated an inherent property by the barrier height difference of two interfaces. The bias dependence on MR attributes to the different decrease slop of resistance for magnetization parallel and anti-parallel state. This inherent property has not been explained clearly yet.

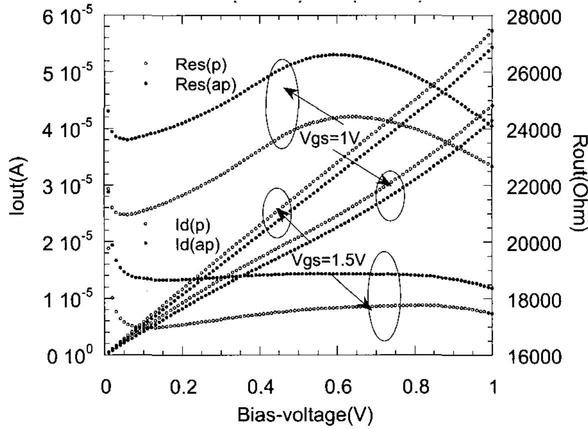


Fig. 6. I-V Characteristics of the MRAM core cell.

The most critical issue will be resistance control for each MTJ over the entire wafer. Either small variation of barrier thickness or area of the MTJ during patterning process makes margin narrower or even destroys resistance boundaries between magnetization parallel and anti-parallel state. We point out that issues of process capability are much more important than technology fundamental.

V. MRAM SCALING

The main issues for writing scheme are to find a method for low current operation. This operation requires reduction of switching field and high field generation by relatively small applying current. Unlike situation of data reading, size effect dominates for magnetization reversal. Hence switching is a major factor to limit device size. Fig. 7 shows switching field by the MTJ size where each switching field was measured along the exchange-bias pinning direction.

There may be two ways for low current data writing – one is to generate high magnetic field from the current lines and the other is to reduce the actual switching field by control of demagnetization effect. Fig. 8 shows a numerical estimation of magnetic field generated by line current with an assumption of uniform current density in the write line. If switching field is 50 Oe and digit line distance from MTJ is 1000 Å, current needs ~8 mA for normal write line. If we apply some special technique such as a field cladding layer (FCL) to write line, ~2 mA is enough for writing data.

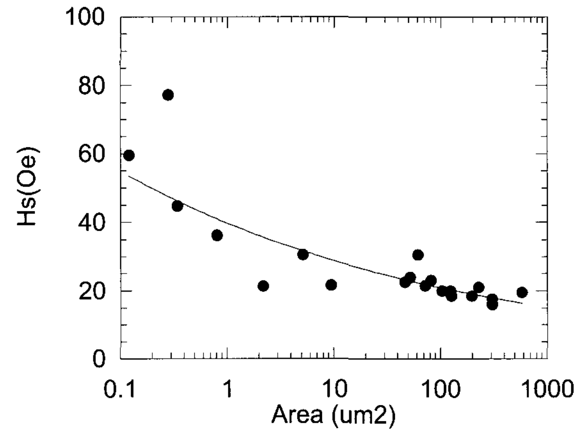


Fig. 7. Size effect for switching field (switching field measured along the exchange bias pinning direction).

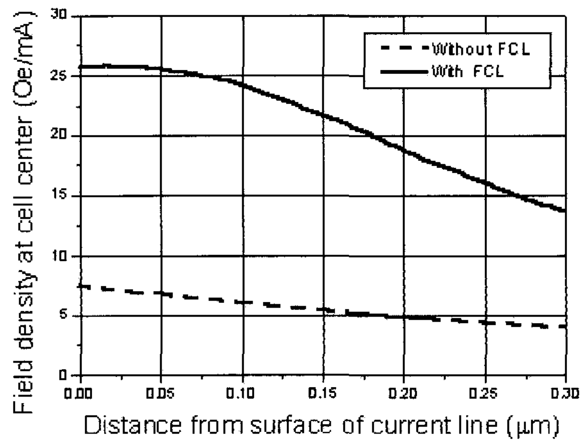


Fig. 8. Estimation of field generation by applying current (with assumption of uniform current density).

Actual operation of MRAM uses two directional writing fields to select a unit cell from two-dimensional core cell array (Fig. 9). One (H_1) is along the exchange bias pinning direction and the other (H_2) is perpendicular to the pinning direction. Use of two-directional field makes an advantage to reduce writing field since any

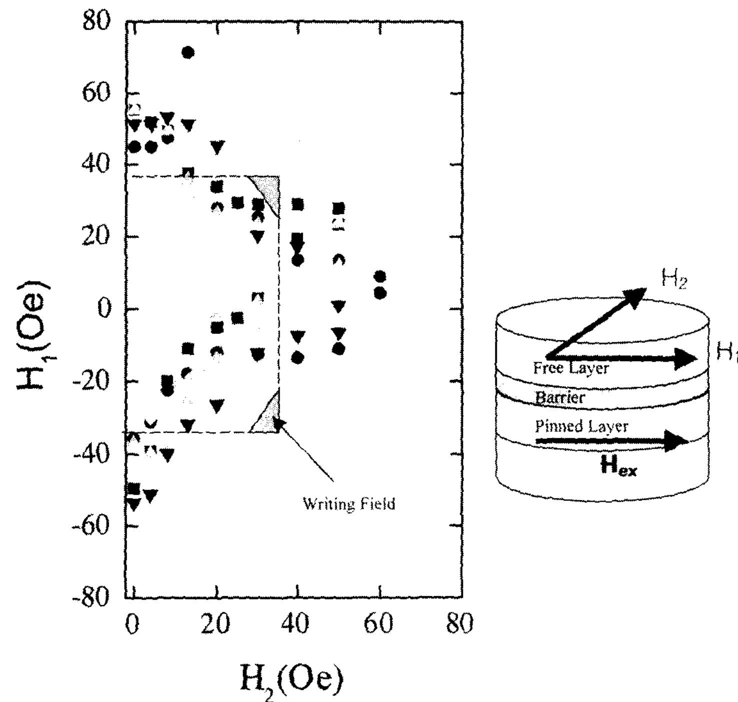


Fig. 9. Asteroid curve for the MTJ: area= 0.34 μm^2 and elliptical shape. (a write current is measured as H_1= 35 Oe, H_2= 30 Oe for example).

points outside asteroid curve can be a choice of writing condition. Another issue related to switching is cell selectivity that is originated from rather fundamental phenomenon such as vortex formation and edge pinning to prevent uniform alignment of magnetic moments. We easily find this type of distortion in MR curve for sub-micron size MTJ samples with strong size dependence. If there is a kink (local distortion of magnetic moment) in MR response curve, even single direction current will select an undesired cell and its magnetization of free layer can be switched statistically. It will result selection fail. Fig. 10 shows actual MR data of 0.35 μm^2 ellipsoidal MTJ cell with aspect ratio 2 that has the local moment distortion

The selection failure will be a critical point to determine scaling limit of MRAM technology. So further extensive study is necessary to figure out the origin of the local moment distortion. Micro-magnetic modeling based on LLG (Landau-Lifshits-Gilbert) equation indicate that the local moment distortion in an ellipsoidal cell shape mainly results from edge domain pinning rather than vortex formation, and reduces at larger aspect ratio [6]. Edge domain pinning can be controlled by a sharp cell boundary formation as well as by an appropriate choice of MTJ shape and aspect. Fig. 11 shows 0.1 μm^2 ellipsoidal MTJ cell with aspect ratio 3 that is free of the local moment distortion.

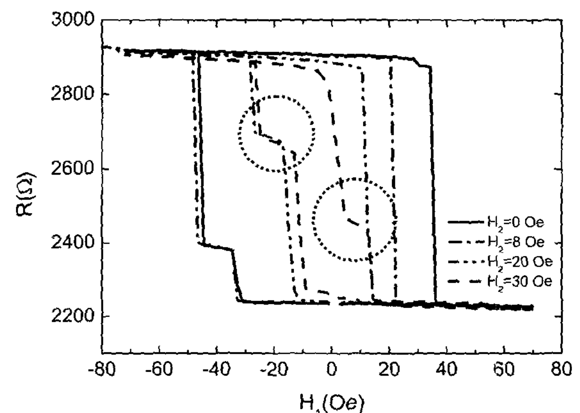


Fig. 10. MR curve of the MTJ samples with local magnetization distortion (size: 0.35 μm^2, shape: ellipse, aspect ratio: 2, the dotted circles indicate MR distortion by edge domain pinning).

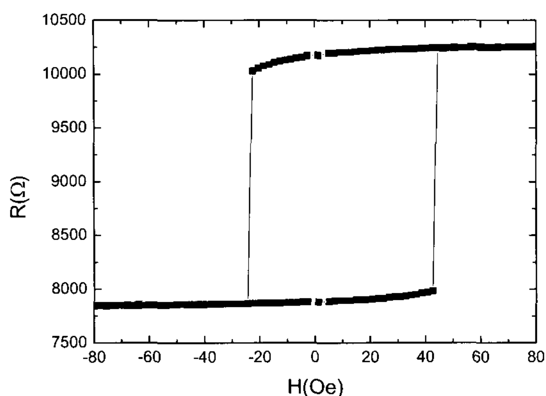


Fig. 11. MR curve of the MTJ samples without local magnetization distortion (size: 0.1 μm^2, shape: ellipse, aspect ratio: 3).

VII. CONCLUSION

The purpose of this study is to test the fundamental technology limit for an actual memory device. Research scope was restricted to only core cell at this stage. After success demonstration of integration process of MTJ and MOS transistor as a core cell unit, our facilities are ready to test the MRAM technology.

The key issues of MRAM technology as a future memory candidate are resistance control and low current operation for small enough device size. Resistance seems to be irrelevant to the size effect. MR is limited by the barrier thickness. Switching issues are controllable with a choice of appropriate shape and fine patterning process. Presenting data meet fundamental requirement to satisfy the condition for coding/decoding function down to 0.1 μm^2 MTJ size that is a corresponding size to ~G-bit density capability. Finally it should be pointed out that controls of fabrication is rather important to realize an actual memory device for MRAM technology.

ACKNOWLEDGEMENTS

This work was partially supported by the national program for Tera-level Nano Devices.

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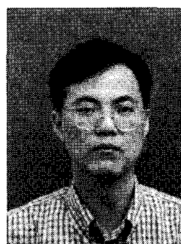

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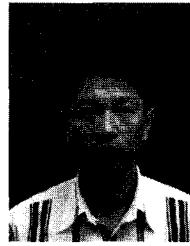

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