MRAM Technology for High Density Memory Application

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Abstract - **MRAM(magnetic random access memory) is a promising candidate for a universal memory with non-volatile, fast operation speed and low power consumption. The simplest architecture of MRAM cell is a combination of MTJ(magnetic tunnel junction) as a data storage part and MOS transistor as a data selection part. This article will review the general development status of MRAM and discuss the issues. The key issues of MRAM technology as a future memory candidate are resistance control and low current operation for small enough device size. Switching issues are controllable with a choice of appropriate shape and fine patterning process. The control of fabrication is rather important to realize an actual memory device for MRAM technology.**

Index Terms – **MRAM, MTJ, TMR, non-volatile memory**

I. INTRODUCTION

Recently, the introduction of MTJ(magnetic tunnel junction) with about 40% of MR (magnetoresistance) at room temperature has been a major impetus to attribute MRAM, new technology of memory device[1]. MRAM is a memory device using magnetic material in a broad sense, and it has a somewhat long history from ferrite core in 1970s to magnetic bubble technology. But, MRAM in a narrow sense includes magnetic memory devices using MR effects, which are AMR(anisotropic magnetoresistance), recent GMR(giant magnetoresistance) and TMR(tunneling magnetoresistance). AMR MRAM device started to be fabricated at the middlw of 1980s, and it has been used for military and space purposes.[1,2] MR device of AMR MRAM consists of triple layers of Py/TaN/Py, it yields about 2% of MR ratio. But, the MR ratio produced by the real device gives only 0.5%.[2] This low MR ratio is a big issue for high density device, and this makes the device slow. So, the price of the AMR MRAM is quite higher than other competing devices, and the application has been limited. GMR and TMR devices have much higher MR ratio, and promise huge enhancement of the density, speed, reliability and power consumption of solid-state memory.

GMR MRAM was the main stream for MRAM developments, Honey well and Motorola had led the progress based on the huge experience in AMR MRAM. GMR MRAM was in a better position in commercializing, as it is very similar to AMR MRAM technically. But, the MR ratio of MTJ, a TMR device developed in 1995 is much higher than that of GMR. In order to achieve reasonable memory array densities many GMR cells (of number N) have to be electrically connected in series which means that the actual signal available when reading one particular cell is ~MR/N. This signal is not sufficient to GMR MRAM competitive with conventional DRAM and SRAM. By contrast, the high MR signal from individual MTJ cells can be fully utilized in a MRAM

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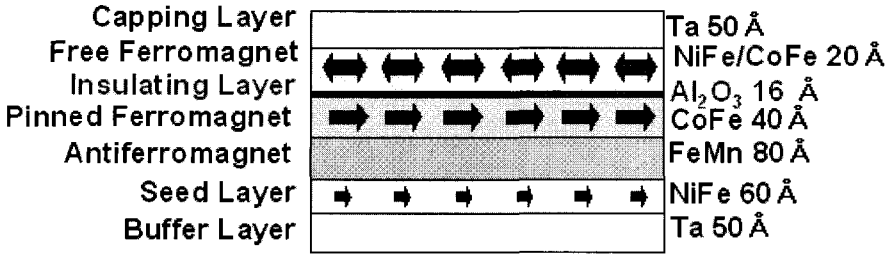


Fig. 1. Schematics of magnetic tunnel junction.

architecture, by connecting each MTJ element in series to a switch, for example, a CMOS transistor or a silicon diode. Consequently, TMR MRAM has been focused for the next generation nonvolatile memory candidate already. Motorola, the front runner of AMR MRAM and GMR MRAM turned to TMR MRAM rapidly, and most of major memory device vendors are reported to be developing TMR MRAM now. We report the review of the TMR MRAM technology briefly and summarize the TMR MRAM development status of major memory device suppliers with the result of hynix.

II. Review of Tmr Mram Technology

TMR MRAM has MTJ as a magnetoresistance device, MTJ has a stack as shown in Fig. 1. The basic MTJ comprises simply two ferromagnetic (FM) layers separated by a thin insulating tunnel barrier(Al-O ~10A). The conductance of such sandwiches varies as the cosine of the angle between the magnetic moments of the two FM layers[3] and is highest when the magnetic moments are parallel to each other. The relative orientation of the magnetic moments in the most basic MTJ structures is varied by utilizing FM layers with different magnetic coercivities. Note that in liothographically patterned basic MTJ elements the magnetic switching fields of the FM layers can be readily varied by changing their self-demagnetizing fields, for example, by varying their shape or net magnetic moment. Nevertheless, it is useful to magnetically pin or magnetically harden one of the FM layers in an MTJ by exchange bias with an antiferromagnetic (AF) layer[4]. In contrast to exchange biased GMR sandwiches[5] the AF layer must be metallic because of an important difference between GMR and MTJ memory elements: namely, whereas in GMR elements the flow of sense current is parallel to the layers, in MTJ elements the current flows perpendicular to the layers. The magnetoresistance of MTJ originates from the spin dependent tunneling effect of spin-polarized electron depending on the magnetic moment difference between the two FM layers. The first observation of a tunnel conductance that changes as a function of an applied magnetic field was reported by Julliere[6] in 1975. Slonczewski proposed a theory of this effect in 1989[3]. The main issue for MTJ preparation is to develop the pin hole free insulating Al-O layer. The maximum MR ratio was 2.7% by the early 1990s. The insulating alumina layer was prepared by natural or thermal oxidations. But, the high quality pin hole free alumina layer was not developed. Recently, the deposited Al has been oxidized by oxygen plasma, the resistance of the MTJ depends on the thickness of the deposited Al and the plasma oxidation condition dramatically(one order of magnitude of resistance per ~3Å). So, the main issue for the fabrication of MTJ is the precise control of the insulating alumina layer condition. The basic MTJ comprises simply two FM layers separated by a thin insulating tunnel barrier, but we should magnetically pin or magnetically harden on e of the FM layers in an MTJ by exchange bias with an AF layer as Fig. 1 if considering lithographically patterned memory applications. We should have the two different resistance conditions without external magnetic field for stable memory operations, this MTJ is much similar to GMR spin valve adopted to today's hard disk drive head. Furthermore, larger MR ratio is the another important issue for the high speed MRAM operations. Up to now, about 50% of the maximum MR has been achieved by NiFe or CoFe FM layers, more MR ratio with the junction by half metallic FM and the resonant junction

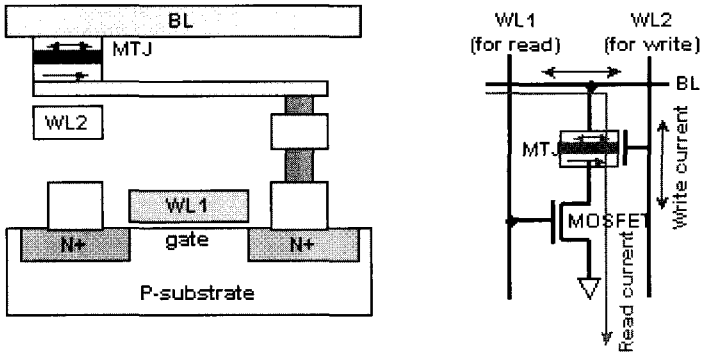


Fig. 2. MRAM cell with a MTJ and a transistor.

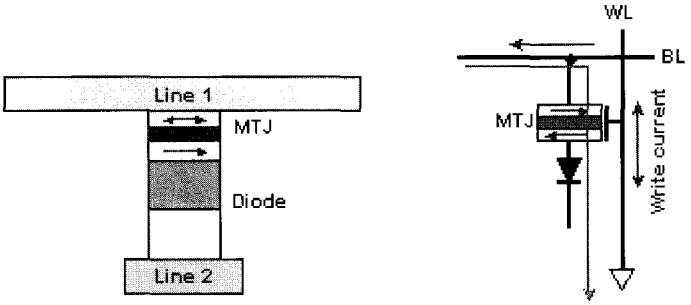


Fig. 3. MRAM cell with a MTJ and a diode.

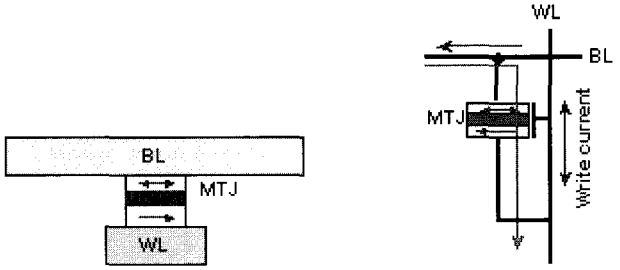


Fig. 4. MRAM cell with a MTJ only.

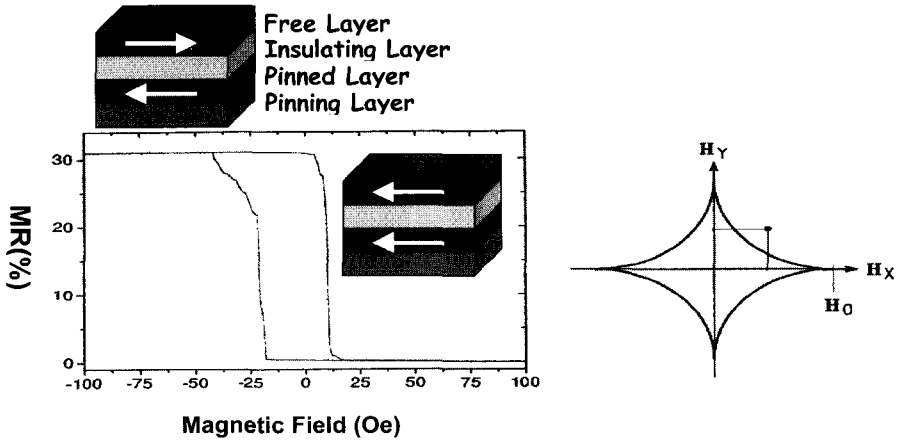


Fig. 5. The magnetic hysteresis curve(a) and the asteroid curve(b).

Table 1. Memory technology comparison.

	SRAM	DRAM	EEPROM	Flash	FeRAM	MRAM
Non-Volatile	x	x	√	√	√	√
Cell Structure Cell Size	6T 80-100F^2	1T1C 6-10F^2	2T ~40F^2	1T 4-12F^2	2T2C or 1T1C 8-12F^2	1T1J 4-12F^2
Read Endurance Write Endurance	∞ ∞	∞ ∞	∞ 10^5	∞ 10^5	10^{12}-10^{15} 10^{12}-10^{15}	∞ ∞
Write Voltage Write Energy	1.0-5V	1.8-5V	12-18V 1pJ	10-18V 10-200pJ	1.0-5V 1pJ	< 1.0-1.8V
Write Time Read Time	< 10ns < 5ns	<60ns <60ns	1-10ms 40-70ns	1us-1ms 30-70ns	20-60ns 20-60ns	< 20-60ns < 20-60ns
Standby current (uA) Read current (mA/op) Write current (mA/op) Voltage Power consumption	20 20 20 >0.5V < 1x	10000 80 80 >1V 1x	20 30 30 ? 1-1.5x	5 15 35 3.5V+12V(+/-6V) 1-1.5x	20 20 20 < 1.8V 0.5-1x	20 30 30 < 1.8V < 1x
Data write Data erase Access time Date retention	Overwrite Bit 6-70ns none	Overwrite Bit 5-70ns none	Erase+write Byte(64Byte Page) 40-70ns >10yrs	Erase+writ e Sector (8k-64k) 40-70ns >10yrs	Overwrite Bit <10-70ns >10yrs	Overwrite Bit <10-70ns none
Special transistor needs Mask count adder	No 0- standard	Yes (low leakage) 3-9	Yes (high voltage) 6-7	Yes (high voltage) 4-8	No 2-3	No 2-4
Maturity	Vol. prod.	Vol. prod.	Vol. prod.	Vol. prod.	Limited prod.	Test chip

by double barrier is being investigated. Heusler alloys of NiMnSb as Half metallic FM, PtMnSb, $La_{0.7}Sr_{0.4}MnO_3$ of Perovskite Mn oxides revealing Colossal MR, and CrO_2, Fe_3O_4 have been known for this application. Recently, several reports describe 200~300% MR ratio by using these materials. And also, MTJ using double barrier can produce ~100% MR ratio theoretically, slightly enhanced MR ratio has been achieved experimentally compared to that of MTJ with single barrier. But, MTJ using double barrier has a merit of mitigating the MR ratio dependence on the applied voltage at the operating voltage level of real device rather than the MR ratio itself enhancement. The MR ratio of MTJ is known to be degraded by the atomic interdiffusions between layers at over 300℃annealing. So, thermally stable MTJ stack design and each layer magnetic materials should be selected. In addition, low temperature back-end process after MTJ has been

Table 2. The front runners' status and target for MRAM.

Maker & Type	IBM & Infineon	Motorola	HP & Micron	NEC	Sony
	1T+1J & 1D+1J / 1J	1T+1J	1J	1J	1T+1J
Target Applications	Stand-alone & Mobile for multi-media	Embedded & Mobile	Mobile & Data storage	Mobile & Data storage	Stand-alone & Mobile for multi-media
Replacement Memory	Complete memory solution	SRAM & DRAM	Flash & HDD	Flash & HDD	Complete memory solution
Design Rule	0.25 completed @IBM in 2000(ISSCC) 0.13 for product (2004)	0.6 completed in 2000, (ISSCC) 0.18 for product (2004)	0.5 completed @ HP in 2000, 0.25 being pursued @Micron	0.1 in 2001 (IEDM)	0.35 in 2002 (Intermag)
Density	4Mb being pursued, target 128Mb (2004)	1Mb completed in 2001, target 32M (2004)	(?), >/=1Gb (mid-term target)	1Gb compatible in 2002	8kb completed in 2002, 128Mb compatible
Performance	Fast : Read 10-50ns, Write 10-40ns, 1.8V(Target) High Density : Read 50ns-1μs, Write 20-40ns, 1.8V	Read 35ns, Write 35ns, 2.7-3.3V	Read 100ns-1μs, Write 20-40ns, 1.8V	Write 50ns	?

investigated.

We may have three types of TMR MRAM cells generally, MRAM cell with a transistor or a diode and only MTJ.

Fig. 2 shows the MRAM cell with a CMOS transistor and a MTJ schematically. Front-end process makes the CMOS transistor and the MTJ for MRAM cell is fabricated in back-end process including metal lines. MRAM employs MTJ rather than a capacitor in current DRAM technology and it requires additional metal line WL2 for writing to make magnetic field. The other metal line is present B/L to make magnetic filed for writing.

Fig. 3 shows the MRAM cell with a diode and a MTJ schematically. This MRAM cell adopts a diode as cell switching device not a CMOS transistor. For writing, we can produce magnetic fields by the two conducting metal lines under and over the MTJ. For reading, the diode permits to flow the current thru MTJ by only one

direction, so the MRAM cell does not require a CMOS transistor as cell switching device.

Fig. 4 shows the MRAM cell with a MTJ only schematically. In this cell type, we should eliminate the disturbance between cells without a CMOS transistor or diode as cell switching device, then we would have additional circuitry for this purpose in peripheral Anyway, the two metal lines under and above the MTJ make magnetic fields for writing.

The magnetic polarization direction of the MTJ free layer in any MRAM cell types above can be adjusted by the magnetic field which is produced by currents thru two metal lines perpendicular to each other. The free layer of MTJ has its magnetic free axis which is defined at the deposition process, the magnetic switching occurs along this axis. Fig. 5(a) shows the magnetic hysteresis curve of a MTJ. If we define x-axis as magnetic easy axis, the variation of magnetic fields along two axes Hx and Hy makes the asteroid curve as shown at Fig. 5(b). The magnetic switching by x-axis magnetic field only requires much larger field of Ho. By writing operation above, TMR MRAM device defines the magnetic polarization direction of the free layer as parallel or anti-parallel to that of the pinned layer, the polarization direction would not flip without the applied magnetic field larger than the switching field. Even if the power is off for this memory device, the switching direction would not flip. So this memory device is non-volatile. The magnetic spin polarization direction can be sensed by detecting the current difference thru MTJ which has the magneto-resistance. This is the reading operation for TMR MRAM. So, we can read the data without any degradation. Table 1 shows the comparison of the commercialized memory technologies and TMR MRAM.

III. MRAM DEVELOPMENT STATUS

MRAM development has been focused on TMR MRAM up to now, most major Si device vendors are engaged. The companies now developing MRAM are Cyprus, Honeywell, HP, Hynix, IBM, Infineon, Micron, Motorola, Sony, NEC, Samsung, etc. The front runners' status and targets reported are shown in Table 2.

IV. MRAM TECHNOLOGIES FOR HIGHT DENSITY

A. *General Requirements*

If we make a MRAM memory cell with a transistor and a MTJ, we will see the schematics as shown in Fig. 6.

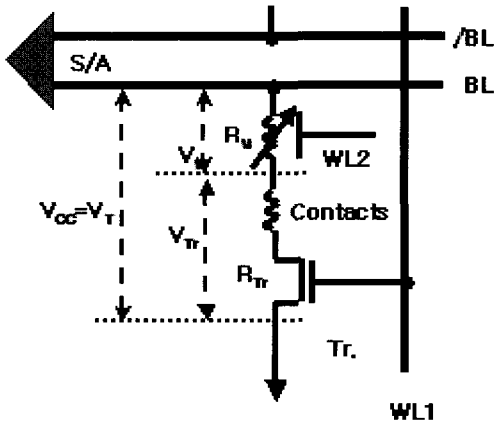


Fig. 6. Schematic MRAM cell with a transistor and a MTJ.

Then, expressions (1) and (2) are the two data saved on the memory, MRAM senses the difference as shown in formula (3).

$$I(data"1") = \frac{V_T}{R_{tr} + R_{MTJ}} \tag{1}$$

$$I(data"0") = \frac{V_T}{R_{tr} + (R_{MTJ} + MR \cdot R_{MTJ})} \tag{2}$$

$$\Delta | = I\ "1" | - I\ "0" \tag{3}$$

The required conditions to sense the difference of the two data are

$$\Delta\ I / I\ "1" > 0.1, \tag{4}$$

$$\Delta\ I > 10\ \mu A. \tag{5}$$

MRAM operation condition from the above requirements can be shown in Fig. 7, which gives

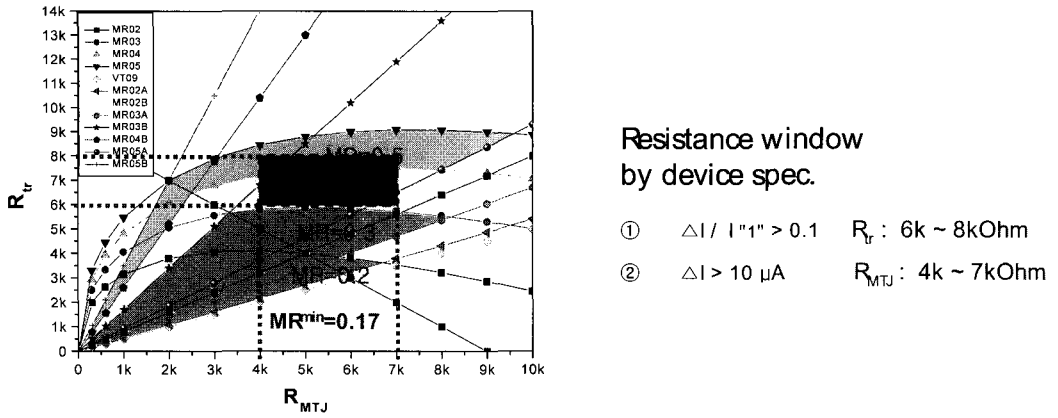


Fig. 7. Acceptable resistance ranges of cell transistor and MTJ with various MR.

acceptable resistance ranges of cell transistor and MTJ with various MR. Vcc is set to 0.9V. If we get over 40% of MR, MRAM cell transistor should have the resistance of 6k~8kΩ , and MTJ should have the resistance of 4k~7kΩ .

B. *Transistor Requirements*

The cell transistor of MRAM may use those of present DRAM and Logic processes. But, the resistance is up to tens of kΩ at the saturation region in the transistor I-V curve. To get 6k~8kΩ of resistance, we should reduce the operating voltage to the linear region of I-V curve. Table 3 shows the resistance region of present Logic and DRAM transistors at the linear region. MRAM may adopt the two kinds of transistors with the change of operating voltages of V_{ext}, V_g and other transistor parameters. As mentioned above, MRAM can not operate in the saturation region of transistor I-V curve because of the high resistance.

Table 3. Resistances of present Logic and DRAM transistors at the linear region.

Parameter	DRAM	Logic
Channel Length [μm]	0.20~0.30	0.13~0.18
V_g [V]	1.5~3	1.5~3
Tr. Resistance @ linear region [Ω]	2.1k~6.5k	0.58k~1.8k

C. *MTJ Requirements*

C-1. MTJ Resistance

MTJ should have the resistance of 4k~7kΩ . To meet this requirement, we should optimize the MTJ size and the the thickness of alumina layer, the insulating layer of MTJ. Above all, the uniformity issue of MTJ size can be cleared easily, but the thickness uniformity of alumina layer of MTJ is an another issue. Fig. 8 shows that we should develop 1.0~1.5nm thick alumina layer with good uniformity for competitive MRAM device. In fact, MTJ with such a thin alumina is required for higher MR ratio. The issue is whether such a thin layer can be deposited uniformly across the whole wafer or not. This issue was cleared already, Motorola reported the MTJ resistance with within 3% of uniformity across the wafer.[7]

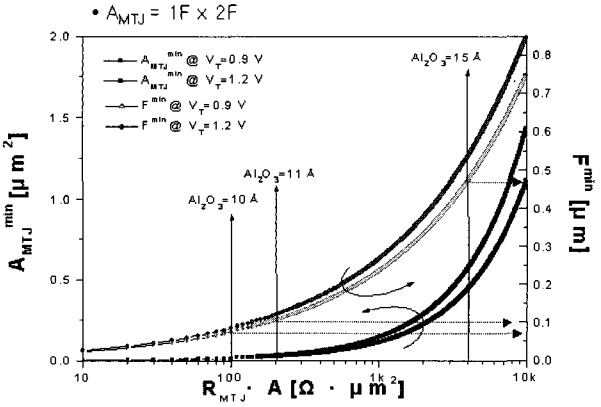


Fig. 8. MTJ scalability as a function of RA and tunnel barrier thickness.

The other layers of MTJ are generally thicker than the insulating alumina, and the uniformity issue is not critical as alumina. So, all the issues are cleared already on the deposition of MTJ.

C-2. MTJ Etch

The photo process is not a concern at the present MRAM development status. But, the MTJ etch is not a usual process in Si process, so there are plenty of issues. Now, two types of MTJ etch methods are possible. One is to etch magnetic free layer and stop at the tunnel barrier alumina, and then etch remained MTJ stack after developing different photo process, two-step etch. The other is to etch whole stack of MTJ with same mask. The two-step etch technology is quite mature already, and it has been applied to real wafer process for MRAM. The MTJ whole stack etch technology is on the development, and Fig. 9 shows the sample etch profile of MTJ. The main issue of this method is the sidewall re-deposition, which leads to electrical short. Fig. 9 does not show this problem.

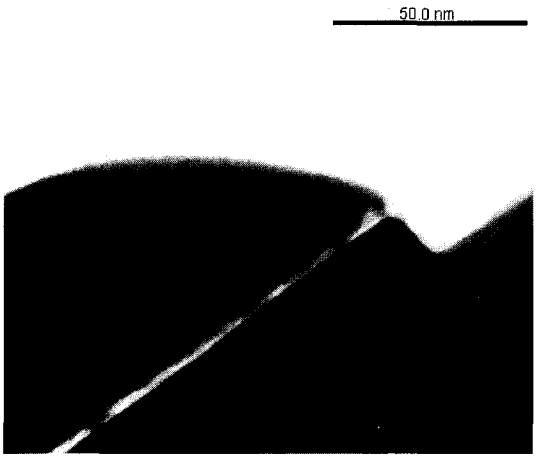


Fig. 9. The profile of whole MTJ etched with one mask.

Fig. 10 shows the typical MR ratio trend by MTJ deposition, etch and magnetic annealing. This 1.2㎛*2.4㎛ size MTJ shows about 42% of MR ratio and 16Oe of switching field. MR ratio is quite acceptable, the switching field should be reduced further. This switching field requires the current of mA level. Even if the magnetic switching occurs with the time frame of sub-nsec, the high current value for writing is not acceptable for low power mobile applications. So, we should reduce the switching field itself and the gap between the MTJ and the writing conducting lines. In parallel, flux concentrating cladding to focus the generated magnetic field has been tried. The flux-concentrating layer is composed of a thin layer of soft ferromagnetic material.

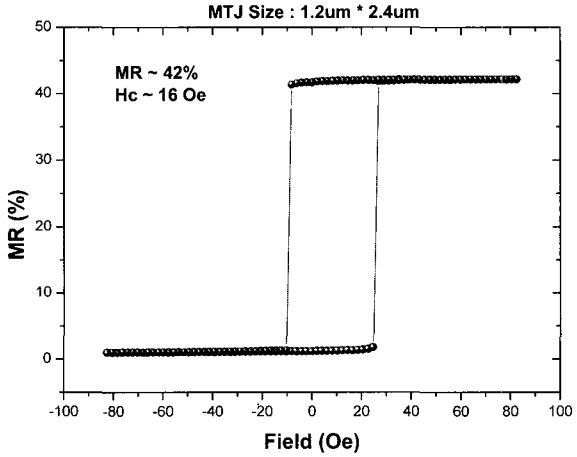


Fig. 10. MR-H curve for 1.2㎛*2.4㎛ size MTJ.

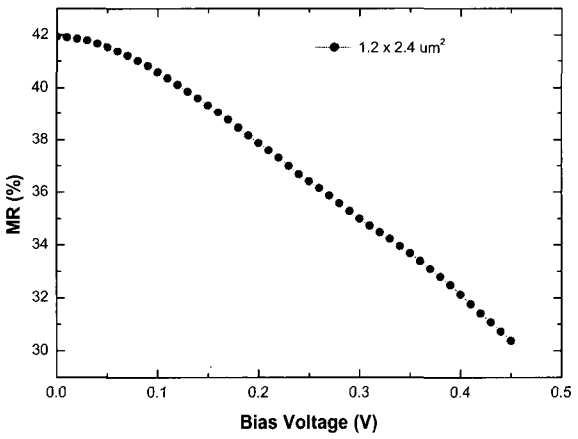


Fig. 11. MR-V curve for 1.2㎛*2.4㎛ size MTJ with Al-O insulating layer.

C-3. MTJ Properties

C-3-1. Voltage Dependency

Another issue for MTJ is the MR dependence of applied voltage. The obtained MR ratio of 42% shown in Fig. 10 is for the applied voltage of about 10 mV. The more applied voltage across MTJ, the less MR ratio we have. Fig. 11 shows the typical MR ratio dependence on

the applied voltage. We assume the applied voltage on MTJ in a real MRAM cell as 0.3~0.5V, many works have tried to get more MR ratio at this bias voltage. It strongly depends on the species of MTJ insulating layer. The alumina has been accepted generally for the insulating tunnel barrier. Different tunnel barriers other than alumina have been investigated, Al-N tunnel barrier was reported to have better MR ratio dependence of applied voltage.[8]

C-3-2. MTJ Shape Dependency

The magnetic switching field of MTJ depends on the free layer thickness, aspect ratio and the shape of MTJ. These factors exert important effect on not only switching field itself, but also it's bound. In other words, these factors are strongly connected to the reliability of TMR MRAM. Many people predicted that sub-micron size magnetic layer smaller than a magnetic domain will be single magnetic domain. But, Shi et al.[9] proved experimentally that it is not true. They observed that sub-micron size magnetic layer is not a magnetic domain and there are end domains along the edge. So, above factors are very important issues for MRAM. Fig. 12 shows the switching fields for elliptical MTJs with the variations of MTJ size and free layer thickness.[9] Aspect ratio is 1.6 in this case and the smaller aspect ratio approaching 1, the smaller switching field. So, we should make thinner free layer of MTJ with smaller aspect ratio. Elliptical MTJ needs more switching field than tapered. Rectangular MTJ needs smaller switching field than tapered.[10] Then, rectangular can be thought to be the best shape. But, this has more end domains, lower MR ratio and larger bound switching field.

D-4. MRAM Cell Scalability

Fig. 13(a) shows the MRAM cell structure with combination of a CMOS transistor and a MTJ. SEM view of fabricated cell cross-section up to metal 2 layer is shown in Fig. 13(b). The minimum cell size of MRAM is $8F^2$ or $12F^2$ with given technology design rule F which is the minimum finite feature. Eventually, $8F^2$ is possible, but $12F^2$ will be seen mainly for the time being. Fig. 14 shows the MRAM cell with $8F^2$ and $12F^2$. Fig. 15 shows the MRAM cell size shrinkage trend compared to other memories.

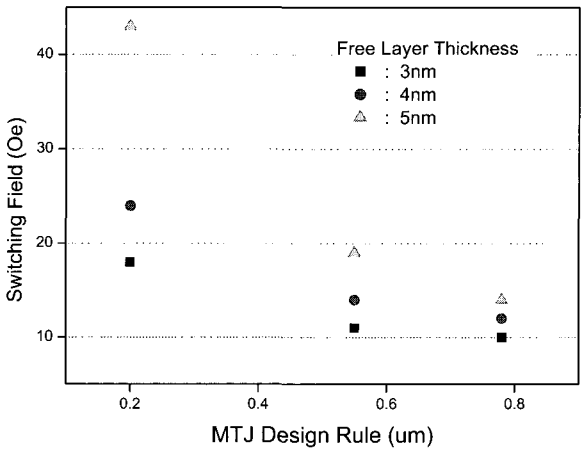
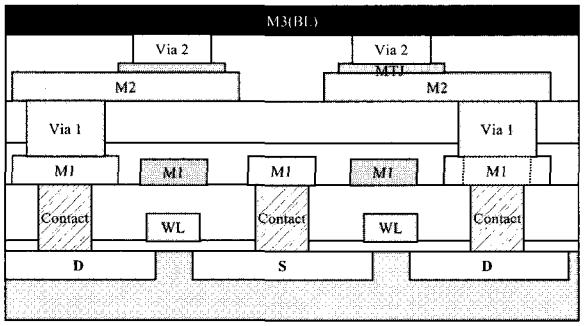
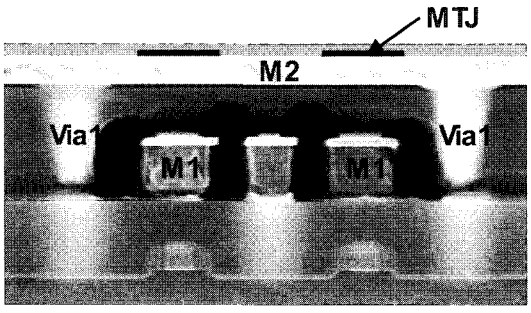


Fig. 12. Switching field dependence on MTJ design rule for various free layer thicknesses.



(a)



(b)

Fig. 13. 1T1J type MRAM cell.

IV. CONCLUSION

A new device MRAM utilizes spin dependent electron tunneling thru extremely thin insulator. MRAM requires the whole magnetic technology developed, magnetic material etch and integration technologies. We also need the technology of device design and test. Magnetic

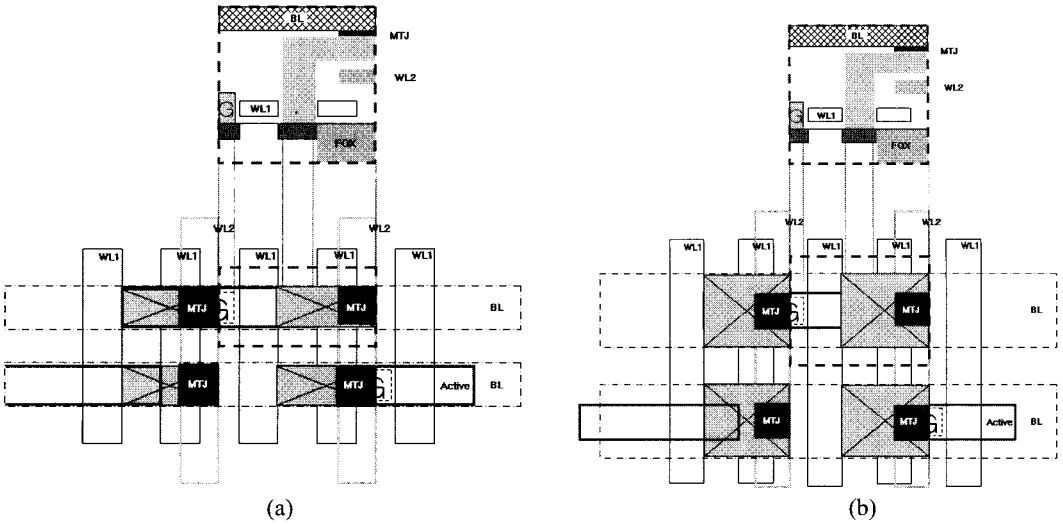


Fig. 14. $8F^2$ (a) and $12F^2$ (b) MRAM cells.

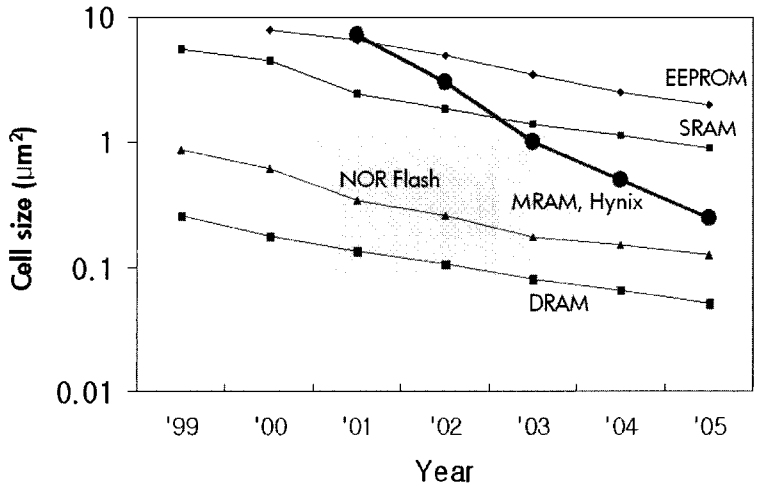


Fig. 15. MRAM cell size reduction against other memories.

materials are transition metal elements, and their thin film property strongly depends on the microstructure. So, the development of MRAM is a combination of well developed magnetic and Si technologies.

For magnetic side, GMR and TMR devices are hetero-structure composed of magnetic multi-layers. We need plenty of knowledge on them, because we may require new MR device with over 100% MR ratio in the future. Now, MRAM development is on the test chip, the spin dependent tunneling is a hot issue for magnetic material physics. Magnetic active devices such as spin transistor, spin FET and spin dependent effect for single electron tunneling, etc. have been investigated for the future magnetic applications.

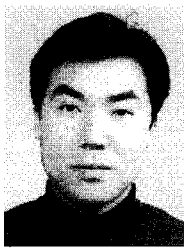
MRAM is a radiation hard memory technology, so MRAM already have had a market for space and military applications. We have flash and FRAM devices as non-volatile memory. Flash already has huge market, and FRAM would be market in soon. MRAM has several merits of faster read/write operation speed and low power operation for mobile applications. And the magnetic storage is much more stable than electrical storage, so MRAM may take niche memory market first and has a potential to be substitute for present DRAM as mainstream memory. DRAM technology depends on the development of new capacitor material and design, but it

is quite uncertain to keep its pace further.

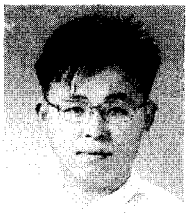
The key issues of MRAM technology as a future memory candidate are resistance control and low current operation for small enough device size. Switching issues are controllable with a choice of appropriate shape and fine patterning process. Finally, it should be pointed out that control of fabrication is rather important to realize an actual memory device for MRAM technology.

REFERENCES

[1] S.S.P. Parkin et al., J. Appl. Phys. 85 (1999) 5828.
[2] J.M. Daughton, Ferroelectrics, 116 (1991) 175.
[3] J.C. Slonczewski, Phys. Rev. B39 (1989) 6995.
[4] A. Yelon, in "Physics of Thin Films: Advances in Research and Development, edited by M. Francombe and R. Hoffman (Academic, New York, 1971), Vol.6, p. 205.
[5] S.S.P. Parkin, Phys. Rev. Lett. 71 (1993) 1641.
[6] M. Julliere, Phys. Lett. 54A (1975) 225.
[7] S. Tehrani et al., The Int'l Symposium on Magnetics of KMS, Sept. (2000)
[8] H.J. Shim et al., J. Appl. Phys. 92 (2002) 1095.
[9] J. Shi et al., IEEE Trans. Magn. 34 (1998) 997
[10] T. Zhu et al., IEEE Trans. Magn. 33 (1997) 3601

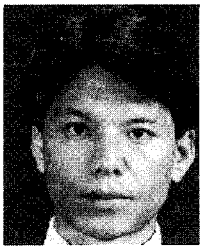


Chang-Shuk Kim is a member of technical staff of memory research and development of division at Hynix Semiconductor Inc., Korea. Since 2001, he has worked on the development of MRAM. He received his PhD from Seoul National University in 1999. He had worked at IBM Almaden Research Center, USA during 1999-2000.

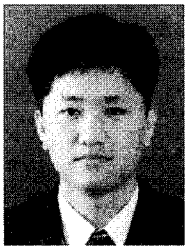


In-Woo Jang is a member of technical staff at Hynix Semiconductor Inc., Korea. He is currently a member of new device team developing MRAM since 2001. He received his MS in Physics from Korea University in 2001.

Kye-Nam Lee was born in Seoul, Korea. on December 17,1962. He received the B.S. in 1986 and M.S. in 1988 and Ph.D. degree in materials engineering from Korea Advanced Institute of Science and Technology(KAIST), Korea, in 2001. He joined LG Semiconductor in 1989 and now working for Hynix Semiconductor Inc., as a leader of MRAM development. He had worked on DRAM and Logic development during 1989-1998 and has been working the process integration and device analysis of MRAM development since 2001.

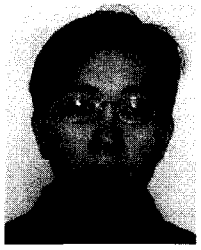


Seaung-Suk Lee was born in Seoul, Korea. on April 14,1959. He received the M.E and Ph.D. degree in materials engineering from Korea Advanced Institute of Science and Technology (KAIST), Korea, in 1987 and 1996, respectively. He joined Hynix Semiconductor Inc., Ichon, Korea, in 1989, where he has been working on the CVD process development of DRAM, and the process integration and device analysis of FeRAM.



Sung-Hyung Park received the B.S. degree in physics from Konkuk University, Seoul, Korea, in 1996. In 1996, he joined LG Semicon, Co., Ltd, (merged with Hyundai Electronics Industries Co., Ltd.), Choongbuk, Korea, where he has been involved in the development of 0.25, 0.18 CMOS technologies, respectively. His research interests are in the and 0.15 areas of CMOS devices, P2ID, junction engineering, self-aligned silicidation, m CMOS technology and design-rule. He is now involved in developing a 0.13 especially in device design and process of record.

Geun-Sook Park is a member of technical staff at Hynix Semiconductor Inc., Korea. She is currently a member of new device team developing 0.13um logic device, FeRAM and MRAM. She received her MS in electrical engineering from Korea Advanced Institute of Science and Technology (KAIST) in 1998.



Keun Do Ban is a Member of Advanced Tech. Team developing 0.10um device, FeRAM and MRAM. He has worked on Memory R&D at Hynix Semiconductor Inc., Korea from 1997.

Young-Jin Park is vice president at Hynix Semiconductor Inc., Korea. He is currently a leader of new device team developing 0.13um logic device, FeRAM and MRAM. He received his MS and PhD in materials science and engineering from Korea Advanced Institute of Science and Technology (KAIST) in 1987 and 1990, respectively. He had worked on DRAM development at Hyundai Electronics, Korea during 1990-1997 and at Infineon Technologies, USA during 1997-2000.