A Novel Sensing Circuit for 2T-2MTJ MRAM Applicable to High Speed Synchronous Operation

Eun-Jung Jang, Jung-Hwa Lee, Ji-hyun Kim, and Seungjun Lee

Abstract - **We propose a novel sensing circuit for 2T-2MTJ MRAM that can be used for high speed synchronous operation. Proposed bit-line sense amplifier detects small voltage difference in bit-lines and develops it into rail-to-rail swing while maintaining small voltage difference on TMR cells. It is small enough to fit into each column that the whole data array on selected word line are activated as in DRAMs for high-speed read-out by changing column addresses only. We designed a 256Kb read-only MRAM in a 0.35μm logic technology to verify the new sensing scheme. Simulation result shows a 25ns RAS access time and a cycle time shorter than 10 ns.**

Index Terms – **MRAM, Sensing, TMR, 2T-2MTJ, page mode, synchronous operation, MR ratio**

I. INTRODUCTION

Magnetoresistive RAM(MRAM) has several advantages including nonvolatile storage, unlimited read and write endurance, low power, high density and high speed, all of which enables MRAM architectures to be studied for long[1][2].

MRAM architectures are mainly based on Giant Magneto Resistance(GMR) cells. GMR effect is observed in the structure of two or more magnetic layers separated by a non-magnetic layer. GMR material basically consists of three layers; a soft magnetic layer, a hard magnetic layer and a noble metal layer or a dielectric barrier layer that isolates either end. Two kinds of GMR structures are the pseudo spin valve(PSV) and the magnetic tunnel junction(MTJ). The PSV structure consists of three layers; a thin magnetic layer, a metal interlayer and a thick magnetic layer. Neither of the two magnetic layers is pinned contrary to the spin valve. More current is required to change the polarization of the thick magnetic layer. Information is stored in the two possible polarization states of the thick layer. The resistance of the memory bit is low if the relative polarization is parallel. On the contrary, the resistance is high if the polarization is anti-parallel. The MTJ structure includes the tunneling layer between the two magnetic layers. In the case of the MTJ structure, voltage is applied in vertical orientation. The difference of the tunneling current in quantity is caused by the polarization state. Therefore information is stored as resistance of R_H or R_L, which is called Tunnel Magneto Resistance (TMR). TMR shows even higher MR ratios and has high resistance that it is very promising to make a small MRAM cell comparable with DRAM cells.

Several prototypes of MRAMs based on MTJ structure have been reported[4][6][7] to prove the operability of MRAM cells. However, the basic architecture doesn't take account practical DRAM or SRAM architectures that allow page-mode operation for high-speed synchronous read-out. We propose a new sensing circuit that provide stable operation and is small enough to fit into 1~2 column pitches as in DRAMs.

This paper will first discuss design constraints on sensing circuits for the synchronous operation and recent

Manuscript received July 1, 2002; revised September 10, 2002.

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developments in MRAM architectures. Then, the new sense amplifier will be explained and the simulation results will be given based on 256Kb cell arrays.

II. Design Constraints on Sensing Circuit for Synchronous Operation

There are two basic constraints on sense amplifier design; one is to guarantee enough sensing margin and the other is to make it small. In MRAM cells, the sensing margin depends on two factors; Magneto Resistive(MR) ratio variation and the turn-on resistance, R_{on} of the pass transistor connected to TMR to form a storage cell.

MR ratio depends on the voltage applied to the MTJ. It changes little with a small voltage bias, whereas it decreases significantly at higher bias. It reduced by half when the voltage reaches the critical voltage such that it cannot function as a storage element. Therefore, it is critical to control the voltage applied to the MTJ not to reach the critical voltage which is in the rage of 0.6 ~ 1.0V.

When the data is read by detecting the difference of the reference cell and the data cell in the 1T/1MTJ structure, R_{on} of pass transistor can be too large compared with TMR value. This makes the sensing of the voltage difference of bit line difficult. Consequently, it is necessary to tune the size of the pass transistor. Fig 1 shows an example of the characteristic curve of the pass transistor and MTJ load line. If the data that gives the quantity of current according to the variance of the voltage applied to the MTJ is given, it is possible to draw MTJ load line and the characteristic curve of pass transistor. In this way, we can set the size of the pass transistor. In the case of the current forcing, assume that the total voltage across the MTJ and the pass transistor is P3 in Fig 1. The distance from the origin to P1 indicates the voltage across the pass transistor and the distance from P1 to P3 indicates the voltage across the MTJ. Then, the gap between P1 and P2 is the voltage difference caused by the difference of the MTJ resistance. The larger the voltage difference is generated, the better in the aspect of easy sensing.

For page-mode operation, the size of the sense amplifier needs to be small enough to fit into at most 4-cell pitches in the case of adopting the shared sense amplifier structure. When a word-line is selected, all the sense amplifiers connected to the selected row are activated and generate fully-developed data ready for consecutive read-out by asserting only column addresses, or clock signal in the case of synchronous operation.

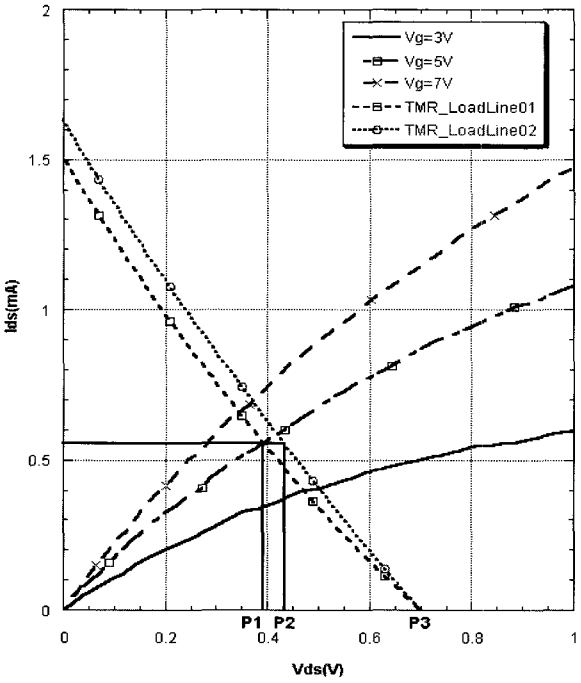

Fig 1. MTJ load line with I_{ds} - V_{ds} curve of pass transistor.

III. Recent Developments

IBM proposed voltage clamped sensing [4]. The information is stored in a twin cell arrangement where two adjacent cells written to opposite states. The information is read by comparing the resistance of adjacent MTJs of the twin cells. In this sensing scheme, transistors in saturation mode clamp the voltage on the nodes connected to the MTJs and limit the voltage across the MTJs. Therefore this scheme avoids the decrease of MR ratio. The sensing circuit consists of a transresistance preamplifier, a differential stage and a differential to single ended conversion stage to full voltage swing. And the bias applied to the gate of the transistors in saturation mode above mentioned is generated to the desired sense line voltage level. The feedback loop replicates one half of the transimpedance preamplifier circuit. In this way the sense amplifier can

accommodate variations on MTJ resistance. The sense line swing is limited to 300mV. The sense amplifier is shared by all of the memory cells in the array, such that the whole reading process has to be restarted to read from another cell in the array.

The sensing scheme using the differential current was proposed by Motorola based on 1T/1MTJ cell structure[7]. The information in a selected cell is read by comparing its resistance with the resistance of a reference cell in the same wordline using the differential current conveyor. Each reference cell acts as reference for 64 cells to its left and 64 cells to its right. An actual current conveyor is shared by 32 bitlines and the reference bitline has its own current conveyor. The actual and reference current conveyors form a differential pair. The current conveyors clamp the voltages of bitlines and those of reference bit lines. This limits a constant bias across the MTJs regardless of MTJ resistance variations. The 256Kb MRAM using the current conveyor sensing scheme operates with address access time and cycle time of 50ns. This 1T/1MTJ cell has advantage in terms of area efficiency, but is highly sensitive to process variation. Also, the sensing circuit is made pretty big for reliable sensing that it can only fit into 32 cell-pitches.

A small sense amp identical to that of DRAMs was adopted in the new sensing scheme proposed in [8]. Even though the sense amplifier is made very small, the scheme requires very accurate timing control, which has been implemented with multiple clock singals. The reliability of sensing operation is heavily dependent on relative timing of those clock signals.

IV. The Sense Amplifier with Clamped Voltage Swing

As mentioned above, it is necessary to generate a large voltage difference caused by the difference of the MTJ resistance for easy sensing. In the twin cell structure, two adjacent cells are always written to opposite states and one cell function as a reference to the other cell. In this structure, it is needless to make the additional reference cell which has the resistance of middle value between logic "0" and logic "1". The current is a loop following up one bit line and down the adjacent bit line of the twin cell pair. Thus the current loop makes it possible to make the opposite state cell pair. As compared with sensing the cell resistance relative to a reference resistor, the twin cell arrangement doubles the signal available for sensing and provides protection from common mode noise. Therefore we adopted twin cell pair structure for the stable operation at the expense of the size.

The proposed sensing scheme is detecting the potential difference on both ends of the cells (Fig. 2). In this sense amplifier structure, the bit-lines (bit, bit_b) are separated from the output nodes (out, out_b) that the bias voltage across TMR remains unaffected when the sense amp is activated. Current source at each bit-line provide the same amount of current to the twin cell pair and produce voltage difference due to the resistance difference of the twin cell pair.

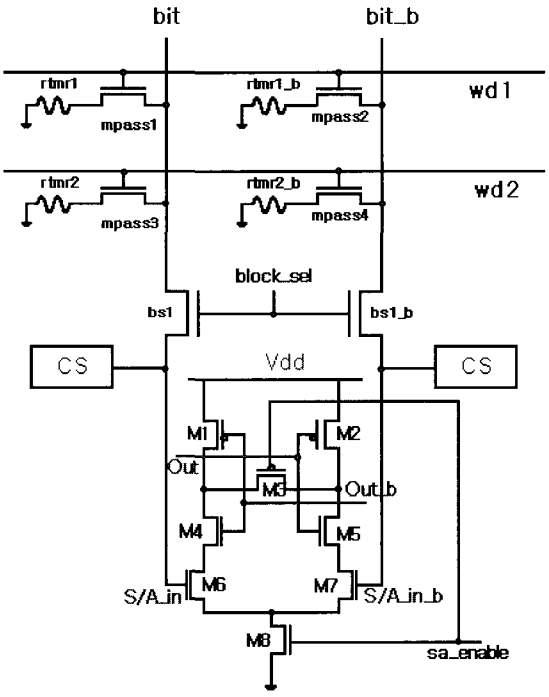

Fig 2. Current source bit-line clamped Sense Amplifier structure.

After the sense current is provided, the potential on both ends of the cells, bit and bit_b are connected to the input of the sense amplifier passing through the block select transistors (bs1, bs1_b). And the difference of the MTJ resistance is converted into the voltage difference that leaves an enough margin for the input of the sense amplifier by passing through the pass transistors and the

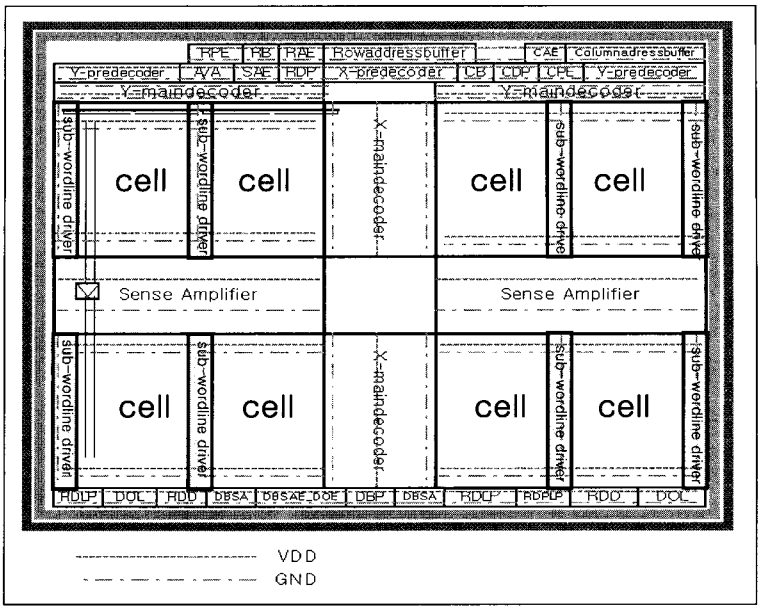

Fig 3. read-only MRAM block diagram.

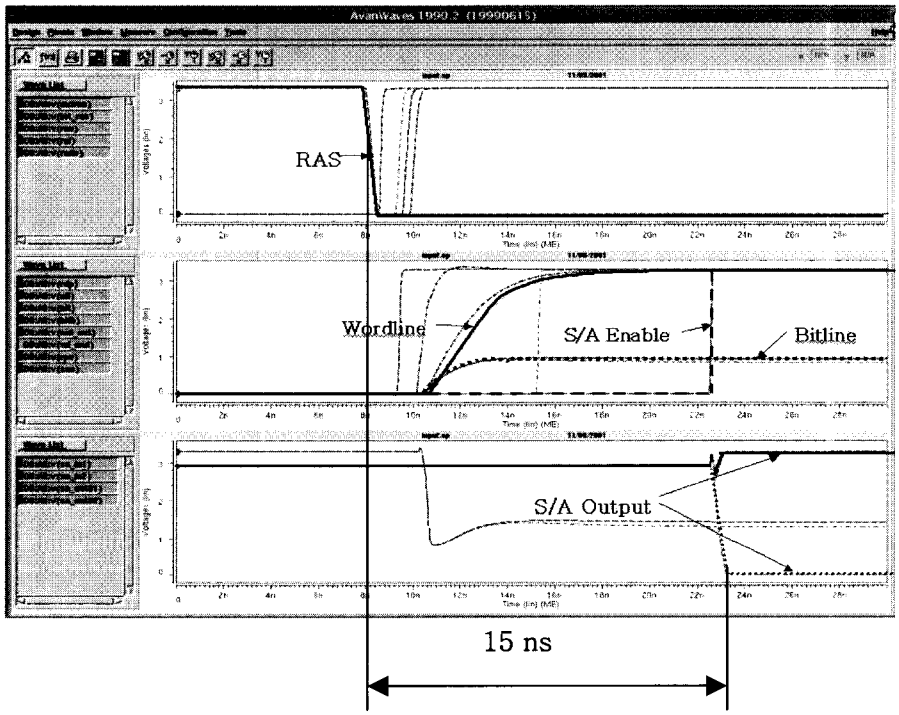

Fig 4. Row-Path Simulation.

block select transistors. Once the voltage difference is detected at the input nodes, it is amplified by the PMOS transistors M1,M2 and the NMOS transistors M4,M5. Unless the sensing is proceeded, output nodes are equalized by PMOS transistor M3.

This scheme has the feature that clamps the bit-line voltage after sensing within 0.6V range, which produces little degradation of MR ratio. Careful sizing gives ~100mV sensing margin which is usually considered enough for reliable bit-line sensing in DRAMs. Also the

Table 1. Key features.

Process	0.35㎛ CMOS (1 Poly / 4 Metal)
Organization	128K x 2
Supply Voltage	3.3 V
Access Time	25 ns
Cycle Time	10 ns
MR ratio	18 % (2.5K㏀ ~ 2.95K㏀)
Chip Size	4mm x 4mm (including PADs)
Cell Size	4.65 ㎛ x 3.15 ㎛

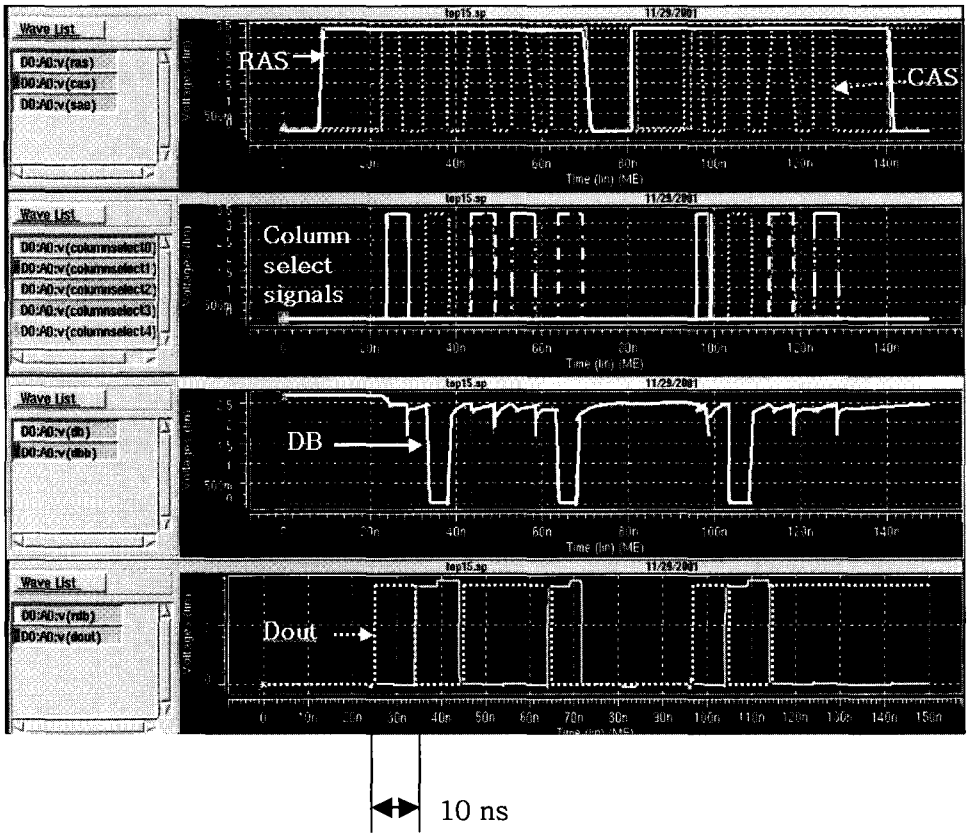

Fig. 5. Page-Mode Operation.

size of the current sense amplifier is small enough to fit into the 4-cell pitch that it can be placed in every column in shared sense amp architecture. Consequently, the page mode of a DRAM is possible and can operate synchronously like most of recent DRAMs and SRAMs.

V. 256Kb Read-Only Mram

We designed the 256Kb read-only MRAM to verify the sensing scheme proposed in this paper. The MTJ was simulated with a pair of unequal MOS devices that gave the same resistance as TMR at given operating condition. This is used to confirm circuit operation independent of the MTJ process. Writing was not implemented with our simulated cells. In MRAMs writing is performed with separately provided digit line while the sense amplifier is disabled, such that we can fully verify the operation of our sensing circuit with the read-only simulated cells.

The device consists of 4 sub-blocks composed of 256

rows by 256 columns. X-main decoder combines a main wordline driver and a main decoder. To reduce the RC delay of the wordline, X-main decoders are located at the center and two sub-wordline drivers are located at each sub-block. The shared sense amplifier architecture was used. At each address 2-bit output is generated, one bit is from the left cell arrays and the other is from the right cell arrays. The chip was designed using a 0.35μm logic process. The chip size is 4mm x 4mm. The MR ratio of our simulated MRAM cell is assumed to be 18% which is in accordance with reference[4]. We adopted 2T-2MTJ structure and the cell efficiency of our chip is about 0.90. The cell efficiency of 1T-1MTJ structure would be about 0.81 with 45% smaller chip size . The key features of our device are summarized in Table 1.

Figure 4 shows the simulation waveform at row path. It shows the output of the sense amp is fully developed in 15ns after RAS is asserted. Figure 5 shows the simulation result of page-mode operation. Column address changes every 10ns and data output changes accordingly. Thus, the RAS access time(t_{RAC}) can be estimated less than 25ns.

VI. Conclusion

As MRAM has several advantages over DRAMs and SRAMs, it has potential to replace present commercial semiconductor memories. However, there are certain circuit issues to be resolved as well as process issues.

In this paper, the design constraints for sensing circuits of MRAM has been analyzed and current research works on MRAM have been summarized. Then, we proposed a twin cell pair structure with a novel current source clamped sense amplifier for implementing high-speed synchronous MRAM. This novel sensing circuit is small enough to fit into each column pitch while limiting the bias voltage on TMR within 0.6V. 256Kb read-only MRAM array has been designed to verify our sensing circuits in 0.35μm logic process. The designed MRAM showed 25ns RAS access time and 10ns cycle time in spice simulation.

Acknowledgement

This work was performed under the 21C Frontier R&D Project supported by Korea Ministry of Science and Technology.

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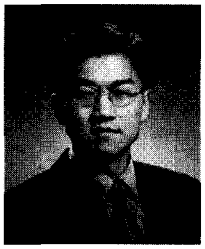

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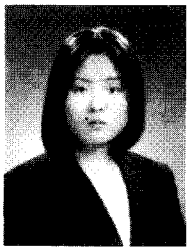

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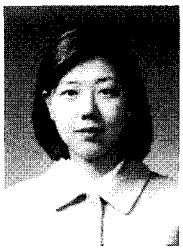

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