Field Effect Transistor of Vertically Stacked, Self-assembled InAs Quantum Dots with Nonvolatile Memory

Shuwei Li, Kazuto Koike, and Mitsuaki Yano

Abstract - **The epilayer of vertically stacked, self-assembled InAs Quantum Dots (QDs) was grown by MBE with solid sources in non-cracking K-cells, and the sample was fabricated to a FET structure using a conventional technology. The device characteristic and performance were studied. At 77K and room temperature, the threshold voltage shift values are 0.75V and 0.35 V, which are caused by the trapping and detrapping of electrons in the quantum dots. Discharging and charging curves form the part of a hysteresis loop to exhibit memory function. The electrical injection of confined electrons in QDs products the threshold voltage shift and memory function with the persistent electron trapping, which shows the potential use for a room temperature application.**

Index Terms – **Field-effect transistor, self-assemble d quantum dots, Molecular beam epitaxy, Nonvolatile Memory**

I. Introduction

Semiconductor quantum dot (QD) structures with strong quantum confinement have attracted much attention for the fundamental properties and applicability to semiconductor devices, and the self-assembled vertically stacked InAs nanodots in AlGaAs barrier is very interesting in memory effect devices [1]. The QDs can be directly created in defect-free systems using the Stranski-Krastanov growth mode in highly strained materials without lithography and etching procedure by Molecular beam epitaxy (MBE) and Metal organic chemical vapor deposition (MOCVD). To QD electronic devices the electron transport properties are extremely important for device application, and in this paper we investigate these properties through InAs self-assembled QDs and an adjacent quantum well in an $Al_{0.5}Ga_{0.5}As/GaAs$ field effect transistor. The electrical injection of confined electrons and holes of QDs products a nonvolatile memory function with the persistent electron trapping, which shows the potential for room temperature application.

II. Layer Structure

The QD sample was grown by MBE with solid sources of Al, Ga, In, and As in non-cracking K-cells [2]. In Fig.1, the layer structure consists of a buffer combined by a 10-period $Al_{0.3}Ga_{0.7}As/GaAs$ superlattice and a 300nm GaAs layer, a 50nm $Al_{0.5}Ga_{0.5}As$ layer, a 50 nm Si-doped layer among a 90nm $Al_{0.3}Ga_{0.7}As$ layer, a

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30nm GaAs quantum well channel, 5-period vertically stacked nanodots in a 65 nm $Al_{0.5}Ga_{0.5}As$ barrier layer, and a 15nm GaAs cap layer. The quantum well channel is adjacent to QDs with distance 15nm, and the doped Si layer may provide transport electrons to the quantum well channel.

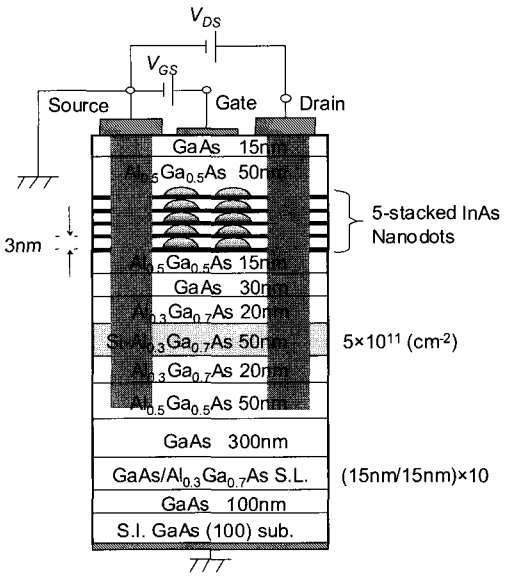

Fig. 1. the sample structure of the nonvolatile memory FET.

III. Device Characteristic and Performance

The sample was fabricated to a FET structure using a conventional technology by photolithography and wet etching, and the dimension of the gate is 2μm long and 50μm wide. The electrical measurements were carried out using an HP-4145B semiconductor parameter analyzer.

In Fig.2 and 3, the drain current-voltage (I_{DS}-V_{DS}) characteristic after discharging and charging at room temperature of, the measured I_{DS} curve values after charging are small to that after discharging, which is contributed by the carrier transport from the quantum well channel to confined QD states, and the conductions are controlled by gate bias which changes the energy position of the Fermi level. In discharging processes, the holes are collected in the nanodots where the valence band energy is high and recombine with the trapped excess electrons [3], and the result is a reduction of the electron density in the QDs. The performance improvement should be attributed by an improved confinement of the QDs and the high 2DEG density in the quantum well.

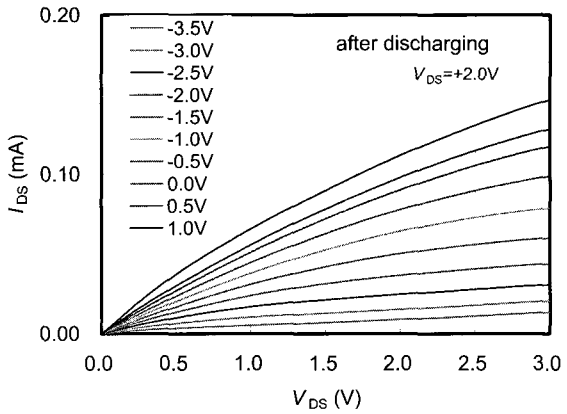

Fig. 2. I_{DS}-V_{DS} curve after discharging.

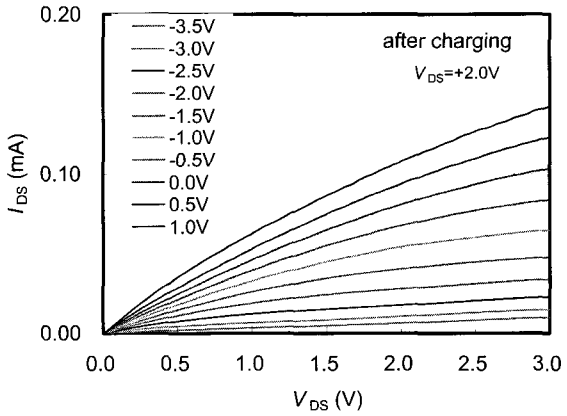

Fig. 3. I_{DS}-V_{DS} curve after charging.

Figure 4 is the characteristic of the drain-source current (I_{DS}) in respect of the gate-source voltage (V_{GS}) of the discharging and charging at 77K, and the drain-source voltage (V_{DS}) kept at 2.0V. The threshold voltage shift value is 0.75 V, which is caused by the trapping and detrapping of electrons in the QDs [4]. At room temperature the threshold voltage shift value is 0.35 V. The discharging and charging curves form the part of a hysteresis loop to exhibit memory function, which also is caused by the charge injection to the nanodots from the quantum well 2DEG. When the device is taken into forward bias, 2DEG QW electrons flow to the QDs, and deep trapping centers play a critical role in the memory function where excess charges are stored in deep traps.

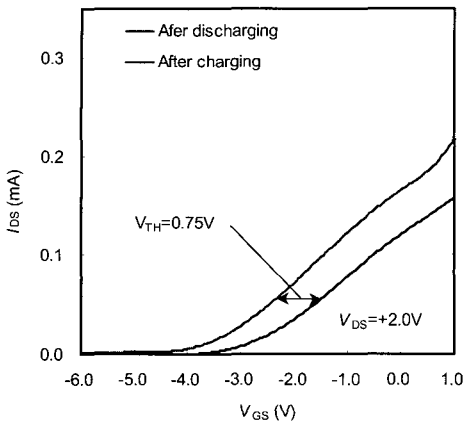

Fig. 4. Vth shift curve at 77K. Discharging and charging curves form the part of a hysteresis loop to exhibit memory function.

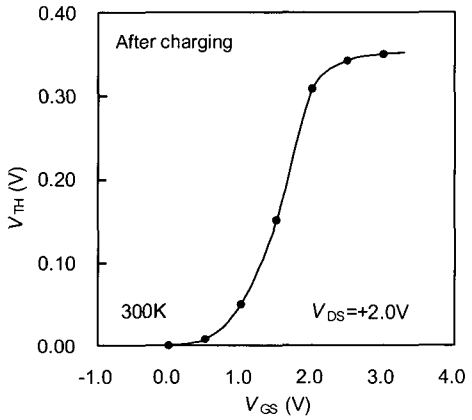

Fig. 5. The curve of the threshold gate voltage shift at room temperature.

Figure 5 shows the positive shift of the threshold gate voltage (ΔVth) dependencing on the gate charging voltage at room temperature, and at 3.0 V the threshold voltage shift value becomes saturation because the trapping levels of the QDs are then fully occupied. So, the electrical injection of confined electrons and nanodots products the threshold voltage shift and memory function with the persistent electron trapping, which reflects an important factor to realize a memory application of a long-term retention. In our case, the least retention time is about 10^6s.

VI. Conclusions

The 5-stacked self-assembled QDs is incorporated in parallel to the quantum well channel associated with strong quantum confinement of electrons and holes, which is very helpful for the further improvement of optoelectronic device performance and the application of nonvolatile memory devices with long charge retention time at room temperature.

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The biography and photograph of the author is not available at the time of publication.