A RF Frong-End CMOS Transceiver for 2GHz Dual-Band Applications

Yong-Sik Youn, Nam-Soo Kim, Jae-Hong Chang, Young-Jae Lee, and Hyun-Kyu Yu

Abstract— This paper describes RF front-end transceiver chipset for the dual-mode operation of PCS-Korea and IMT-2000. The transceiver chipset has been implemented in a 0.25μm single-poly five-metal CMOS technology. The receiver IC consists of a LNA and a down-mixer, and the transmitter IC integrates an up-mixer. Measurements show that the transceiver chipset covers the wide RF range from 1.8GHz for PCS-Korea to 2.1GHz for IMT-2000. The LNA has 2.8~3.1dB NF, 14~13dB gain and 5~4dBm IIP3. The down mixer has 15.5~16.0dB NF, 15~13dB power conversion gain and 2~0dBm IIP3. The up mixer has 0~-2dB power conversion gain and 6~3dBm OIP3. With a single 3.0V power supply, the LNA, down-mixer, and up-mixer consume 6mA, 30mA, and 25mA, respectively.

Index Terms —RF CMOS IC, Wireless Front-end, Dual-band Transceiver, PCS, IMT-2000.

I. INTRODUCTION

In the near future, as third-generation wireless systems are launched, there will be an increasing demand for multiband capabilities [1], [2]. It is desirable to combine two or more standards in one mobile unit for overall capacity enlargement, higher flexibility, and roaming capability as well as backward compatibility. Moreover, multi-standard transceivers will allow access to different systems providing various services [3], [4]. These are the cause of the instigation for the multi-band multi-mode operation.

This paper presents the design and implementation of a pair of dual-band CMOS RF front-end transceiver ICs for PCS-Korea and IMT-2000 standards. The optimal multi-standard transceiver should be as simple and small as possible. Hence, it would be advantageous if the transceiver could share as many of its building blocks as possible in all operation bands. The front-end transceiver presented in this paper use its building blocks in common in both bands. Section II describes the design of the building blocks. Experimental results are presented in Section III and the paper is summarized in Section IV.

II. CIRCUIT DESIGN

This prototype CMOS RF front-end transceiver chipset is intended for PCS-Korea and IMT-2000 mobile units. The simplified block diagram of the RF front-end transceiver is shown in Fig. 1.

The receiver IC consists of a LNA, a down-conversion mixer, and the transmitter IC integrates only an up-conversion mixer. The designed transceiver ICs together with external band-select filters and a power amplifier including driver, complete the RF front-end and interface with the IF signal block providing channel selection filter, variable gain amplifier, IF-BF conversion mixer, and low pass filter.

A. Low Noise Amplifier (LNA)

The primary goal of a LNA is to keep the overall

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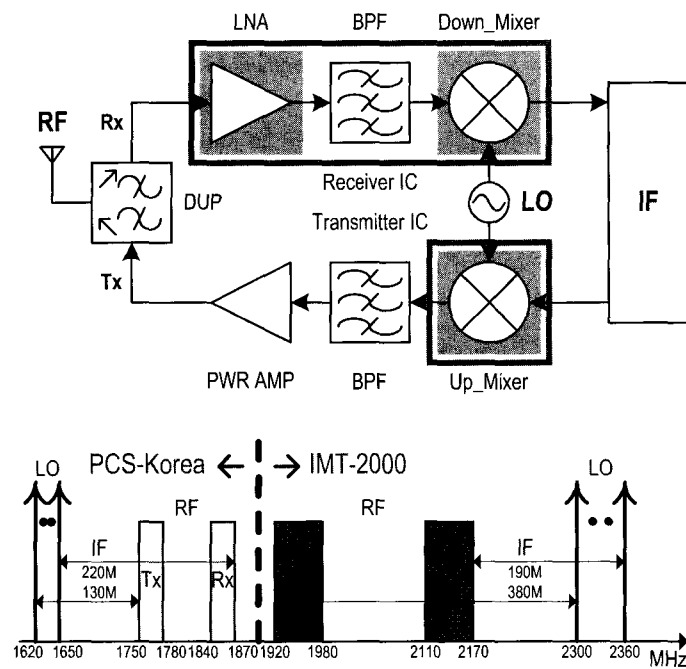
Fig. 1. Simplified RF front-end transceiver architecture.

noise figure of the receiver low enough by screening the relatively large noise of the following mixer by the gain of the LNA. The essential requirements of a LNA are low noise, high gain, high linearity, and low power consumption.

The inductively degenerated LNA depicted in Fig. 2 is the most suitable from the above requirements standpoint as well as input 50Ω matching because the gate of a MOS transistor (M1) is purely capacitive [5]. It is well known that the resistive part in the input impedance can be expressed as (gm/Cgs)*Ls of the input stage. In addition, the signal swing across Cgs is proportional to the quality factor (Q) of the input network by the resonating between Lg and Cgs [6]. Thus the noise figure can be improved so much by increasing the signal voltage across Cgs, which is due to the fact that it has the same effect as a noiseless amplifier exist in front of the main amplifying transistor (M1). However, the linearity of the LNA is degraded as much as the signal voltage across Cgs increases. So the trade-off between noise and linearity is required. The cascode transistor (M2) provides better reverse isolation, and enables M1 drain more induced output current by alleviating the miller effect of Cgd in M1.

To obtain higher gain than that of the conventional cascode structure, a transistor (M3) is used additionally

to drive the gate of M2 after boosting the drain voltage of M1. This structure so called "regulated cascode" has higher output impedance by gm*R0 and thus can get higher its gain [7]. In radio-frequency range, however, the gain does not depend so much on the output impedance because the parallel loaded inductor does not have high Q. Adding M3 as well as M2 forces the signal swing at M1's drain node so small that this alleviates the miller effect of M1 furthermore. By these two positive effects, simulations show that this structure has higher gain above 2 dB than the conventional cascode structure.

The biasing current and transistor size of the LNA must be chosen to optimize the above mentioned requirements. The M1 was decided to drain 5mA biasing current and to have 200μm total gate width on the basis of measuring its noise performance. The width of M2 was selected to 100μm by considering the gain and output 50Ω matching. M3 has 40μm gate width and drains 1mA as small as possible. To reduce the noise occurred by gate resistance, all the transistors have a multi-fingered structure with 5μm unit gate width and have the double-sided gate contact of meander type [8].

The two circular spiral inductors (Lg and Ld) have 7nH and 6nH, respectively. The bond wire inductor (Ls) was assumed roughly as 1nH on the general rule of thumb that the inductance is approximately

1nH/mm [6]. Noise consideration requires that Lg should be a low loss inductor. The measured quality factor of the spiral inductors is above 8 at 2GHz with the help of 2μm-thickness top metal. Thus, Lg as well as Ld were integrated on the chip for lower cost and higher on-chip integration. The combined Ld-Cd forms the "L-matching" network for optimal power transfer to the following stage by the impedance transforming operation [6]. Cd also provides the same operation as Cg added to block both dc and low frequency harmonic components.

B. *Down-Conversion Mixer*

The LNA output signal is filtered by a LC band pass filter and down converted to IF frequency by the down mixer shown in Fig. 3. The down mixer must have sufficient conversion gain with a minimal noise contribution. Therefore, the down mixer was realized with an active Gilbert cell multiplier. The down mixer without the LO processing circuit has three-stage configuration composed of a single to differential amplifying balun, a double-balanced Gilbert cell mixer, and an output driver.

The rigid resistor (R0) was used for input 50Ω matching. It is possible to use higher resistance than the required resistance for matching. This is due to the fact that R0 can be shown as lower resistance when the combination of the parasitic bond & package inductance and the parasitic pad & gate capacitance creates series resonance. By using higher resistance over 100Ω than 50Ω resistance, we minimized the noise contribution as small as possible. The single-ended input signal is transformed to differential signal for driving double-balanced mixer input transistors, and amplified for improving noise figure degradation. The transistor (M3, M4) so called "active inductor" load, was employed to increase and flatten the gain up to the desired RF band [6].

The transistor (M5, M6) must have a large bias current to minimize its nonlinear gm component because the signal voltage at its gate node is very large by the amplifying action of the prior balun stage. Generally, the more current a transistor uses, the more linear its gm becomes. To use large bias current, however, gives a difficulty in complete switching the LO quad-transistors (M7~M10) with the LO overdrive voltage as small as

possible. Hence, we chose a current bleeding (I1, I2) method to reduce the LO overdrive required for complete switching and thus effectively to increase the conversion gain [7]. In addition, this technique also improves the voltage headroom for the quad switches. However, the linearity is degraded when the bleeding current approaches the bias current of M5 (M6). Setting the bleeding current to be half of the M5 (M6) bias current appears to be a good compromise after several simulations.
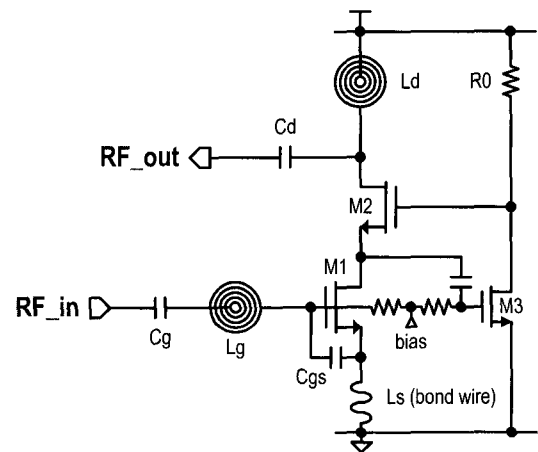

Fig. 2. LNA simplified schematic.

The mixer output driver consists of four transistors (M13~M15) and two current sources (I3, I4). To remove the third-order intermodulated signal components, we adopted the linearization technique of adding the cross coupled structure (M15, M16) to the typical differential pair (M13, M14). Since the drain current of M15 (M16) is much smaller than that of M13 (M14), the former has less fundamental and more harmonic components than the latter. Thus, we can cancel the third-order components without deteriorating the fundamental component. Simulations show that the down mixer with the third-order cancellation structure has 3dB higher IIP3 than the one with a conventional differential pair. The output signal goes out through the open-drain nodes in order to adapt various impedance matching for both PCS-Korea of 1KΩ and IMT-2000 of 200Ω.

The LO processing circuit consists of a LO balun and a LO buffer. The LO balun transforms the single-ended LO input to differential signal for driving the LO quad transistors in the down and the up mixer. The bisymmetric Class-AB topology (M17~M20) based on
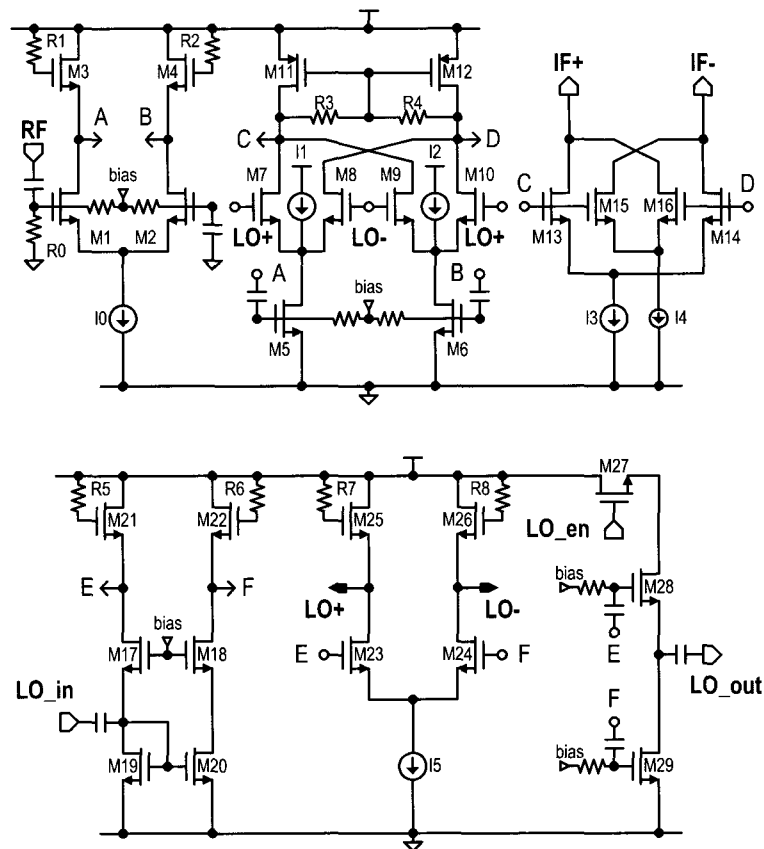
Fig. 3. Down-mixer simplified schematic.

translinear principles was selected to the LO balun. Compared with a typical differential pair converter, this topology provides the wide band 50Ω resistance suitable to impedance matching from 1.62GHz PCS-Korea to 2.36GHz IMT-2000 as shown in Fig. 1. It has been proved by our measurements that a common gate transistor has a uniform input resistance up to 20GHz. The LO buffer is required to enable other circuitry to be switched on or off depending on the status of the transceiver modes. It has a switching transistor (M27) and the push-pull structure combined with a common-source transistor (M29) to boost the signal and a source follower transistor (M28) to drive the external matched 50Ω impedance.

C. Up-Conversion Mixer

To perform the frequency translation from IF to RF, we used the double-balanced Gilbert mixer with low LO-RF feed through in the up-conversion mixer shown in Fig. 4 [7]. The up mixer without the LO processing

circuit has three-stage configuration composed of a common gate differential amplifier, a double-balanced mixer and an output driving buffer.

The common gate transistor (M1, M2) is employed in the first stage because its structure provides the required constant resistance simply for input matching at both 130MHz PCS-Korea and 380MHz IMT-2000. When connecting the first stage and the next double-balanced mixer stage, we chose a current mirroring method not to use dc blocking capacitors because IF signal suffers from its power loss more seriously than RF signal on passing through dc blocking capacitors. Since the mirrored gain is proportional to the size ratio of the driving transistor (M5, M6) and the driven transistor (M7, M8), the latter must be larger than the former in order to achieve current gain. However, the biasing current of M7 (M8) is also increased in proportional to the mirrored gain. To adjust the bias current of M7 (M8), hence, the transistor (M3, M4) was employed. The active inductor load (M13, M14) and the push-pull structure (M15, M16) are also utilized in the up mixer by the above mentioned reason.
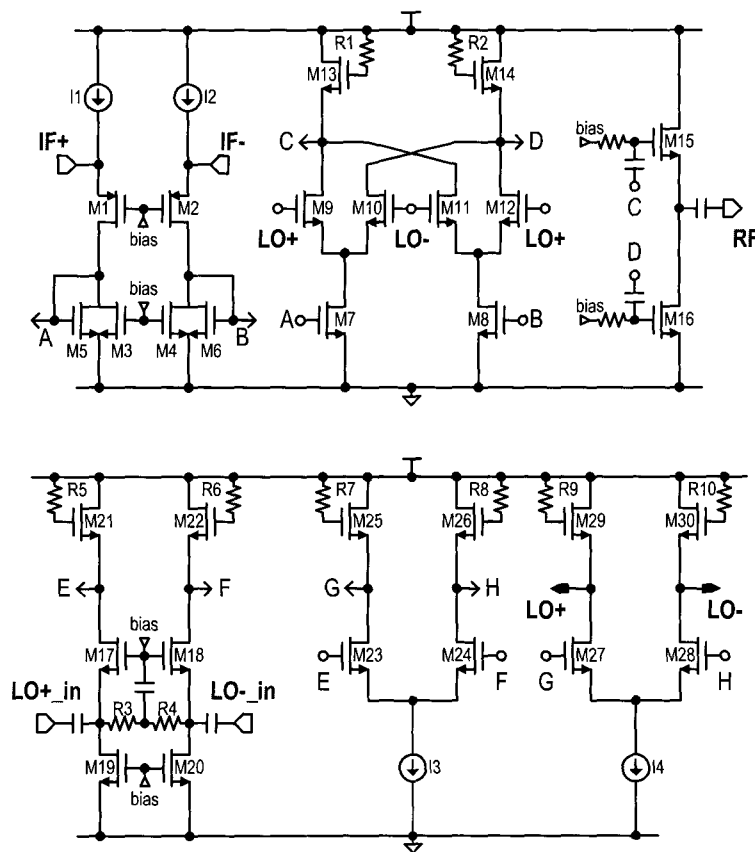
Fig. 4.   Up-mixer simplified schematic.

Though single-ended LO input is general, the LO balun in the up mixer must operate well regardless of single or differential LO input signal. To processing both the signals, a pair of the common gate transistors (M17, M18) was employed to the input stage of the LO balun. This structure has a wide band constant resistance suitable to the impedance matching from 1.62GHz PCS-Korea to 2.36GHz IMT-2000 as explained before. On the contrary to the bisymmetric Class-AB topology used in the down mixer section, this structure can not enable us to get the balun operation in the case of single-ended input signal. Thus the following double differential structures are inserted to get more balanced differential LO signal owing to its inherent balun operation.

III. EXPERIMENTAL RESULTS

The RF front-end transceiver chipset has been designed with our RF device models and fabricated in a standard 0.25μm single-poly, five-metal CMOS technology. Fig. 5 shows the die photos of the receiver

and the transmitter IC. Their die areas including the bonding pads are 2.4x1.4 mm^2 and 1.4x1.2 mm^2, respectively.
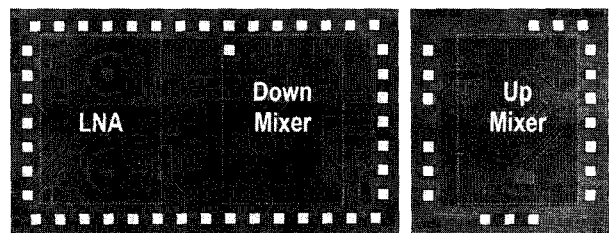

Fig. 5.   Micrograph of the RF front-end transceiver chips.

The dies have many pieces of dummy patterns inserted to guarantee uniform etching and to keep the different layers as planar as possible in today's submicron CMOS technologies [9]. The dummy patterns composed of metals and poly layers are placed around the circuits. In radio frequency range, however, dummy patterns may cause some unexpected effects especially on internal inductor. Thus, we have no dummy inside the inductors to protect eddy current loss and outside the

inductors to prevent magnetic flux deterioration. All transistors passing through differential signal have a common centroid layout to improve balancing. The LNA and mixer of the receiver has been laid out as stand-alone circuits and was tested and characterized individually.
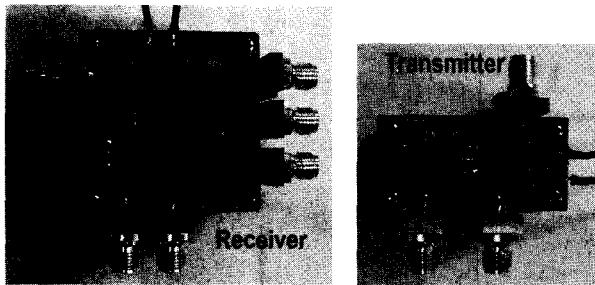

**Fig. 6.**   Transceiver ICs mounted on printed circuit boards.

Fig. 6 shows the printed circuit board for testing the receiver and the transmitter IC, which were packaged using SSOP-24pin and SOIC-8pin package, respectively. We used double or triple bonds for power and ground to minimize the bond wire inductance. Since most devices to connect the transceiver IC and external circuitry are integrated to maximize on-chip integration, as shown in Fig. 6, only a few support components are utilized except IF balun transformers. The two baluns are used for impedance transformation from IF matching impedance to the 50Ω of measurement setup. With a single 3.0V power supply, the LNA, the down-mixer, and the up-mixer consume 6mA, 30mA, and 25mA, respectively.

Fig. 7 shows the measured LNA s-parameters, noise figure and two-tone imtermodulation results. The LNA has 14~13dB gain, less than -10dB return loss and 2.8~3.1dB NF from the lowest frequency of 1.84GHz for PCS-Korea to the highest frequency of 2.17GHz for IMT-2000 in each receive band. And its IIP3 is equal to 5dBm at 1.86GHz for PCS-Korea and 4dBm at 2.14GHz for IMT-2000.

The measured results of the down mixer and the up mixer are shown in Fig. 8 and Fig. 9 including the one-tone harmonic test results for PCS-Korea and IMT-2000. As illustrated in Fig. 8 and Fig. 9, all measurements were performed using -5dBm single LO signal at the fixed frequencies for each standards. In measurements, the down mixer has 15 & 13dB power conversion gain, less
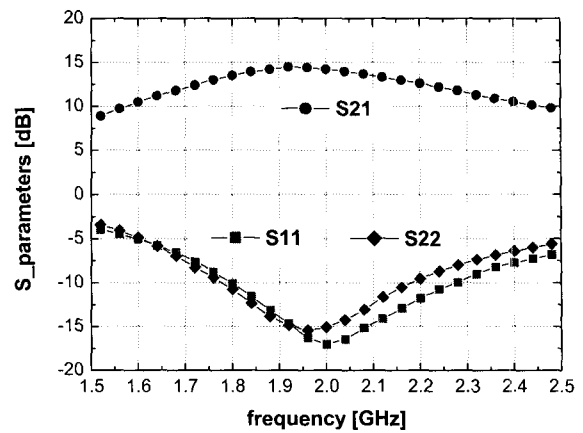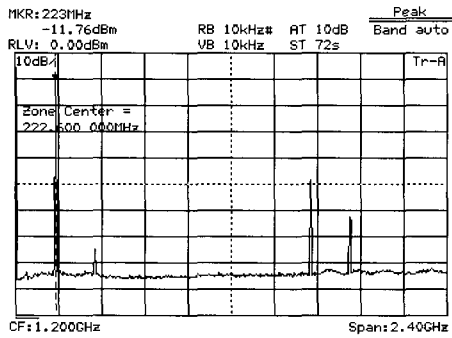

(a) S-parameter test
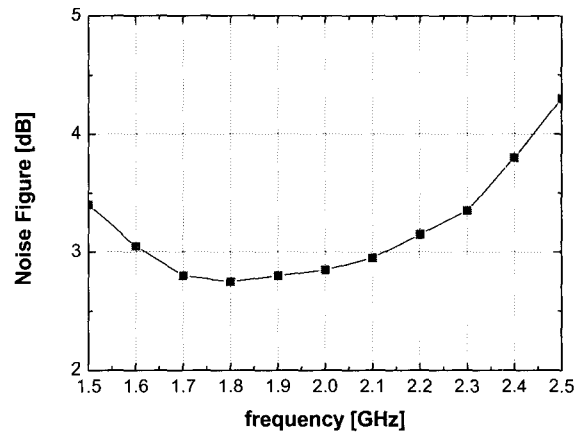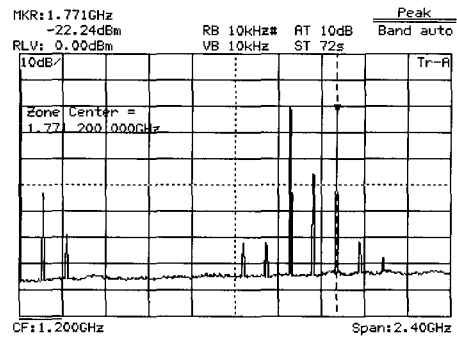

(b) Noise figure test
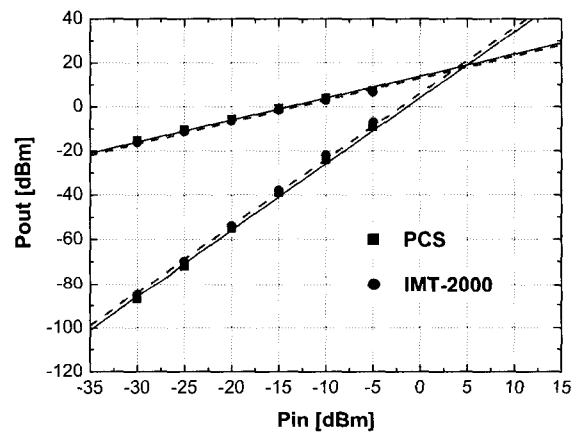
(c) Two-tone imtermodulation test
(1.86GHz for PCS-Korea, 2.14GHz for IMT-2000)

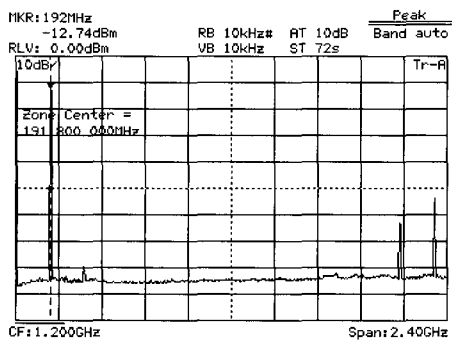**Fig. 7.**   Measured results of the LNA.

than -12 & -10dB return loss, 15.5 & 16dB NF, and +2 & 0dBm IIP3 for PCS-Korea and IMT-2000, respectively. Its measured NF is a little high, in our guess, due to the rigid resistor (R0) for input impedance
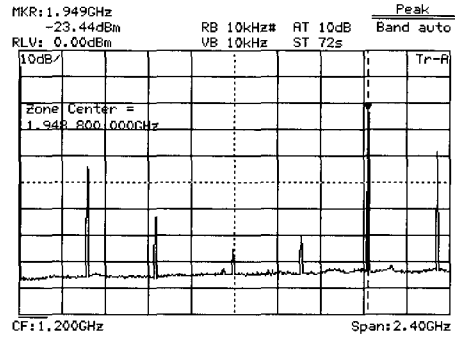
(a) One-tone harmonic test for PCS-Korea
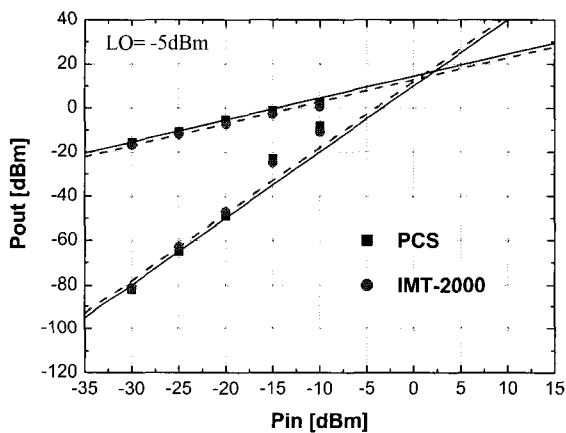(RF= -25dBm at 1.86GHz, LO= -5dBm at 1.64GHz)

(b) One-tone harmonic test for IMT-2000
(RF= -25dBm at 2.14GHz, LO= -5dBm at 2.33GHz)

(c) Two-tone imtermodulation test
(RF= 1.86GHz & 2.14GHz, LO= 1.64GHz & 2.33GHz)

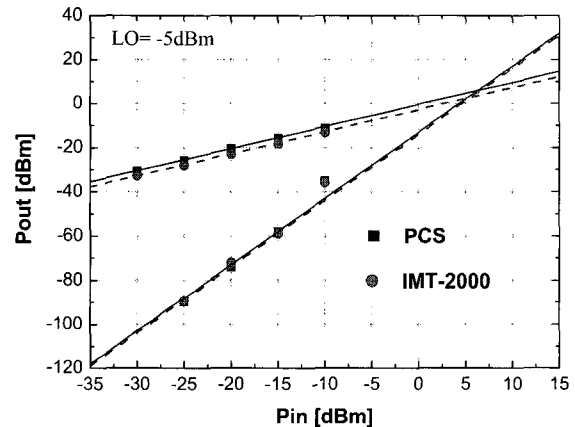**Fig. 8.** Measured results of the down-mixer.

(a) One-tone harmonic test for PCS-Korea
(IF= -20dBm at 130MHz, LO= -5dBm at 1.64GHz)

(b) One-tone harmonic test for IMT-2000
(IF= -20dBm at 380MHz, LO= -5dBm at 2.33GHz)

(c) Two-tone imtermodulation test
(IF= 130MHz & 380MHz, LO= 1.64GHz & 2.33GHz)

Fig. 9. Measured results of the up-mixer.

matching as shown in Fig. 3. And the up mixer has 0 & -2dB power conversion gain, less than -15 & -16dB return loss, and 6 & 3dBm OIP3 for PCS-Korea and IMT-2000, respectively. The overall power loss in down and up mixer measurement setup is assumed as about 1~2dBm. This value is very reasonable considering the losses of balun transformers and cables.

IV. CONCLUSION

We present the design and implementation of dual-band CMOS RF front-end transceiver ICs for PCS-Korea and IMT-2000 standards. Since the presented transceiver shares its building blocks in both the standards, it is as simple and small as possible. The

transceiver has been implemented in a standard 0.25μm CMOS technology. The receiver IC consists of a LNA and a down-mixer, and the transmitter IC integrates an up-mixer. With a single 3.0V power supply, the LNA, down-mixer and up-mixer consume 6mA, 30mA and 25mA, respectively. The overall measured performances are summarized in table 1.

TABLE 1.   Transceiver Performance Summary

| Technology	0.25um CMOS 1P5M		
Supply Voltage	3.0 V		
	PCS-Korea	IMT-2000	Unit
Receiver IC (LNA + Down Mixer : Idc = 36mA)			
LNA (Idc = 6mA)			
Gain	14	13	dB
Input IP3	+5	+4	dBm
Noise Figure	2.8	3.1	dB
In/Out return loss	-12 / -12	-14 / -12	dB
Reverse Isolation	30	30	dB
Down Mixer (Idc = 30mA)			
Conversion Gain	15	13	dB
Input IP3	+2	0	dBm
Noise Figure	15.5	16.0	dB
RF/LO return loss	-12 / -16	-10 / -18	dB
LO to RF/IF Isolation	35 / 30	30 / 30	dB
Transmitter IC (Up Mixer : Idc = 25mA)			
Conversion Gain	0	-2	dB
Output IP3	+6	+3	dBm
RF/LO return loss	-15 / -17	-16 / -20	dB
LO to RF/IF Isolation	30 / 35	25 / 35	dB
LO Leakage	-40	-35	dBm

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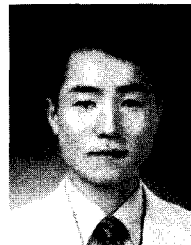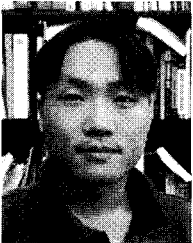
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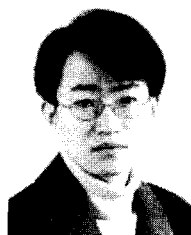
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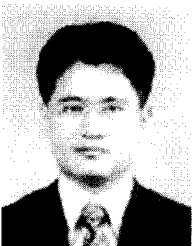
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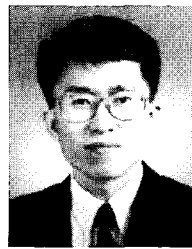
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He is a Senior Member of IEEE and a Principal Member of Engineering Staff in ETRI. He received Technology Outstanding Achievement Award from IEEK in 1999. He is the author and co-author of over 100 technical papers and 60 patents in the silicon RF devices and circuits design areas. His interests include device modeling, high speed and low power logic circuits, frequency synthesizer, and RF CMOS circuit design for multi-band single chip transceiver.