FeRAM Technology for System on a Chip

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Abstract — The ferroelectric RAM (FeRAM) has a great advantage for a system on a chip (SOC) and mobile product memory, since FeRAM not only supports non-volatility but also delivers a fast memory access similar to that of DRAM and SRAM. This work develops at three levels: 1) low voltage operation with boost voltage control of bitline and plateline, 2) reducing bitline capacitance with multiple divided sub cell array, and 3) increasing chip performance with write operation sharing both active and precharge time period. The key techniques are implemented on the proposed hierarchy bitline scheme with proposed hybrid-bitline and high voltage boost control. The test chip and simulation results show the performance of sub-1.5 voltage operation with single step pumping voltage and self-boost control in a cell array block of 1024 (64 x 16) rows and 64 columns.

Index Terms — *Ferroelectric memory, non-volittle memory, micro controller system, boost scheme.*

I. INTRODUCTION

DRAM, SRAM and other semiconductor memories are widely used for the processing and high speed storage of information in computers and other devices.

These memories are volatile, meaning that stored information is lost when the power is turned off. By comparison, EEPROM and Flash Memory have been introduced as non-volatile memories that store data as electrical charges in floating-gate electrode [1][2]. EEPROM and Flash Memory, however, take long time to write data, and have limits on the number of times that data can be rewritten. Therefore, it is tough for these types of memories to use in such systems as RAM, rewriting frequently.

But FeRAM has a good balance of RAM and ROM characteristics, making it ideal semiconductor memory.

In recent years, IC cards have come to be used in a variety of applications, including as ID cards, financial cards, and mass transit and toll collection cards, including e-commerce capability.

Currently, EEPROM is the primary memory device used to store data in IC cards, but FeRAM is superior to EEPROM in many respects, including a write speed about 10,000 times faster. In addition, FeRAM consumes 1/1,000th of the power for writing data, and its rewrite endurance is almost unlimited times.

The recent dramatic popularization of the Internet has focused attention on e-commerce, virtual shopping, virtual offices, and other web-based activities. Practical application of these concepts requires the use of security systems using public key encryption.

As a result, the FeRAM is expected to make a major contribution to achieving secure systems in the mobile terminals, digital home appliances, and smart cards in the future.

Moreover, the integration of FeRAM and CPU in a chip makes it possible to create an extremely secure system, allowing data encryption for e-commerce transactions over the Internet, as well as personal authentication through public keys.

The incorporation of large density FeRAM makes it

possible to carry out multiple applications and store large amounts of data, and makes it ideal for use in multi-functional IC cards in the burgeoning broadband Internet era [3][4].

The process technology of FeRAM has been improved by enhancing the performance characteristics of ferroelectric material crystals and electrodes and developing a protective layer to eliminate the ferroelctric degradation during manufacturing process. FeRAM device process has been constructed by simply adding a ferroelectric capacitor fabrication process to the standard logic CMOS process. This method enabled FeRAM and logic CMOS to be easily combined at low cost.

The reliability of FeRAM tends to be dependent on the level of polarization, and as time elapses, the polarization charge decreases. This characteristic is greatly affected by materials. From a design standpoint, this characteristic can be improved by increasing the write voltage to the ferroelectric capacitor.

Thus writing with an insufficient power supply voltage may cause a reduction of sensing margin and reliability. The proposed boost voltage control of both bitline (BL) and plateline (PL) in hierarchy BL scheme is worked well at low power supply voltage (VCC). The proposed hierarchy BL scheme with multiple divided sub-cell arrays reduces BL capacitance without decreasing cell array block size with high cell array efficiency. In conventional method, data 0 is written in the first period and data 1 is written in the second period to memory cell during precharge time period. Thus the conventional write operation uses two time intervals in precharge time period. The proposed write operation shares both active and prechrge time period and thus increases chip performance with short precharge time.

In conventional folded BL, the cell sensing and reference BL are paired in a same cell array block, thus the reference level is unstable by coupling noise with neighbor cell data sensing voltage of large cell data distribution. In proposed hybrid BL architecture, reference BL is composed from neighbor cell array block like open BL structure, with the controlling of switch devices. Thus the reference level is free from the coupling noise, and each cell data sensing voltage is also protected from coupling noise by unused neighbor BL.

The inter-BL cross-talk noise levels of sub-BL (SBL) and main-BL (MBL) are increased without shielding

layer in more scaled memory cell, but the proposed BL structure can overcome the scaling problem of future FeRAM. The test chip of 256kb is constructed with hybrid BL sensing scheme.

II. OVERVIEW OF MICRO-CONTROLLER SYSTEM

Fig. 1 shows the pin configuration on package type of 40-PDIP in an 8-bit micro-controller system (MCS-52) family. Fig. 2 shows the chip layout the MCS-52 family. Fig. 3 shows the conventional block diagram of MCS-52.

SRAM and Flash memories are used for data memory and program memory respectively.

The memory sizes of SRAM and Flash are 256 bytes and 8K bytes respectively. The machine cycle of micro-controller core circuit operates at 1/12 of the frequency of 40 MHz.
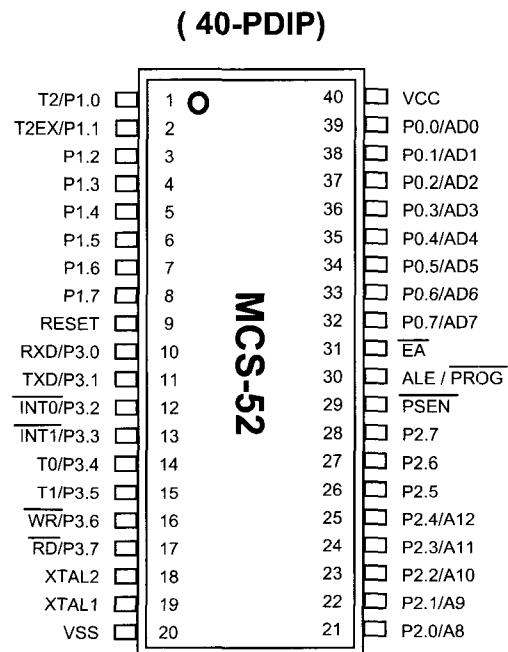
(40-PDIP)

Fig. 1.   40-PDIP pin configuration of MCS-52.

Micro-controllers incorporating Flash Memory as non-volatile memory have been developed. However, for erasing and writing, these micro-controllers requires the power from an external source or internally boosting scheme.
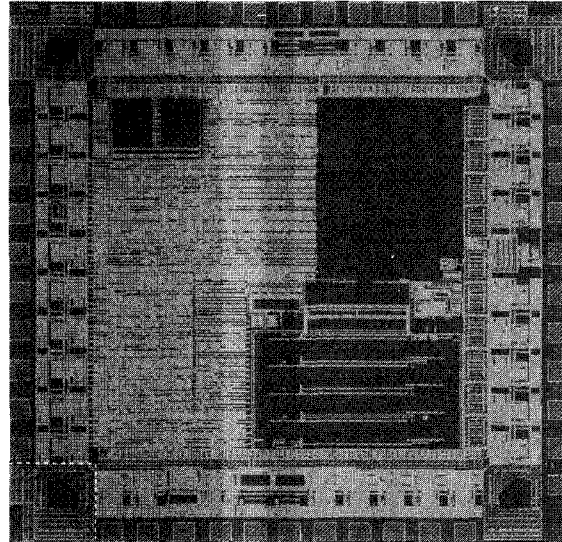
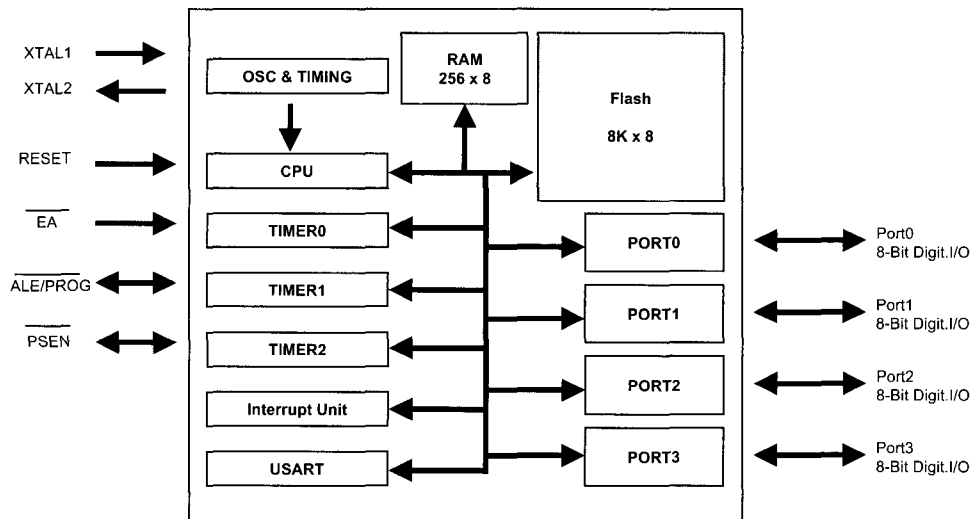Fig. 2.   The chip layout of MCS-52.

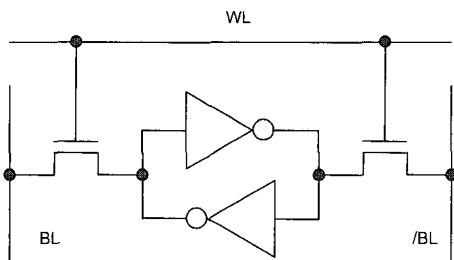
Fig. 3.   The conventional block diagram of MCS-52.

Fig. 4.   The SRAM cell structure.

This causes power consumption to increase and results in longer erase and write times, making this type of micro-controller impractical as a RAM device for writing data in real time.

The SRAM cell is composed of 6-transistors (6-T) with the data latch devices and selection switch devices as shown in fig. 4. The read and write mode is controlled by WEB signal as shown in fig. 5. The SRAM cell operation is stable and fast but the large cell size is a critical weak point with cost issues.

The circuits of Flash memory are characterized by the block circuits of high voltage generation, read, write and erase from the block diagram in fig. 6.

After power up, during the programming (PGM) mode, the write pulses of /PROG for each bits or bytes are
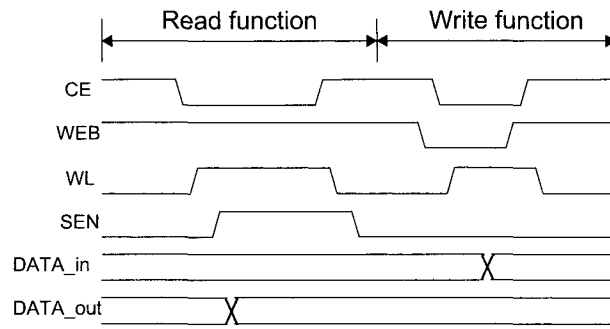
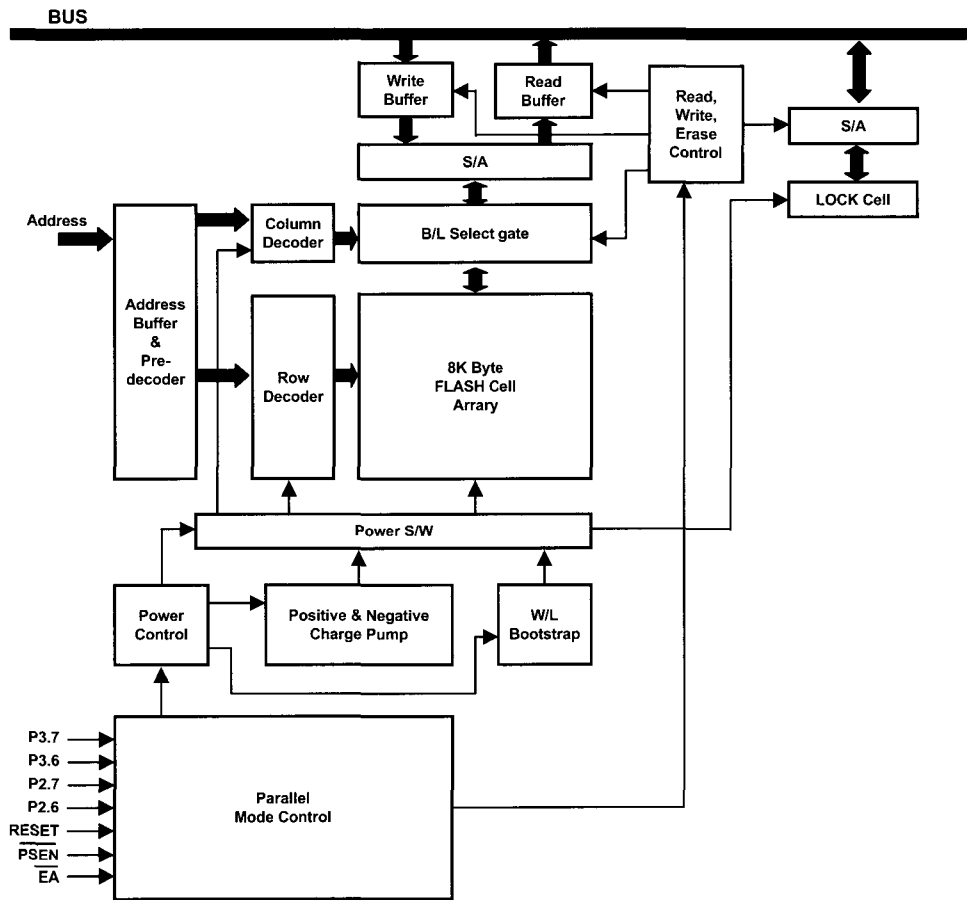**Fig. 5.** The SRAM read and write timing diagram.

Fig. 6. The block diagram of Flash memory.

repeated for a certain number of times with the long write period as shown in fig. 7. Because write operation of Flash memory is mainly by injecting hot electrons or using the tunnel effect at float gate, write speed is slower by about 1,000 times or more than that of FeRAM.

Only read speed of Flash memory is the same level with that of FeRAM.

Besides write power dissipation of Flash memory is relatively large with boost pumping circuit and long write time by about 1,000 times than that of FeRAM.

The fig. 8 shows the cross-sectional view of Flash memory and the cell operation condition on the read mode of Flash cell array in a sub-block. In a sub-block of Flash cell array, the PW and Deep N-Well is commonly connected and same voltage biased. The bias condition of read mode of the Flash cell is described in the below table.
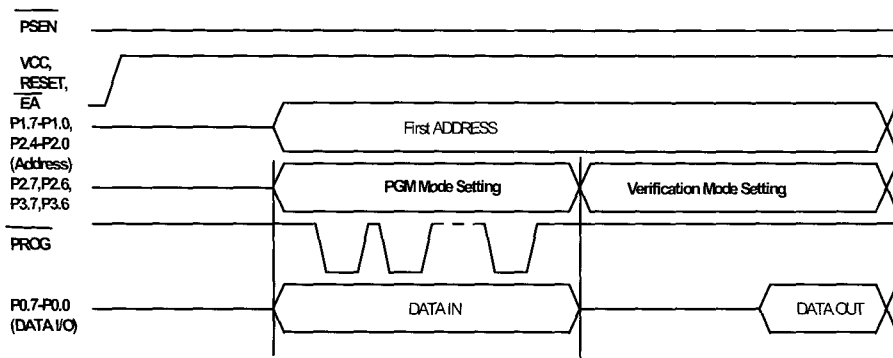
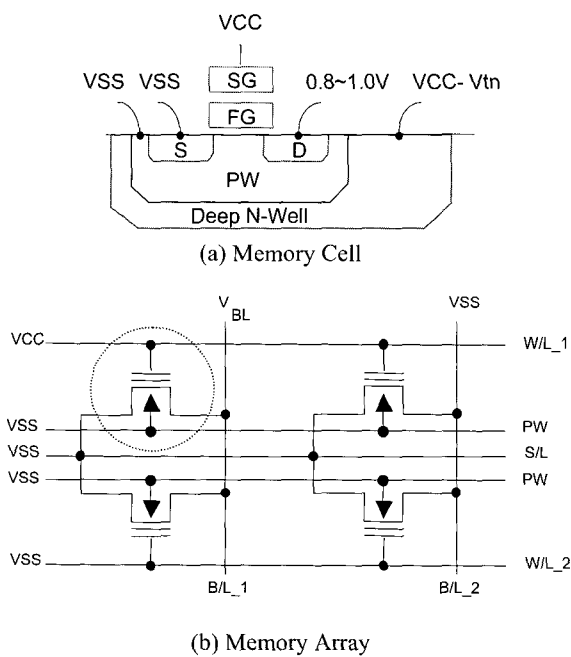**Fig. 7.** The write and verify timing diagram of Flash memory.

(a) Memory Cell

(b) Memory Array

Fig. 8. The read mode condition of Flash memory.

Node	Voltage@	Read Condition
SG	Vsg	5 V
D	Vd	0.8 V
S	Vs	0 V
SUB	Vsub	0 V

(a) Memory Cell

(b) Memory Array

Fig. 9. The write mode condition of Flash memory.

Node	Voltage@	Write Condition
SG	Vsg	9 V
D	Vd	5 V
S	Vs	0 V
SUB	Vsub	0 V

The figure 9 shows the cell cross-sectional view of Flash memory and the cell operation condition on the write mode of Flash cell array in a sub-block. And the programming is executed by injecting hot electrons to FG by the current flow between drain and source node. The bias condition of write mode of the Flash cell is described in the below table.
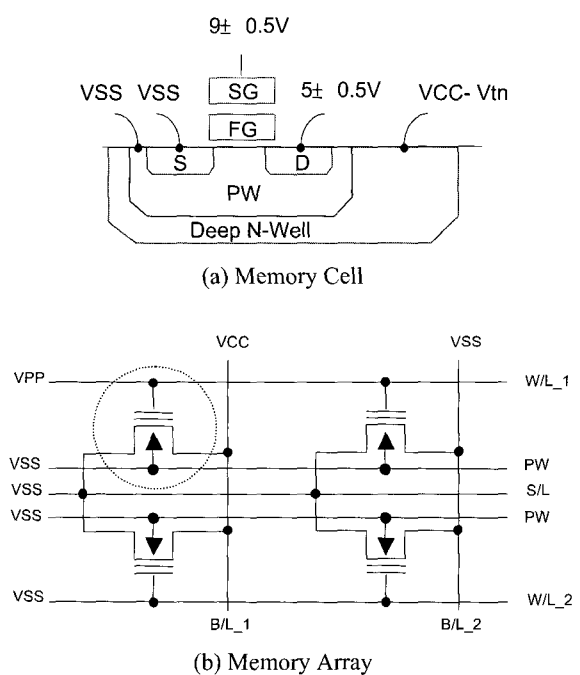
The fig. 10 shows the cross-sectional view of Flash memory and the cell operation condition on the erase mode of Flash cell array in a sub-block. And the erase is executed by discharging electrons of FG by using the tunnel effect at float gate oxide. The bias condition of erase mode of the Flash cell is described in the below
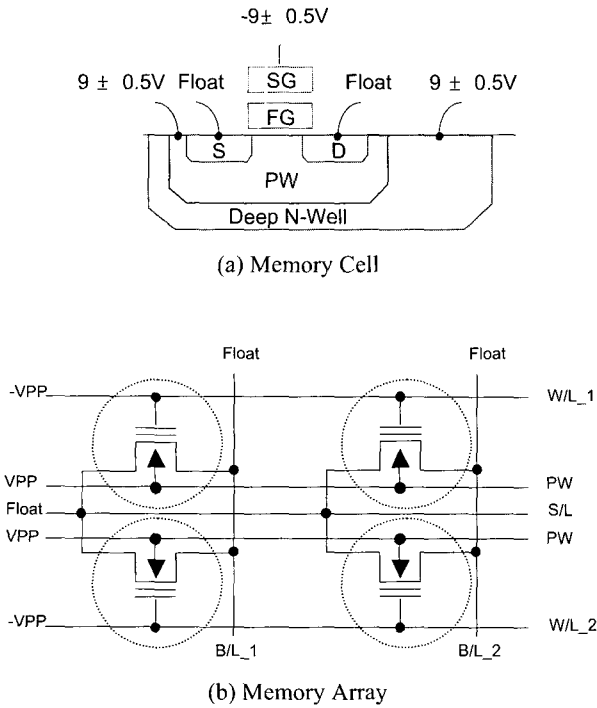
table.

(a) Memory Cell

(b) Memory Array

Fig. 10. The erase mode condition of Flash memory.

Node	Voltage@	Write Condition
SG	Vsg	-9 V
D	Vd	float
S	Vs	float
SUB	Vsub	9 V

III. FeRAM Technology in Micro-Controller System

Fig. 11 shows the proposed block diagram of the embedded FeRAM on micro-controller system. SRAM and FeRAM memories are used for data memory and program memory respectively. The memory sizes of SRAM and FeRAM are 256 bytes and 8K bytes respectively. The machine cycle of micro-controller core circuit operates at 1/12 of the frequency of 40 MHz.

Fig. 12 shows the timing diagram of embedded FeRAM system. The signal of CE is for the control of memory block operation of embedded FeRAM. The signal of SEN is for the control of cell data sensing and amplifying of embedded FeRAM. The signal of DOUT

is for the control of output latch of embedded FeRAM

Fig. 13 shows the read and write timing diagram of FeRAM. The read and write operation time is same and well cooperates with system machine cycle in real time.

The embedded FeRAM on micro-controller system guarantees writing with high speed in real time, lower power consumption, and unlimited write cycle compared to Flash memory. The embedded FeRAM is the unique total solution with the function for data and program memories.

The embedded FeRAM is seen as an ideal memory for a high performance SOC.

The process compatibility of FeRAM with logic CMOS process will be the first step in realizing a high performance SOC.

Fig. 14 shows the conventional memory mapping method of the external data and program memories on micro-controller system. The data memory is controlled by /WE and /RD. The program memory is controlled by /PSEN. Each memory mapping addresses are located at the same spaces, but the each control signals of /WE, /RD and /PSEN are independent.

Fig. 15 shows the proposed memory mapping method of the external data and program memories with a FeRAM memory. The write mode of data memory space is controlled by /WE. The read mode of data and program spaces is controlled by /RD and /PSEN.

The only one type of FeRAM memory is merged for data and program memories without another memory types.

Fig. 16 shows the read timing diagram of external program memory. Figure 17 and 18 shows the read and write timing diagram of external data memory.

The FeRAM memory uses the timing diagram of SRAM for read and write mode and Flash for read mode.

IV. FeRAM Technology in Stand-Alone Memory

Like a DRAM cell, the unit FeRAM cell structure comprises a transistor (1T) to access a stored data and a capacitance (1C) to store data as shown in figure 19. However, different from DRAM, which uses such paraelectric oxide layer as silicon oxidized film or silicon nitride film for the storage capacitance, the FeRAM structure uses ferroelectric material. As a result,
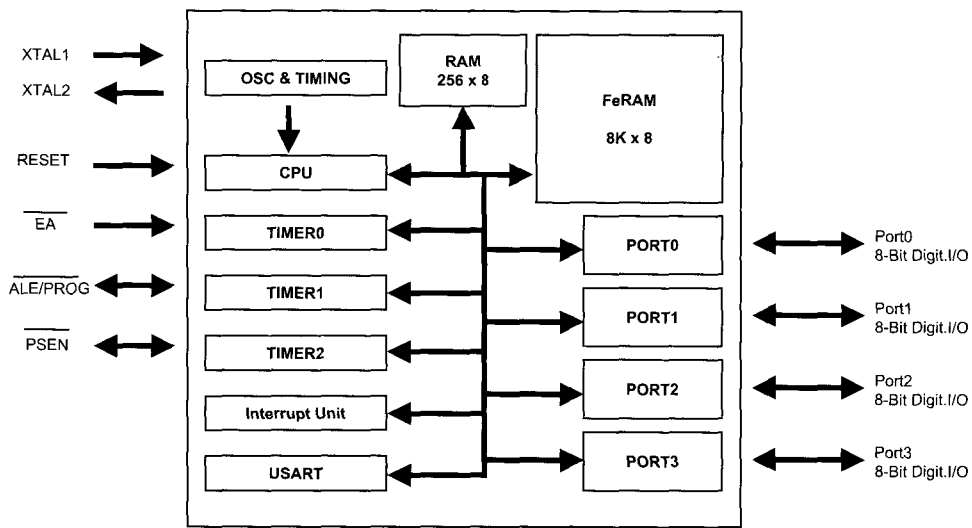
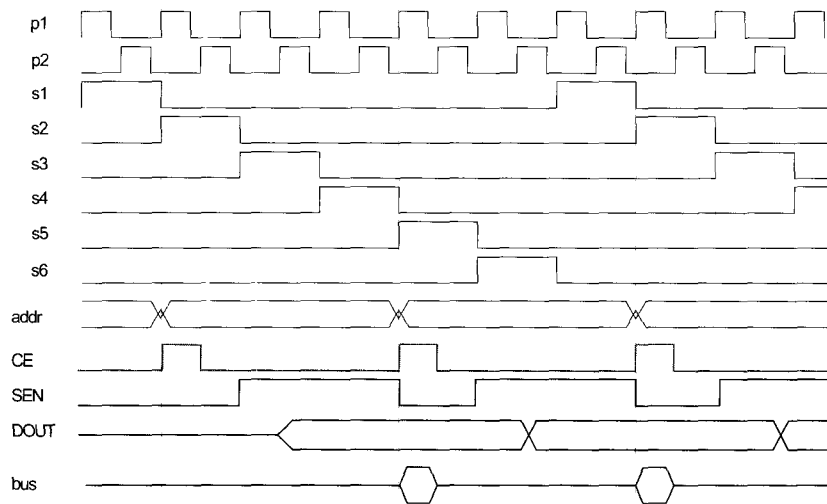**Fig. 11.**   The proposed block diagram of MCS-52.

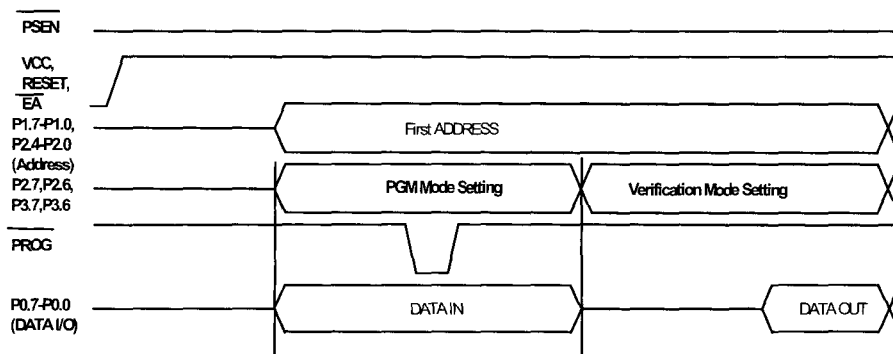**Fig. 12.**   The timing diagram of Embedded FeRAM system.

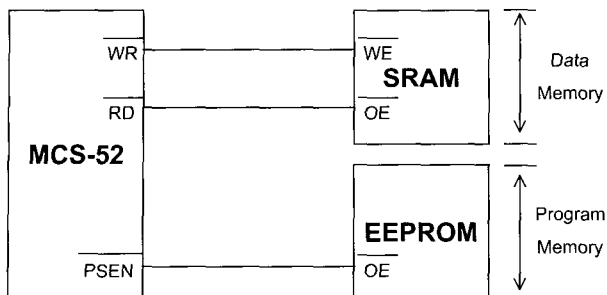**Fig. 13.**   The write and read timing diagram of FeRAM.

Fig. 14. The conventional memory mapping method of external memories.
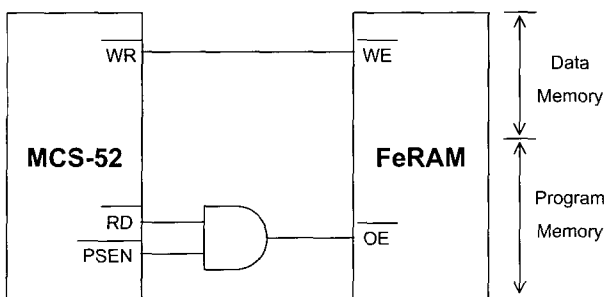
RD	PSEN	FeRAM
L	H	Data Memory
H	L	Program Memory
H	H	No Operation

Fig. 15. The proposed memory mapping method of FeRAM memory.
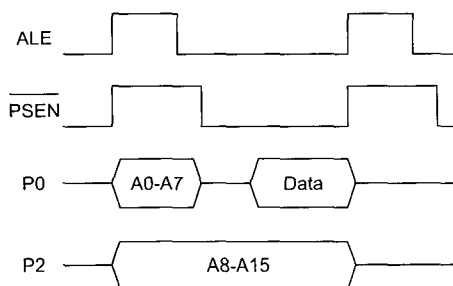

Fig. 16. The read timing diagram of external program memory.
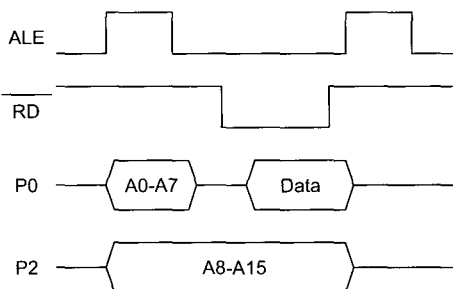

Fig. 17. The read timing diagram of external data memory.
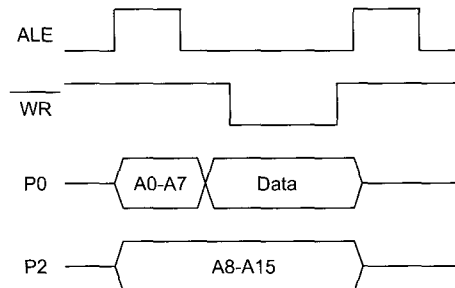

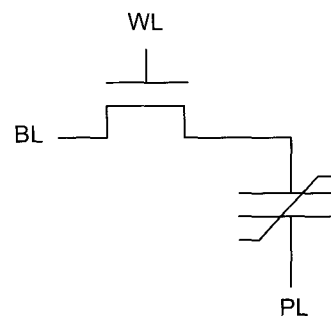Fig. 18. The write timing diagram of external data memory.

Fig. 19. The unit cell of FeRAM.

FeRAM technologies are similar to DRAM cell technologies, and the two technologies can be cooperated relatively easily.

Cell stored data is detected by reading the charges in polarization capacitor when a voltage is applied to the PL.

The ferroelectric film on the memory cell capacitor is made of PZT (Pb(Zr, Ti)O3), SBT (SrBi2Ta2O9), or BLT ($Bi_{4-x}La_xTi_3O_{12}$) permitting high storage density. Also, write operation of FeRAM is controlled by the electrical polarization of ferroelectric capacitor by applying the electric field, compared to writing by injecting hot electrons, as is done on Flash Memory.

PZT is chemically expressed as ABO3, with an octahedron constructed by six oxygen atoms including a smaller metallic element near their center. PZT has high remnant polarization values of 2Pr. SBT or BLT, has a low Ec, enables an operating low voltage by making the film thinner, and exhibits little fatigue even after polarization has been reversed more than 10E12 times. Consequently, PZT or BLT is seen as a promising material for highly integrated FeRAM, which requires low voltage operation.

The electrical property of remnant polarization is propotional with the operation voltage in linear region

and saturated at over the 3.0V in saturation region as shown in fig. 20. Under the 3.0V, the remnant charge of ferroelectric capacitor is largely dependent to the applied voltage to it and from which, multi-bit storage operation of ferroelectric cell is possible.
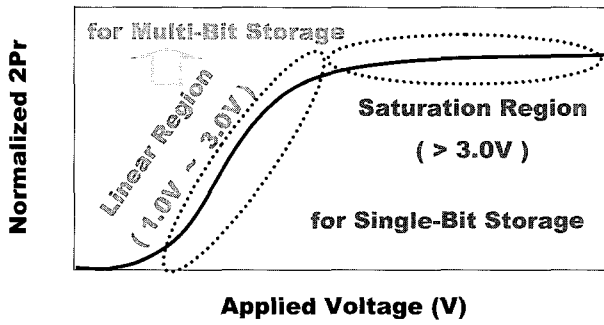

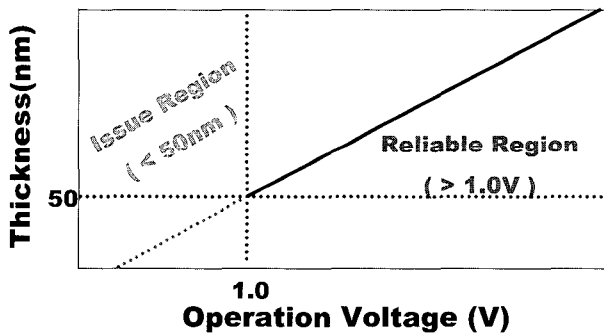**Fig. 20.** The polarization characteristics of ferroelectric capacitor.

Fig. 21. The thickness characteristics of ferroelectric capacitor.

The voltage level for the saturation of remnant charge is dependent on the thickness of ferroelectric capacitor as shown in fig. 21.

The cell operation voltage of FeRAM can be reduced to low voltage level by decreasing the thickness of ferroelectric film, but that will be confronted to the reliability issues. The thickness of ferroelectric film with less than 50nm will cause unreliable properties in ferroelectric capacitor. The method of decreasing the thickness for low voltage operation is not adequate solution.

The Ferroelectric capacitor of test chip is composed of electrodes material with platinum and ferroelectric material with BLT of the thickness of 70nm as shown in fig. 22, which is annealed at temperature of 650°C.

The write operation of FeRAM memory starts at high edge slope of chip selection (CSB) signal from write

operation specification in data book of FeRAM as shown in figure 23. In the conventional method, data 0 is written in period C1 and data 1 is written in period C2 to memory cell during precharge time period. Thus the conventional write operation uses two time intervals of C1 and C2 in precharge time period. The proposed write operation changes to share both active and prechrge time period and thus increases chip performance with short precharge time.
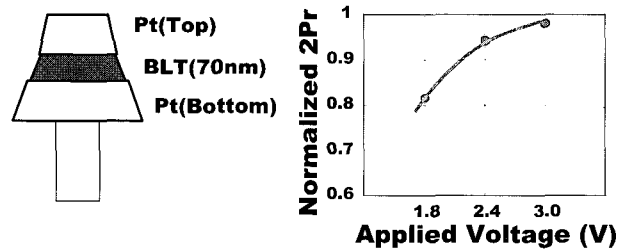

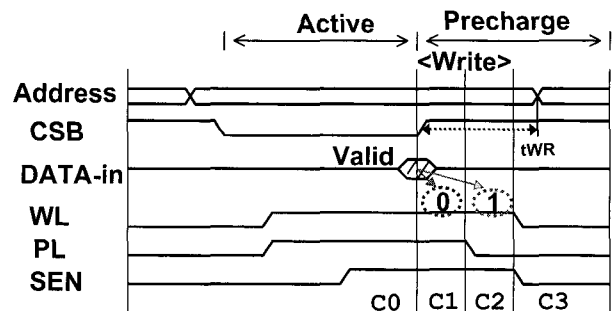**Fig. 22.** The polarization characteristics of BLT capacitor.

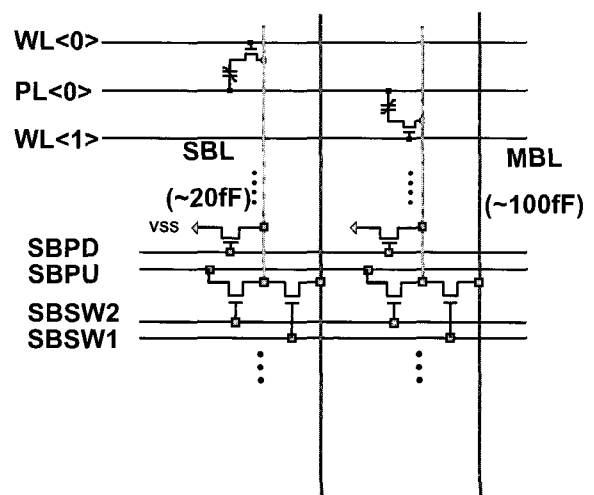**Fig. 23.** The conventional write operation of FeRAM.

Fig. 24. The proposed hierarchy bitline scheme.

An insufficient write voltage of FeRAM cell at a low

power supply voltage may cause a reduction of sensing margin and reliability. The proposed boost voltage control of both bitline and plateline in hierarchy bitline scheme is worked well for sufficient operation voltage of FeRAM cell as shown in fig. 24.

The cell array block is composed of multiple sub cell array blocks with folded bitline structure. To reduce capacitance of SBL, each cell array of SBL is limited to 64 rows. The main bitline is electrically coupled to one of 16 SBLs at a time. The sense amplifier (SA) and column selection (CS) devices are consisted through MBL, and two MBLs share the same SA at the middle of cell array block. The switch devices for controlling of SBL and MBL are constructed with three NMOS transistors. The control signals of SBL and MBL are composed of SBSW1, SBSW2, SBPU and SBPD. The SBSW1 controls data flow between the SBL and MBL. The SBSW2 controls the signal transfer between the SBL and SBPU signals. The SBPU is used for providing the high boost voltage signal to SBL from single step pumping voltage (VPP). The SBPD is used for pull-down control of SBL to zero level (VSS) in precharge time period. The each capacitance values of SBL, MBL and SA are about 20fF, 100fF and 20fF in cell array of 1024 rows (64rows x 16).
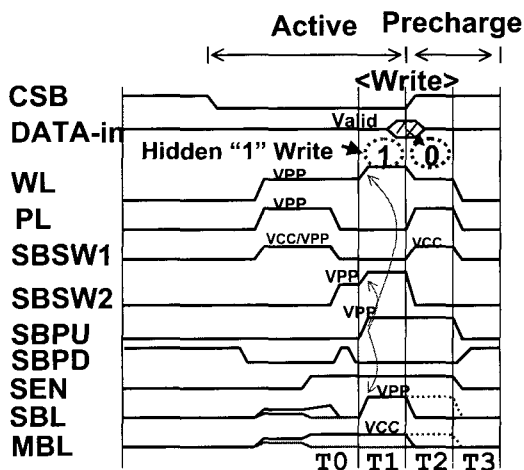

Fig. 25. The proposed timing diagram of hierarchy bitline scheme.

Fig. 25 shows proposed timing diagram of hierarchy bitline scheme.

The major change of new operation scheme is the introduction of hidden 1-write in the active period,

regardless external data-in is valid or not.

And in the precharge period, the time interval of data 0-write only is needed. The precharge time period is reduced to short time range with one time period.

In active time period of T0, SBL and MBL are coupled by activation to VCC level of SBSW1 signal. The WL and PL signals are activated to VPP level. The sensing voltage of SBL is transferred to MBL as shown in figure 26.
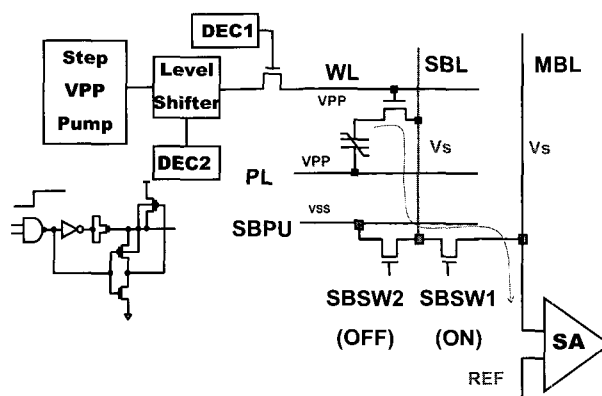

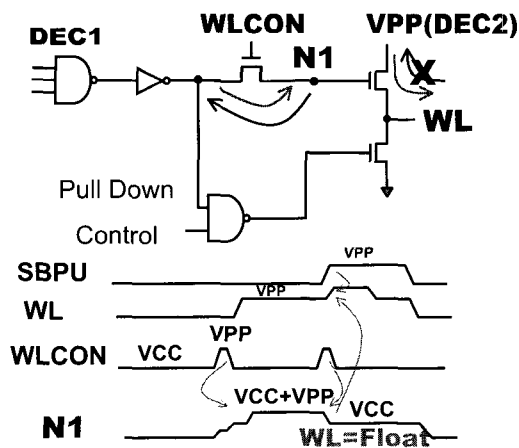**Fig. 26.** The sensing operation details of hierarchy bitline scheme.

Fig. 27. The boost and float control details of hierarchy bitline scheme.

One of requirements of competitive FeRAM should be low power consumption.

The power consumption at proposed scheme is low by the single step pumping method for VPP generation.

For the float state of WL and SBSW2 signals, we uses the proposed control scheme as shown in fig. 27.

The signals of WL and SBSW2 drivers are composed

of DEC1, DEC2, pull down and WLCON signals.

By controlling of WLCON signal, the voltage of node N1 is controlled. At first WLCON pulse of VPP level, the voltage of N1 is changed to VCC level. And the voltage of N1 is self-boosted to VCC+VPP by conducting the DEC2 signals of VPP level to WL

At second WLCON pulse of VPP level, the voltage of N1 is changed to VCC level again. Then the state of WL is float at VPP level.

After sense amplifier is activated, SBSW1 and PL signals are pulled down to VSS level. The SBSW2 signal is switched to VPP level. Before T1 period, the NMOS switch devices of drivers of WL and SBSW2 signals are turned off. The two nodes of WL and SBSW2 signals are changed to float state at VPP level.
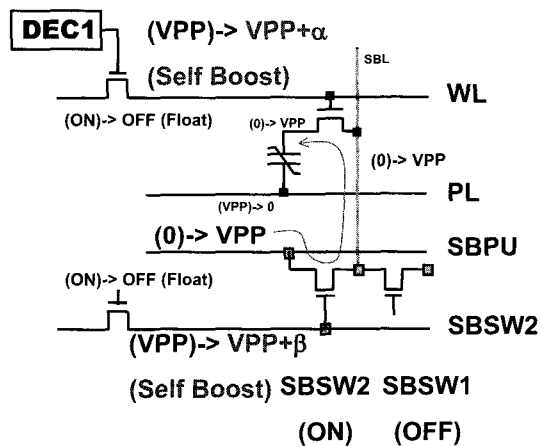

Fig. 28.   The 1-write details of hierarchy bitline scheme.

In T1 period, SBPU signal is switched to VPP level as shown in fig. 28. Then two nodes of WL and SBSW2 signals are boosted to double VPP levels of VPP+α(~VPP) and VPP+β(~VPP) by self-boost operation of each NMOS devices. For example, the VPP level of 2.5V is induced from the VCC level of 1.5V. And the self-boost voltage level of 4.5V with double VPP level or quasi-quadruple VCC level is induced from VPP level of 2.5V. By self-boost voltage level of 4.5V, VPP level of SBPU can be transferred to SBL and storage node of memory cell.

Thus data 1 at SBL is written without voltage drop with VPP level in T1 period.

In T2 period, SBSW2 signal is switched off to VSS level. The SBSW1 and PL signals are switched to high voltage of VCC and VPP level for data 0-write operation

as shown in figure 29. Due to SBSW1 signal of VCC level, VPP level at SBL is maintained from different voltage level with VCC level at MBL, but VSS level at MBL can flow to SBL in data 0-write operation. In proposed write operation, data 1 is written to all selected cells regardless of sense amplifier operation in active time period of T1, on the other hand, data 0 is written to the target cells in precharge time period of T2. The proposed write operation shares two time periods of T1 and T2 in both active and precharge period. Thus level of precharge time period can be reduced to less than 20ns at VCC level of 3.0V.
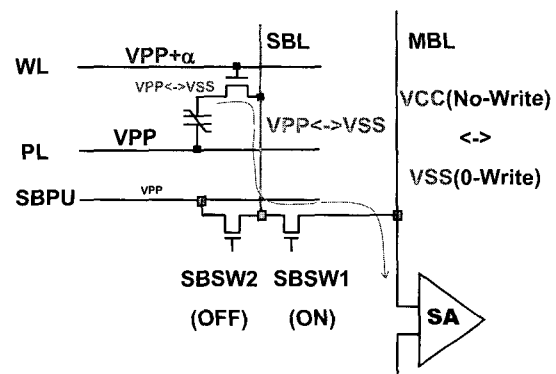

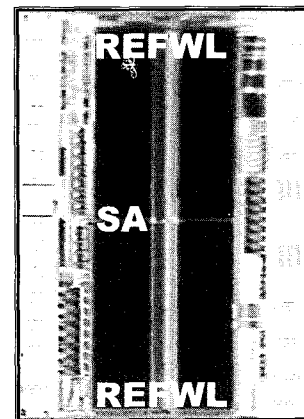Fig. 29.   The 0-write details of hierarchy bitline scheme.

Fig. 30.   The die photography of test chip.

The test chip for hybrid BL is composed of SA at the middle of cell array and the reference control switches at both edge region of cell array as show in fig. 30.

Fig. 31 shows the block diagram of hybrid BL architecture, which is combination of the folded and open scheme. Each cell arrays are composed of folded cell array, and sensing method is composed of open BL
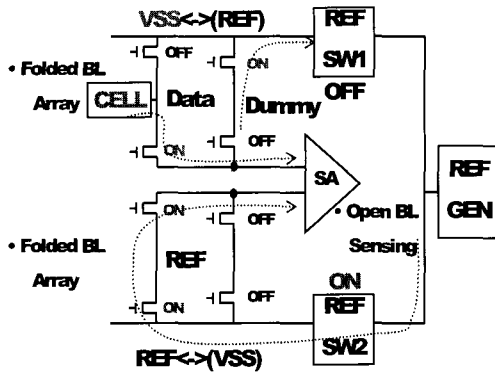
scheme.

Fig. 31. The operation details of hybrid bitline.

In conventional folded BL, the cell sensing and reference BL are paired in a same cell array block, thus the reference level is unstable by coupling noise with neighbor cell data sensing voltage of large cell data distribution. In proposed hybrid BL architecture, reference BL is composed from neighbor cell array block like open BL structure, with the controlling of switch devices. Thus the reference level is free from the coupling noise, and each cell data sensing voltage is also protected from coupling noise by the shielding effect of unused neighbor BL.
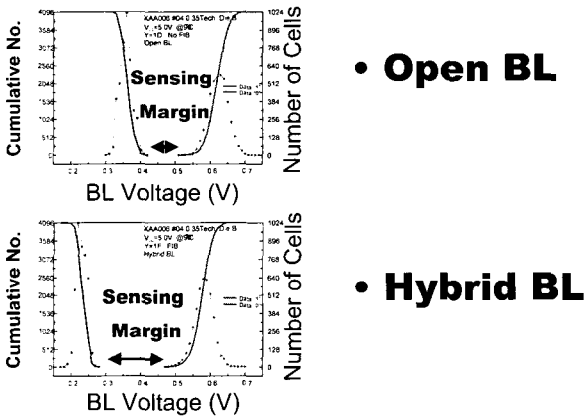

Fig. 32. The cell data distribution of hybrid bitline.

Fig. 32 shows the comparison of cell data distribution between the conventional open BL and the proposed hybrid BL architecture. By the cross-talk noise, the conventional open BL reduces much bitline sensing voltage. The large cell data distribution will cause severe cross-talk noise in FeRAM.

The fig. 33 shows the comparison results of retention

property between the conventional open BL and the proposed hybrid BL, in which the retention life-time is extended to about 10 years with hybrid BL from about 30 hours with open BL at 125°C.
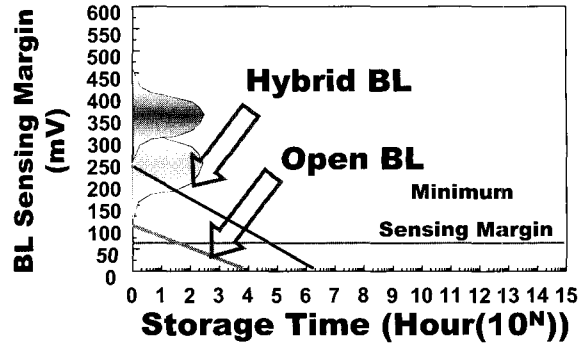

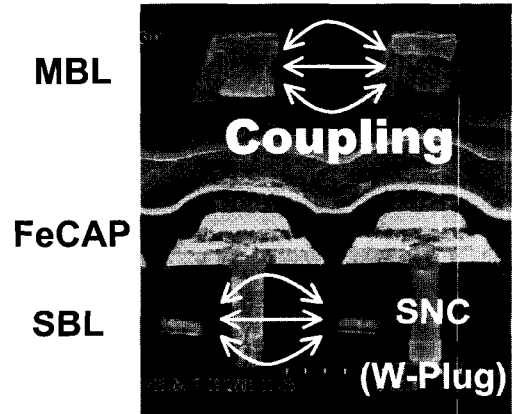Fig. 33. The reliability estimation of hybrid bitline.

Fig. 34. The ferroelectric capacitor under MBL.

The ferroelectric capacitor under MBL structure is shown in fig. 34. The cross-talk noise level at MBL is more than 15% per a side without shielding layer. But the cross-talk noise level at SBL is less than 4% per a side with shielding layer in tungsten plug of SNC.

The ferroelectric capacitor over MBL structure is shown in fig. 35. The cross-talk noise levels at MBL and SBL are less than 2% and 5% per a side with shielding layer in tungsten plug of SNC at 0.25μm technology. The inter-BL cross-talk noise levels of SBL and MBL are increased without shielding layer in more scaled memory cell, but the proposed BL structure can overcome the scaling problem of future FeRAM.

In sub-1.0 voltage range at VCC level of 0.8V, VPP level of 1.4V is transferred to SBL and storage node of memory cell without voltage drop from simulation
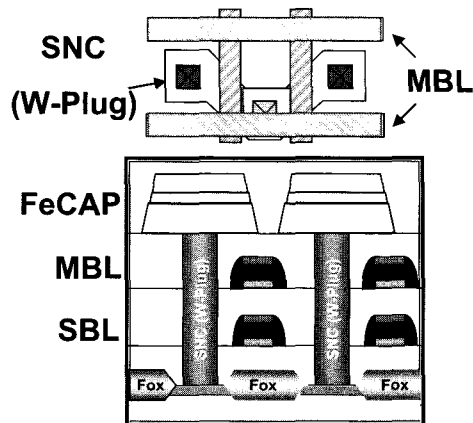
results as shown in fig. 36.
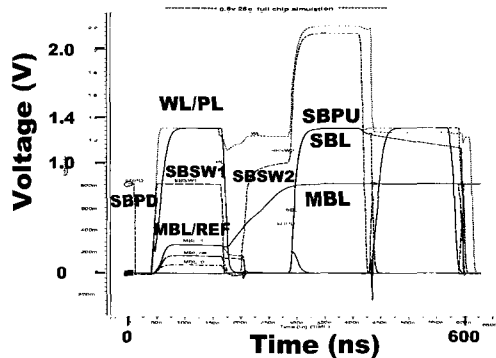

Fig. 35. The ferroelectric capacitor over MBL.

Fig. 36. The operation waveforms at 0.8V.

V. Conclusions

Ferroelectric capacitor of Pt/BLT/Pt with 70nm sol-gel BLT at anneal temperature of 650°C has low coercive voltage of 0.5V. The memory cell and capacitor size are $1.5\mu m^2$ and $0.8\mu m^2$ with 1-poly/2-tungsten and 2-metal process in $0.25\mu m$ design rule. SBL and MBL are formed with 2-w layers under the ferroelectric capacitor. The life-time reliability of the proposed hybrid BL improved to more than 10 years in comparison from 30 hours of conventional open BL at 125°C. The access and precharge time of test chip are estimated to 180ns and 70ns at supply voltage of 1.5V from internal probing results. The precharge time is almost half level in compared to conventional one. In sub-1.0 voltage range at VCC level of 0.8V, VPP level of 1.4V is transferred to

SBL and storage node of memory cell without voltage drop from simulation results.

The test chip and simulation results show the performance of 0.8V ~1.5V operation with single step pumping voltage and self-boost control with the hierarchy BL.

REFERENCES

[1] B. Ricco, G. Torelli, M. Lanzoni, A. Manstretta, H. Maes, D. Montanari, and A. Modelli, "Nonvolatile mutilevel memories for digital applications," Proc. IEEE, vol. 86, pp. 2399-2421, Dec. 1998.

[2] P. Pavan, R. Bez, P. Olivi, and E. Zanoni, "Flash memory cells – An overview," Proc. IEEE, vol. 85, pp. 1248-1271, Aug. 1997.

[3] R.E. Jones Jr., "Ferroelectric nonvolatile memories for embedded application," in Proc. IEEE Custom Integrated Circuits Conf., 1998, pp. 431-438.

[4] T.Miwa, J. Yamada, Y. Okamoto, H. Koike, H. Toyoshima, H. hada, et al., "An embedded FeRAM macro cell for a smart card microcontroller," in Proc. IEEE Custom Integrated Circuits Conf., 1998, pp. 439-442.

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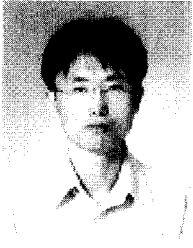
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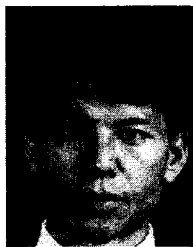
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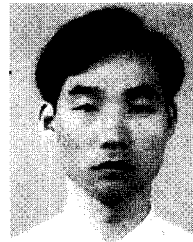
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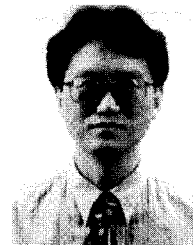
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