A Method for Measurement of Limiting Intrinsic Non-Uniformity Due to Process in CCD-Multiplexers for Focal Plane Arrays

R. K. Bhan and R. S. Saxena

Abstract— **We present a simple experimental method for determination of limiting intrinsic fixed-pattern non-uniformity (NU) due to fabrication process in two-dimensional CCD multiplexers (MUXs) that are used for hybrid focal plane arrays. Here, this is done by determining separately the two NUs viz. that are V_T dependent and V_T independent. From these measurements, process dependent NU can be extracted. It is argued that V_T dependent NU can be eliminated by designing novel input circuits whereas V_T independent NU, primarily, dependent on process control and material variations may be reduced but cannot be eliminated completely and hence limits the FPA performance eventually.**

Index Terms —**Interconnects, Doplanar strip line, Fourier series approach, silicon substrate, point matching procedure.**

I. INTRODUCTION

Advanced infrared (IR) thermal imaging systems use two-dimensional Focal Plane Arrays (FPAs). In hybrid configuration, these FPAs consist of IR sensitive detector arrays hybridized with Si-based readout circuits (ROICs), using advanced interconnect indium-bump technology. However, these FPAs suffer from the problem of fixed-pattern-noise (FPN), i.e., pixel-to-pixel variation in detector's response even for the constant IR flux incident on the array [1]. Contributions to this FPN, as regards detector material, arise due to its composition, doping, lifetime variations etc. The NU in the detector array is the maximum contributor to the total FPN of the FPA. In addition, there are process variations, and also the variations caused by optical arrangements used to collect the IR photons coming from the scene [2]. However, as regards Si-readout circuit, it also contributes, although least, to this FPN. One of the stringent requirements of a readout circuit is that it should introduce minimum NU in the process of readout because non-uniformities contributed by the detector array are already a problem. However, there is a certain minimum NU dictated by material and fabrication process variations across the multiplexer array that cannot be completely eliminated called 'intrinsic non-uniformity' in this paper. This intrinsic NU should be at least less than one-tenth of the total NU due to detector and other sources. If it is not controlled and minimized, it can be a significant contributor to an otherwise uniform detector array. Hence it should be routinely measured and controlled.

The readout circuits presently in use are either CMOS or CCD Si-based multiplexers. The choice of multiplexer depends on the type of application [3]. Here we shall report the results of an experimental method on CCD MUX used as ROIC for determination of this NU. However, the concept can be implemented in CMOS ROICs as well by novel design of proper input structure. The method, uses peak to peak measurements of NU, for determination of this NU due to processing variations,

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Dr. R. K. Bhan Scientist-E Soild State Physics Laboratory, Lucknow Rod, Delhi-110054.
(e-mail : bhan/sspl@ssplnet.org)

by determining separately the two NUs viz. that are V_T dependent and V_T independent.

II. EXPERIMENTS

The devices used in this study were 100 x 100 shallow buried channel CCD multiplexers. Briefly, the process consists of fabricating CCD MUXs on p-type Si wafers using double poly double metal process. Gate oxide thickness was about 1100 Å and buried channel depth was about 1 μm. The devices were two-phase CCDs using implanted well for store/barrier formation. The MUX consists of 50 vertical shift registers (VSRs) and a horizontal shift register (HSR). Figure 1 shows the photograph of the portion of the chip showing eight vertical shift registers (VSRs), one horizontal shift register (HSR) and an on-chip amplifier. At each pixel site there is an input structure used for coupling the detector output to CCD MUX. Furthermore, an on chip charge detection circuit was floating diffusion preceded by an output gate. The floating diffusion was followed by a double stage cascaded source follower (DSF) wherein the load resistor of second stage was connected externally. The DSF had a gain of about 0.6 at room temperature and responsivity of 0.37 mV/e. In addition to this, there were numerous test structures and pads for testing HSR and VSRs independently.

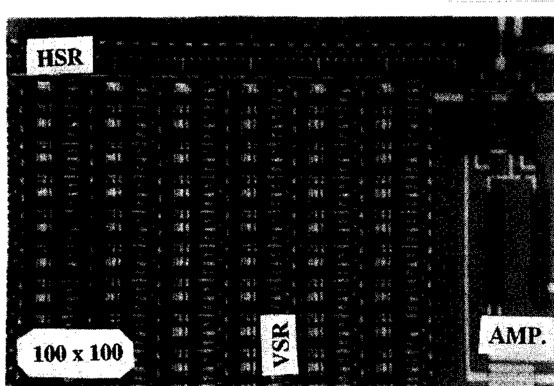


Fig. 1. The photograph of portion of the 100x100 CCD MUX chip showing six vertical registers (VSR), one horizontal register(HSR) and an on-chip amplifier.

The clocks and DC voltages required to run the devices were programmed on dedicated drive electronics developed in-house. The timing of the clocks was programmed on IBM PC and transferred in binary format to the RAM of the dedicated hardware that was clocked repeatedly to give continuous clocks at TTL level. Further, TTL clocks were fed to MOS driver circuit for appropriate clock levels for driving various CCD MUX pins. The other pins not in use during the MUX testing were kept isolated electrically by keeping them 'OFF' i.e. kept at substrate potential if it is a gate or 15 Volts reverse biased if it is diode.

III. EXPERIMENTS

The principle of the present method is demonstrated using the 'direct injection scheme', which is a commonly used input structure in CCD MUXs [4-6]. However, the method can be applied to other circuits as well by inclusion of an additional gate as a test pin. Figure 2 shows the type of input structure used in the present study. This structure consists of input gate (IG) for transfer and control of photo-generated charges from input source (IS) to store gate (SG). During the integration time, the transfer gate TG is kept 'OFF'. Once the integration is complete, TG is switched 'ON' and charges are clocked out by vertical clocks ϕ_{CCD} of VSRs and subsequently by clocks of HSR. At each pixel level, on the side of store gate (SG), there is a transistor connected to this gate, which is used normally for background suppression applications. In fact, it is this transistor, which is utilized here for determining NU in our MUXs. The test signal (charge packet) is introduced electrically into the store gate through the background suppression drain (BSD) pin and the amount of charge is controlled by the potential of the background suppression gate (BSG). However, there are two methods by which the size of charge packet could be controlled while being introduced into store gate viz. diode cut-off method and fill-spill method [7]. In the former, the size of the charge packet integrated in store gate (SG), say Q_{dc}, is dependent on V_T (also called integration mode) of the inputting gate viz. background suppression gate (BSG) by:

$$Q_{dc} = A_{SG} C_{eff} [V_{BSG} - V_T - \phi_S - (2V_o\phi_S)^{1/2}]$$

(1)

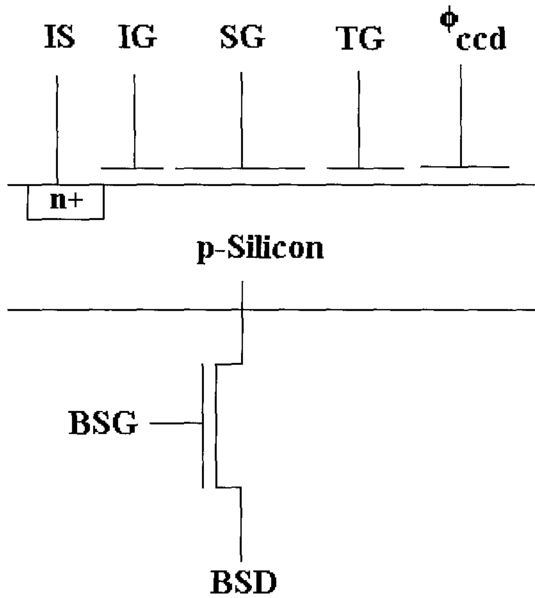


Fig. 2. The 'direct in jection' input structure used to in ject identical charge packets in all the pixels of the multiplexer array.

where $Vo = (qN_A\ \varepsilon_s) / (C_{eff}^2)$, V_{BSG} is the voltage on the background suppression gate, ϕ_S is the surface potential and V_T is its threshold voltage. Here the size of charge packet is controlled primarily by potential of background suppression gate and is dependent on V_T of this gate. And in the latter, Q_{fs} is almost independent of V_T because V_T terms cancel out in differencing while setting (for storage into store gate (SG)) the charge packet in 'fill-spill' and is given by [7]:

$$Q_{fs} = A_{SG}\, C_{eff}\ \ \Delta_{VG} \tag{2}$$

Where Δ_{VG} is the effective potential of charge storing well or the holding potential, this effective potential in the present case equals V_{SG} - V_{BSG} , where V_{BSG} and V_{SG} are the gate voltages on store gate and background suppression gate respectively, A_{SG} is the area store gate and C_{eff} is the effective oxide capacitance (including buried channel) per unit area in case of a buried channel CCD device. Here, the size of charge packet is primarily controlled by difference of potential on store and background suppression gate.

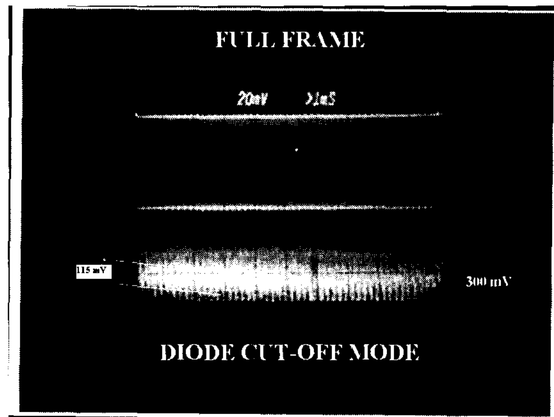
Before proceeding further, it is worthwhile to recall that V_T variation results mainly due to four factors: gate oxide thickness (t_{ox}) variations, channel doping variations, fixed oxide charge density (Q_f) variations and metal semiconductor work function difference (ϕ_{ms}) variations. This can immediately be seen from the equation of V_T as follows:

$$V_T = (Q_f - Q_{sdmax})\, t_{ox} / \varepsilon_{ox} + \phi_{ms} + 2\,\phi_f \tag{3}$$

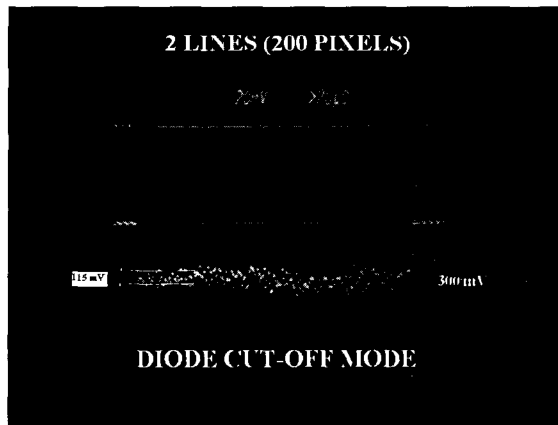
Where Q_{sdmax} is the maximum depletion layer charge density and ϕ_f is the fermi potential dependent on doping density. It may be seen from this equation that variations in oxide thickness, doping densities, fixed oxide charges and work function difference all add up to non-uniformity that is dependent on V_T and called 'V_T dependent non-uniformity, NU_{VT}. In addition to this, there are other sources of variation across the array from pixel-to-pixel due to different charge transfer efficiency (CTE) for different pixels (different pixels suffer different transfers), dark current variations dependent on lifetime variations, lithographic variations in definition of various gates and drains contributing to conversion of charge to voltage output of a pixel. All these contributions add up to total non-uniformity and called non-uniformity due to process, $NU_{process}$ in this paper.

Figure 3a shows the oscilloscopic output of full frame corresponding to all 10,000 pixels of 100x100 array whereas figure 3b shows the enlarged view of this output corresponding to only 2 lines (200 pixels) of the array. Contrary to our expectation, we do not see a flat random non-uniformity in the maximum output from these figures. Typical width of the grass (barring some local defects) i.e. true non-uniformity for the full frame is about 115 mV which can be attributed to purely V_T variation. Pure non-uniformity due to any source of variation from pixel-to-pixel is expected to give flat random output (as in Fig 4a & b). The remaining term of non-uniformity 185 mV (300mV-115 mV) is attributed to variation in non-linearity across the array due to charge inputting technique. It is well known that diode cut-off method is a non-linear technique[7]. Here, it is assumed that non-linear sources, resulting in increasing/decreasing type of output, as in figure 3a, do not contribute to non-uniformity across that array. In this mode, the charges were introduced into MUX array via background suppression drain and background suppression gate. Additionally, it may be seen from this

figure that maximum peak-to-peak (p-p) NU is about 300 mV whereas the average video output as measured from dark level is 450 mV. As discussed earlier, this NU is primarily dependent on process control and V_T variation. Furthermore, it may also be dependent somewhat on the dynamic range or the percent of full well capacity used. Here we are depicting the maximum p-p NU, occurring in our case at typically 75% of well capacity (or maximum saturating output). Also, a reset feedthrough of 600mV above the dark level can be seen from this figure.



(a)



(b)

Fig. 3. (a) The full frame output of 100x100 CCD multiplexer array using 'diode cut-off mode'. The non-uniformity(minimum grass width) without takkin into account nonlinearity is 115mV whereas the total non-uniformity is 300mV. (b) Enlarged view of two lines corresponding to 200 pixels of the array in 'Diode cut-off mode' showing the minimum non-uniformity of 115mV excluding the contribution of non-linearity whereas the total non-uniformity is 300mV.

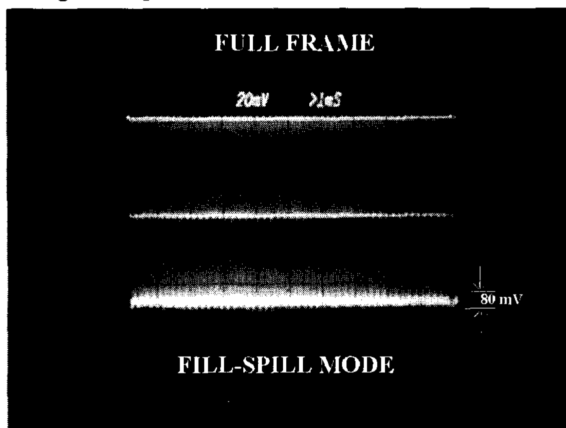
Now, for the actual operation of CCD MUX, charge from each pixel is integrated into store gate by integration mode using input gate and governed by equation (1). The detector is biased via input gate and hence its bias has built-in NU dependent on V_T variation of input gate. It can be seen from equation (1) that the NU in V_T of input gate across the array will introduce a non-uniformity in integrated charge packets even if the photo-generated charge packets coupled from detectors were constant. So in the actual output of MUX, FPA is going to see maximum of 300 mV NU (p-p) or typically 60 mV r.m.s. (r.m.s.= p-p/(4-6)) assuming it has a random normal distribution. A major part of this is due to non-linearity variation (185 mV), V_T variation and rest is due to the process variation. In this paper, we shall be concerned with non-uniformity contributors only. Assuming, non-uniformities due to V_T variations and process variations are not related (un-correlated), the total NU is given by:

$$NU_{tot}^2 = NU_{VT}^2 + NU_{process}^2 \quad (4)$$

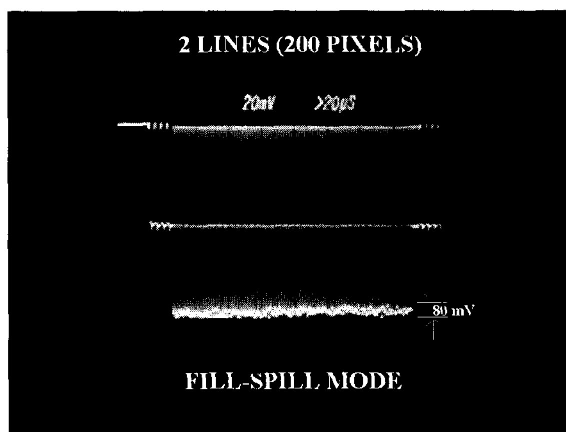
Contributory part from V_T variation viz. NU_{VT} may be possible to alleviate by novel methods of design of input coupling circuits which are V_T independent whereas latter is dictated by process control and may be reduced but cannot be eliminated completely which is referred to as intrinsic limiting process NU in this paper. Determination of this NU is the aim of this paper as it forms a valuable input to the designer. This can be determined by inputting a charge packet that is V_T independent i.e. 'fill-spill mode' and governed by eq. (2). Figure 4a shows the output of full frame corresponding to all 10,000 pixels of the array whereas figure 4b shows the enlarged view of 2 lines of the array corresponding to 200 pixels depicting a reduced peak-to-peak NU of 80 mV. This is the ultimate total limiting NU of the chip from all the sources such as process, material etc. except V_T variation. Here the charge packet has been inputted using 'fill-spill' technique wherein its size is V_T independent. This will be the limiting NU of the FPA even if the detector array was ideally uniform. Only improved processing and tighter material control can minimize it.

Additionally, one can assess the NU of V_T in input gate by this method that is generally a specification of CCD MUXs after separating the two NUs by making

following assumptions:



(a)



(b)

Fig. 4. (a) The output full frame of 100x100 array corresponding to all 10,000 pixels using 'full-spill' mode and showing the reduced non-uniformity of 80mV (b) The output to two lines corresponding to 200 pixels using 'fill-spill' mode and showing the reduced non-uniformity of 80mV.

1) NU due to V_T is independent from NU due to process as explained earlier. That is, one can add up these NUs in quadrature.

2) A strong correlation between V_T of BSG (background suppression gate) and IG (input gate), which is a reasonable assumption, because IG and BSG are closely spaced almost identical MOS gates. The threshold voltage variation across the array for these two gates shall be same and largely only process dependent because their dimensions are comparable. For a typical design requirement, the lengths of BSG and IG are of same dimensions whereas their widths vary by less than 5%, hence their V_T variation will be almost same. Therefore, NU of V_T measured on BSG shall hold for IG as well. Earlier such assumptions were verified by Foss et al [8] and used by Temes and Cheung [9] for alleviating V_T variation in IG of CCD MUX. This is called 'voltage differencing' technique.

In view of above, the estimate of peak-to-peak NU in input gate due to V_T variation alone is given by:

$$\begin{aligned} NU_{VT} &= (NU_{tot}^2 - NU_{process}^2)^{1/2} \\ &= (115^2 - 80^2)^{1/2} \\ &= 82.6 \text{ mV} \end{aligned} \quad (5)$$

This is total peak-to-peak NU due to V_T variation after neglecting variation due the non-linearity in the output as discussed earlier. Including the non-linearity contribution NU_{VT} using eqn.(5) is $(300^2 - 80^2)^{1/2}$=289 mV. Using this figure (289 mV) for estimation of NU in V_T will give overestimated results. Next, this NU_{VT} can be converted back to corresponding input gate voltage variation after taking into account the gain between input and output as follows.

Table 1: Measured V_T values on 10 test pixels by CFM method at 100 nA.

Pixel number	V_T (Volts)	ΔV_T (mV)
1,20	2.228	12
1,40	2.226	10
1,60	2.228	12
1,80	2.230	14
1,100	2.233	17
20,100	2.235	19
40,100	2.229	13
60,100	2.216	0
80,100	2.230	14
100,100	2.190	3

The NU_{VT} of 82.6 mV in the output is correlated with the background suppression gate (BSG) voltage level by measuring the change in output voltage level as a function of BSG potential. After optimizing the potentials of BSG and store gate properly, a plot of output vs. BSG voltage is constructed, which is linear in whole range barring near full well capacity (saturation of the charge in the well). From the linear portion of this plot, slope is estimated to be 4.4. Using this slope, p-p NU of 82.6 in output corresponds to about 82.6/4.4=18.8

(=output/slope) or ± 9.4 mV. Hence, it is estimated that ΔV_T of background suppression gate is 18.8 mV . This estimated value of about 18.8 mV compares well with direct measurement of V_T by current forcing method (CFM) [4] at 100 nA on 10 pixels located on periphery of the array. It may be recalled that CFM is the equivalent to actual operation of FPAs and is relevant here. Table 1 shows the results of the CFM done showing the maximum ΔV_T of 19 mV whereas our estimated value by readout method is18.8 mV that is very close with the actual measurement and comparable.

V. Conclusion

We have been able to determine experimentally intrinsic NU in CCD MUXs, which is the ultimate limiting contributor to total FPN of the FPA. The method can be utilized for other CMOS ROICs as well by incorporating proper test pins at the design stage.

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R.S. Saxena was born 1976. He did his Bachelor of Engineering degree in 1997 in Electronics and Communica-tions from G.B. Pant Engineering College, Pauri, UP (India) and is currently doing Master of Technology from Indian Institute He joined Solid State Physics Laboratory in 1998 as Scientist. His research interests include characterization of CCDs and IR detectors and VLSI.

R.K. Bhan He received his M.Sc Degree in Physics from Kashmir University, Srinagar, India in 1982 and Ph.D degree in Physics from Delhi University in 1994. He was initially Junior Research Fellow in “*Center for Applied Research in Electronics*” at Indian Institute of Technology, New Delhi from 1982 to 1984. He joined Solid State Physics Laboratory, Delhi as a scientist in 1984 where he is currently involved in Infrared Detector characterization. His research interests include MOS physics, CCDs, IR detectors and FPAs. He has published more than 40 research papers in international journals.