A New Basic Element for Neural Logic Functions and Capability in Circuit Applications

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Abstract— **This paper describes a new basic element which shows a synaptic operation for neural logic applications and shows function feasibility. A key device for the logic operation is the insulated-gate pn-junction device on SOI substrates. The basic element allows an interface quite compatible to that of conventional CMOS circuits and νMOS circuits.**

Index Terms **—SOI, gated-pn junction, neural logic, synaptic operation**

I. Introduction

Neural logic devices and circuits have been extensively studied [1,2], and recently, a νMOS transistor and its logic circuits were proposed [3.4]. While quantum effect devices may contribute to new functional applications [5-7] and many other devices have also been examined [8,9], they are still somewhat immature in terms of practical applications.

Hopefully, neural logic devices should be compatible with conventional CMOS logic circuits to utilize the well-known designs available with silicon LSI technology. It is considered that the νMOS transistor which shows a neuron-like operation (sum of product) is one of the desirable solutions. However, it can be considered that νMOS transistor does not reflect a synaptic operation flexibly.

In this paper, a new neural logic device which is recently proposed with a synaptic function [10] and simulation results of some circuit operations are described and discussed in detail. The device, the lateral, unidirectional, bipolar-type, insulated-gate transistor on SOI substrates (Lubistor) [11,12] can be used to realize a signal pre-processing whose operation is very similar to synapse, for key neural logic operations. Since the operation of the Lubistor is composed of the tetrode mode and the triode mode, flexible logic operations can be designed. The following sections discuss basic operations and possible function feasibility.

II. Device Structure, Model and Proposal of a New Logic Element

A. *Device structure and fundamental characteristics*

A cross-sectional view of the Lubistor and typical experimental I-V characteristics are shown in Figs. 1 and 2, respectively. In Fig. 2, the silicon layer thickness (t_s) is 10 nm, the gate oxide layer thickness (t_{ox}) is 5 nm, the buried oxide layer thickness (t_{BOX}) is 110 nm, the gate length (L) is 5 μm, and the gate width (W) is 10 μm [13]. When the bias configuration is as shown in Fig. 1(b), the Lubistor shows a tetrode characteristic at high gate voltages (V_G) and a modified triode characteristic at low gate voltages [11,12]. Thus, the Lubistor can have two natures; one is the feature of a MOSFET/SOI device at high gate voltages and the other is the feature of a forward-biased pn-junction device at low gate voltage. It is an important point that the anode current is suppressed as the gate voltage (V_G) increases at high anode voltages [11-13]; the negative transconductance is observed in this bias region. Therefore its operation can

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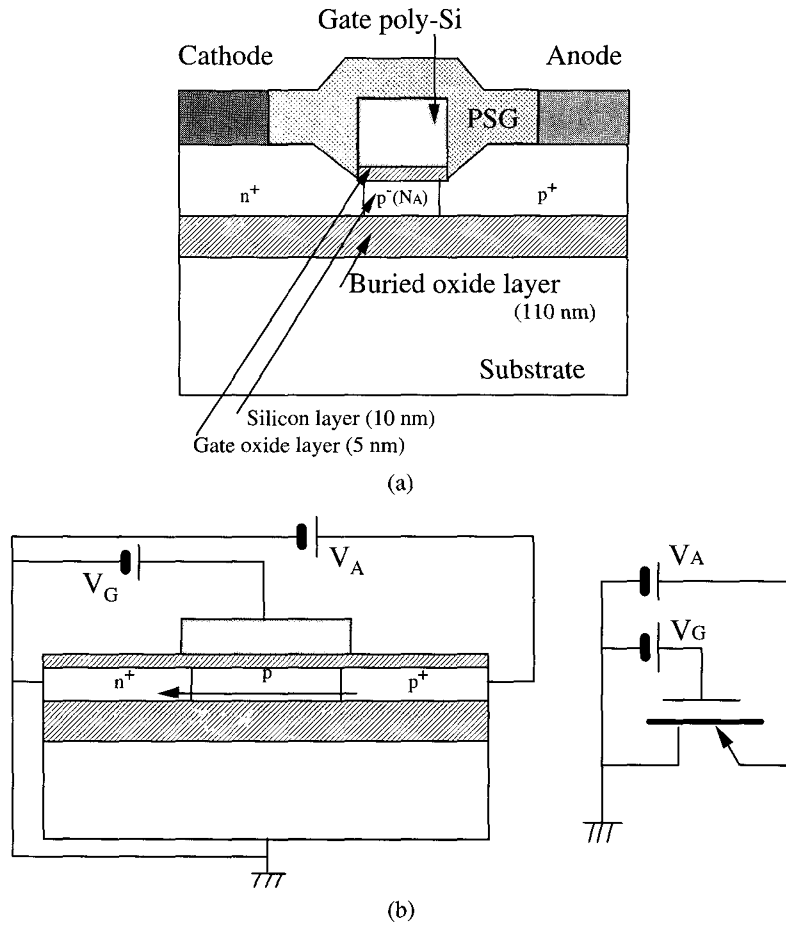

Fig. 1. . Schematic of device structure and its symbol (a) Schematic of the structure of insulated gate pn-junction device(lubistor) (b) Bias configuration for device operation and symbol of device

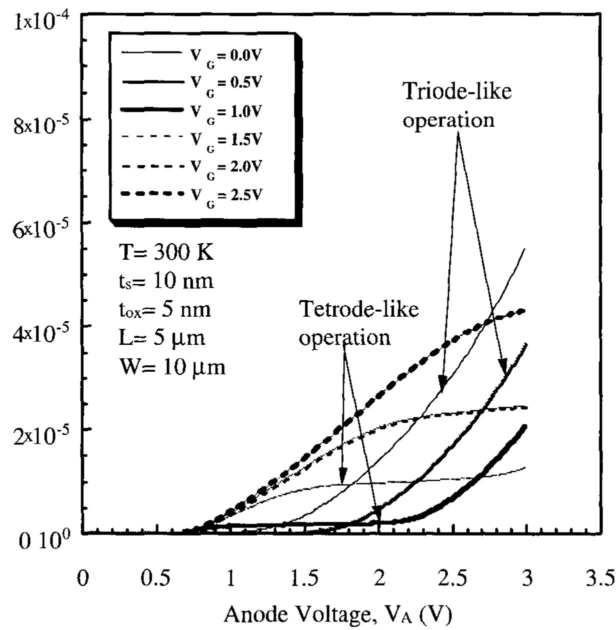

Fig. 2. Current-voltage characteristics of Lubistor. Tetrode-like or triode-like characteristics are found in different anode voltage regions.

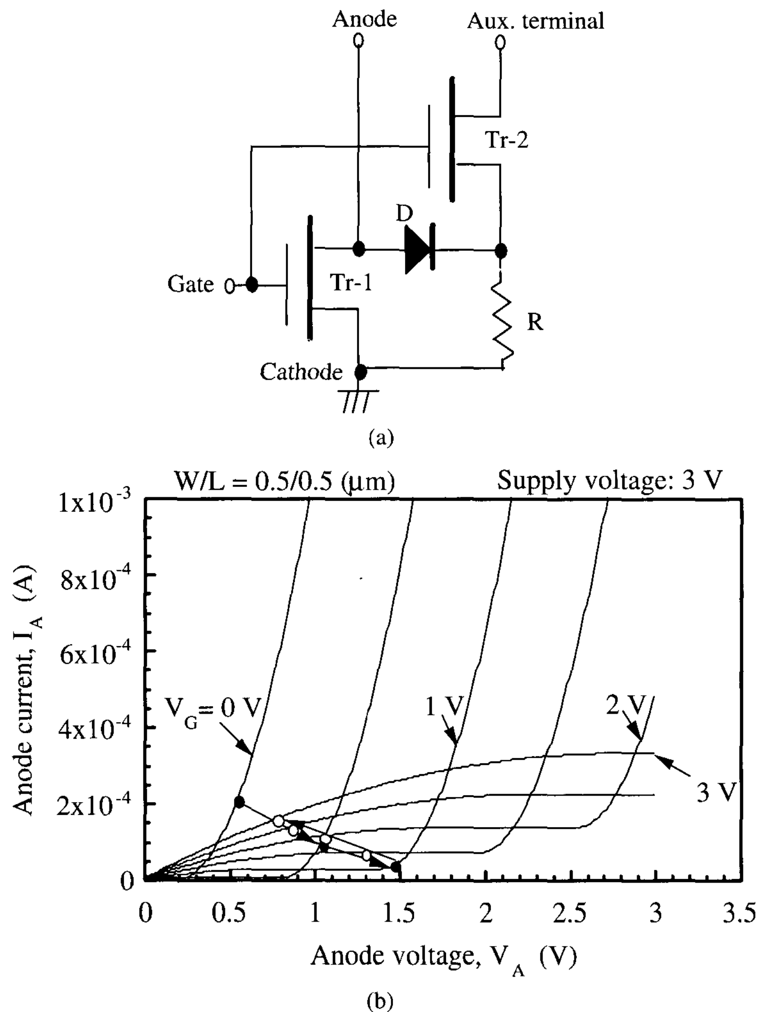

Fig. 3. An equivalent circuit model for the Lubistor (a) An equivalent device model for Lubistor. The auxiliary terminal is only used for adjusting the cathode voltage of diode, and the terminal is set being equal to the anode voltage of the Lubistor. (b) Simulation results based on the model. Basic device parameters are tuned to the usual 0.5-μm-CMOS process technology. Closed circles indicate loci of V_{out} in the logic element shown in Fig. 4(a). The locus moves as the gate voltage increases along with the arrow.

be symbolized as shown in the right hand side of Fig.1(b).

At the "OFF" state, the Lubistor has a built-in pn junction at the cathode side. At the "ON" state, however, the Lubistor has an actual pn junction, which is formed by the electron inversion layer and the p^+ anode, at the anode side. Since the Lubistor has a pn junction, the anode current is observed clearly at V_A larger than 0.7 V, which is different from the conventional MOSFET. At little bit high anode voltages, the anode current saturates so that the device shows a tetrode-like operation. In this V_A range, the saturation of anode current resu lts from the fact that the number of electrons, which contribute to the recombination with injected holes, is controlled by the gate voltage V_G. It should also be noted that the electron inversion layer reduces the effective hole diffusion length. At fairly high anode voltages, however, the anode current increases again so that the device shows a triode-like operation. In this V_A range, the anode bias diminishes electrons in the body because the body potential increases; the electron inversion layer disappears near the anode. In other words, the hole diffusion length increases with the anode voltage and the anode current increases again. Therefore, the critical voltage for V_A is about $V_G+V_{TH}+0.7$ (V) as observed in the figure.

B. *Device model for Lubistor*

Since the Lubistor has two natures as described in the previous section, I propose a model for DC simulations that is shown in Fig. 3(a). The transistor Tr-1 is the parasitic MOSFET/SOI at the cathode side, the diode D is the intrinsic pn junction device at the anode side, and the transistor Tr-2 is the implicit device to raise the cathode voltage of D by the resistor R. Since the supply voltage of auxiliary terminal is set being the anode voltage usually, the gate width of Tr-2 has been set being large so as to keep a voltage drop of R large. Device parameters for simulations are tabulated in Table 1 where the device parameters are tuned to usual 0.5-μm-CMOS technology for simplicity.

Simulation results of the Lubistor are shown in Fig. 3(b). Simulation results show a tetrode-like feature at the range of low-anode voltages and a triode-like feature at the range of high-anode voltages. The significant feature that the anode current at the high-anode voltage is suppressed by the increase in the gate voltage is reproduced by the proposed equivalent circuit model. However, it can be seen that simulated results are slightly different from Fig. 2. The difference appears in the low anode voltage region. This is due to the deficiency of the circuit model. The model should be improved in future. However, the characteristic difference in the low anode voltage region hardly affects the following simulations because all applications, presented here, are considered in high anode voltages.

Table 1. Device paramenters for simulations

Parameters	Values
Gate oxide layer thickness(tox)	10 nm
Gate length(L)	0.5 μm
Gate width(W)	100 μm(Tr-2)
	5 μm(Tr-1)
Threshold voltage(V_{TH})	0.2V
Electron mobility(μ_0)	500cm^2/Vs(Tr-1,2)
Resistor(R)	10Ω
Ideality factor(n)	1.5(Diode)

* These parameters are only used for the basic logic element.

C. *Proposal of a new logic element*

Figure 4(a) shows, as an example, the simplest logic element, which is composed of an nMOSFET/SOI and a p-p-n type Lubistor. The logic element has a control gate terminal (denoted by "C"), an input signal terminal (denoted by "I") and an output signal terminal (denoted by "O"). Simulated results of input-output characteristics are shown as a parameter of the control gate voltage in Fig. 4(b). It can be seen that the output voltage (V_{out}) initially increases as the input voltage (V_{in}) increases and reaches a peak at V_{op}. Subsequent increase in V_{in} leads to a steady fall in V_{out}. V_{op} and V_{ic} increase as the control gate voltage (V_{cg}) increases. Locus points of V_{out} are shown in Fig. 3(b) to explain the operation of this logic element where it assumed V_{cg}=3 V. Trace of loci is complicated, but interesting. The drain-to-source voltage of the load MOSFET traces along with the loci. When V_{in} is lower than V_{ic} (-1.3 V), the anode current of Lubistor decreases with increase in V_{in} because the Lubistor is in the triode-like mode; in the operation, the anode voltage of the Lubistor increases as shown in Fig. 3(b). When V_{in} is higher than V_{ic} (-1.3 V), the anode current of Lubistor increases with increase in V_{in} because the Lubistor is in the tetrode-like mode; the anode voltage decreases in this operation. Thus, V_{out} increases with V_{in} when $V_{in} < V_{ic}$ (-1.3 V), and it falls when $V_{in} > V_{ic}$. This characteristic is very interesting and useful because the operation of the logic element works like a synapse as discussed below.

Here, I simply explain the relationship between the operation of the logic element and the neural operation. Detailed discussion is described in the next section. The simplified model of neural function is expressed mathematically as [14]

$$V_i(T+\Delta t) = f(\sum_{j=1}^{N} J_{ij}V_j(t) - U), \ (i = 1......N), \quad (1)$$

where $V_j(t)$ is the *j-th* activated neuron potential at the time t, Δt is the delay time for the neuron to fire, U is the threshold potential to fire, J_{ij} is the synaptic strength between the *i-th* neuron and the *j-th* neuron, and f(x) is the sigmoid function [14, 15]. The vMOS transistor successfully simulate the sigmoid function in (1) with specifically fixed synaptic strengths [3]. However,

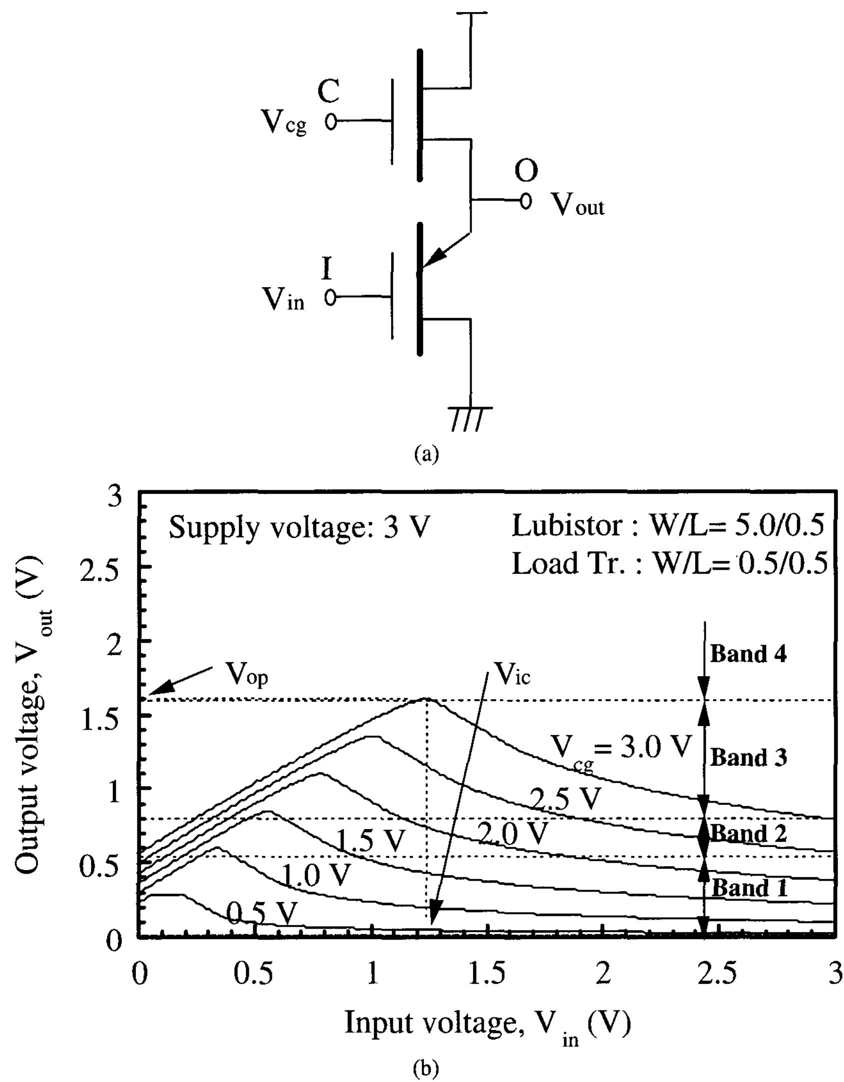

Fig. 4. A basic element and input-output voltage characteristics (a) Basic logic element (b) Input-output characteristics of the basic logic element

flexible synaptic strengths are required to design variable functions. In the vMOS transistor, for example, apparent flexibility of synaptic strength can be realized by using digitized input signals.

The basic logic element proposed here can simulate very flexible synaptic strength by using the control gate "C" in Fig. 4(a). The combination of one basic logic element and two-following CMOS inverters with certain logic threshold (V_{LT}) is shown in Fig. 5(a). In the following, I consider the case of V_{cg}=3 V (supply voltage) for simplicity. I assume the pulse frequency modulation signal is used here as an input signal. When V_{LT} is smaller than V_{out} at V_{in}=0 V ("band 1" in Fig. 4(b)), the output voltage ($V_{out,s}$) of the last CMOS inverter is always equal to 3 V without regard for the input voltage (V_{in}); the logic element operates like an "axon" (pattern (i) in Fig. 5(b)).

When V_{LT} is between V_{out} at V_{in}=0 V and V_{out} at V_{in}=3 V ("band 2" in Fig. 4(b)), the output voltage ($V_{out,s}$) of the last CMOS inverter changes abruptly from 0 V to 3 V as the input signal voltage (V_{in}) increases; the synapse characteristic is "excitatory" (pattern (ii) in Fig. 5(b)). The input voltage (V_{BI} in Fig. 5(b)-(ii)) at which the synapse goes excitatory depends on both V_{LT} and the control gate voltage (V_{cg}), which means that the sensitivity of the synapse can be controlled by either V_{LT} or V_{cg} or both. As an example, consider the case that a capacitor is connected to the control gate terminal "C" of

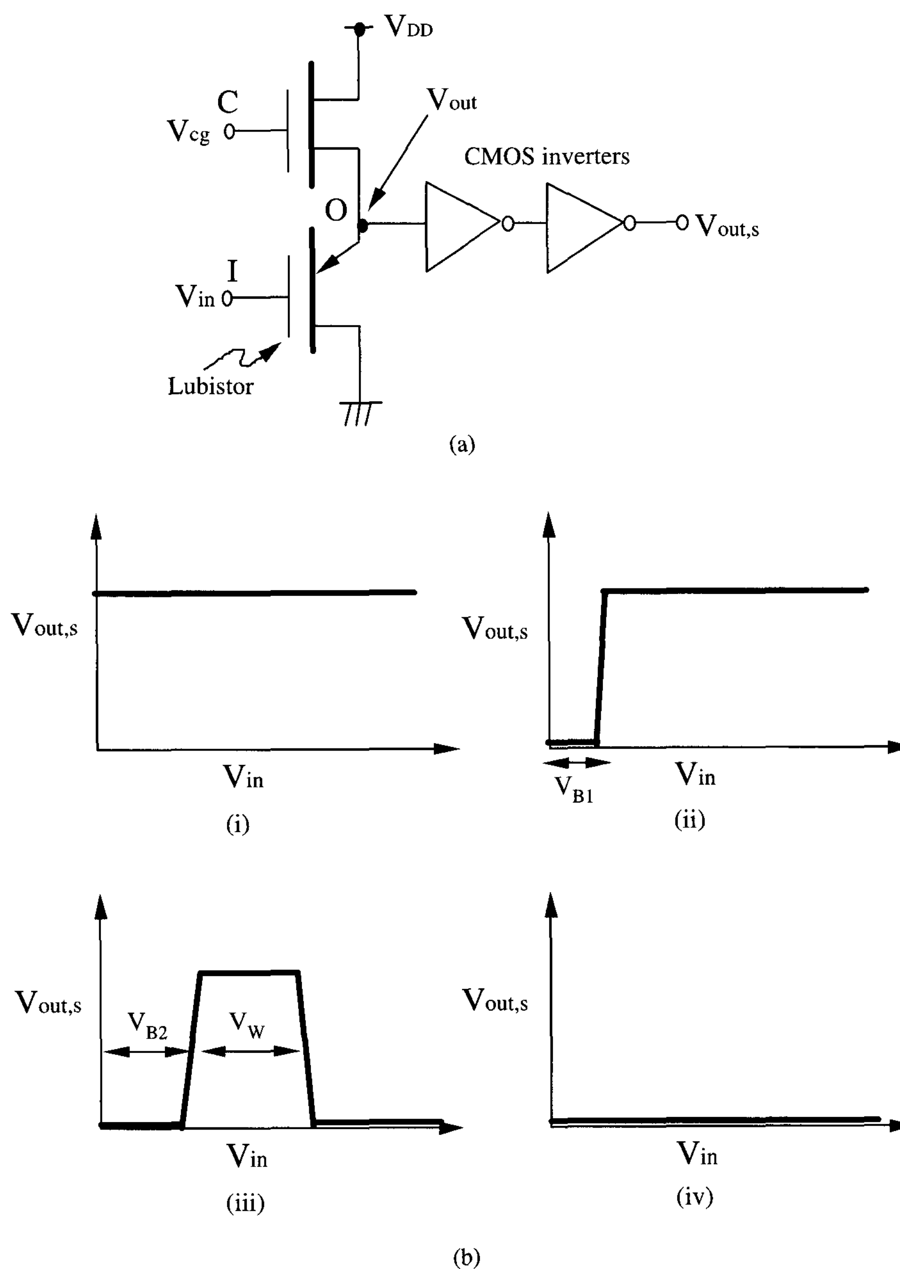

Fig. 5. . Simplified logic unit simulating a synaptic operation (a) The simplest circuit for synaptic operation (b) Schematics diagrams of synaptic operations

the proposed logic element in Fig. 5(a). When charges are transferred to the capacitor from the other terminal, such as memory circuits, the amount of charge determines the control gate voltage V_{cg} (equivalently the weight to input signal for neural devices). Since the given weight modulates V_{B1} of the logic element, the logic element works as a weighted logic gate.

When V_{LT} is between V_{out} at V_{in}=3 V and V_{op} ("band 3" in Fig. 4(b)), the last CMOS inverter gives a single pulse-like signal which can be used as a window function (or literal function)[15]; the synapse characteristic is "semi-excitatory" (pattern (iii) in Fig. 5(b)). This pattern shape is controllable by V_{cg}. The input voltage (V_{B2} in Fig. 5(b)-(iii)) at which the synapse goes excitatory also depends on either V_{LT} or the control gate voltage (V_{cg}) or both; this is also true for the bias

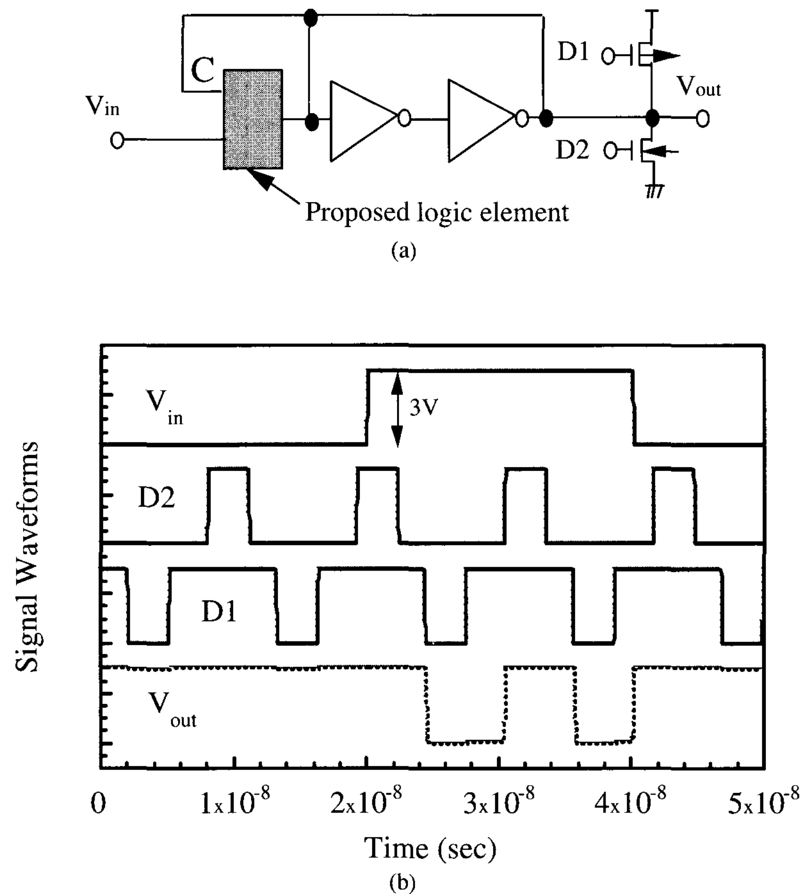

Fig. 6. An example of circuit application and input-output characteristics (a) A "data holding function." (b) Simulation results of the "data holding function."

window (V_W in Fig. 5(b)-(iii)). This means that the sensitivity of the synapse can also be controlled by both V_{LT} and V_{cg}.

When V_{LT} is larger than V_{op} ("band 4" in Fig. 4(b)), CMOS inverters are not activated and the output voltage ($V_{out,s}$) of the last CMOS inverter holds at 0V without regard for the input signal voltage (V_{in}); the synapse characteristic is "inhibitory" (pattern (iv) in Fig. 5(b)).

By designing the logic threshold of the CMOS inverters appropriately, one of the above four functions can be chosen for a certain fixed V_{cg} value. Of particular interest, operations (i), (ii) and (iv) are applicable to setting weight factor (α_w) in neural applications; (i) for α_w=0, (ii) for $0<\alpha_w<1$, and (iv) for α_w=1. Since a pair of CMOS inverters gives a binary logic output signal, the logic element shown in Fig. 5(a) is compatible with conventional LSIs.

The important point is that the above four operations are flexibly changed by the control gate ("C") voltage. In other words, the control gate voltage (V_{cg}) directly determines the synaptic strength. It is easily noticed that the output signal patterns shown in Fig. 5(b) can be used as an input signal to a νMOS transistor. The combination of the basic logic element and an SOI νMOS transistor should yield new functional applications. Examples of important applications and functions of the proposed basic element are discussed later.

Circuit operations similar to Fig. 4(b) have already been examined by Y. Sekine et al.[16]. However, the aim of their work was to produce pulse series to simulate output signals of neurons by use of the negative conductance characteristics. The circuit needs several passive elements such as quite a large capacitor, which means that monolithic LSIs would be difficult to realize. As discussed later, a similar operation is easily demonstrated in a very simple circuit without any

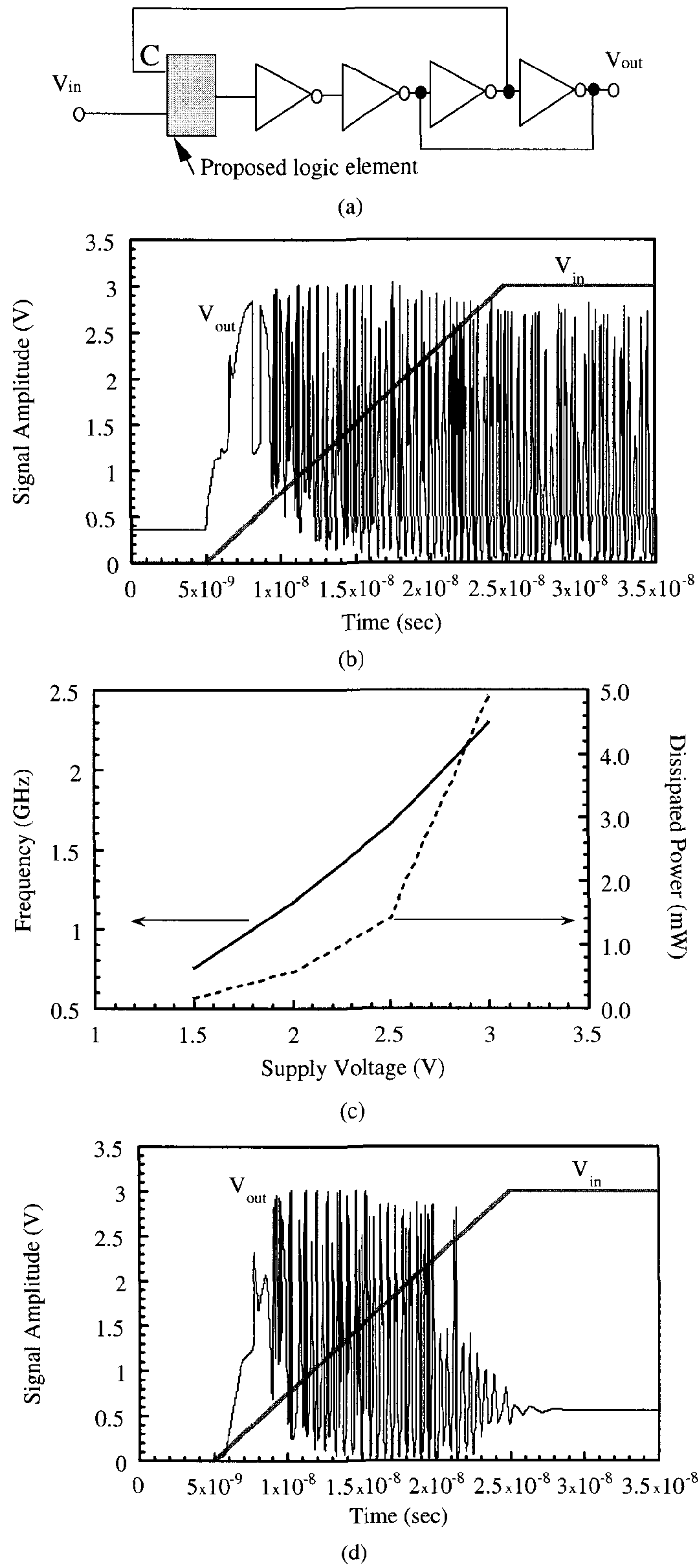

Fig. 7. An example of circuit application and input-output characteristics (a) A selective "oscillation function." (b) Simulation results of the selective "oscillation function." (c) Dependence of oscillation characteristics on supply voltage (d) Simulation results of the "geyser function."

additional passive elements by using the basic logic element proposed here.

III. Circuit Applications and Discussion

A. *Examples of fundamental elements for circuit applications*

The important characteristic of the logic element shown in Fig. 4 was discussed simply in the previous section. This section discusses more practical circuit operations including a couple of important applications. Examples are shown in Figs. 6-8.

Figure 6(a) shows a small circuit element which has the function of data holding. In this circuit, just the output signals of the proposed basic logic element and the last CMOS inverter are fed back to the control gate terminal in the element shown in Fig. 5(a). The two CMOS inverters also work as a positive-feed-back amplifier. The MOSFET for "D1" is p-channel type and that for "D2" is n-channel type. Simulation results are shown in Fig. 6(b). It is assumed that the V_{LT} of the first CMOS inverter lies inside band 3 at low control gate voltages and low V_{in} (see Fig. 4(b)). When the input signal (V_{in}) is level "0" and the output signal of the last CMOS inverter, which is equivalent to that of the control gate terminal ("C"), is "1" level, any input signal from "D1" or "D2" to replace the data with new data is rejected and V_{out} holds the "1" level. This is because the output level of the proposed logic element is beyond V_{LT} of the first CMOS inverter and the output level of the first CMOS inverter goes down to "0" level. This state is fixed by the positive-feed-back effect of the two CMOS inverters. In this case, naturally V_{out} is insensitive to any disturbance from the "D1" or "D2" terminal. On the other hand, when the input signal (V_{in}) is "1" level, the data at the V_{out} terminal is replaced with new data by a signal from "D1" or "D2" as shown in Fig. 6(b). As shown in Fig. 4(b), this is because, at high V_{in}, the V_{LT} of the first CMOS inverter lies inside band 3 at low control gate voltages and it lies inside band 1 at high control gate voltages. When V_{out} is changed from level "1" to level "0" by the signal from "D2", V_{out} becomes lower than V_{LT} of the first CMOS inverter. This state is stable due to the positive-feed-back effect of the two CMOS inverters. When V_{out} is changed from level "0" to level "1" by the signal from "D1", V_{out} becomes higher than V_{LT} of the first CMOS inverter. This state is also stable due to the positive-feed-back effect. Thus, the circuit shows a "data holding function" when V_{in} is "1" level.

Figure 7(a) shows a circuit which has the function of selective oscillation. In this circuit, the output signal of the third CMOS inverter is fed back to the control gate terminal ("C") in the element shown in Fig. 5(a), and the output signal of the last CMOS inverter is fed back to the third CMOS inverter. First, we consider the case wherein that the V_{LT} of the first CMOS inverter lies inside band 2 (see Fig. 4(b)). Simulation results are shown in Fig. 7(b). It should be noted that the output signal level (V_{out}) oscillates during the transition and the level "1" of V_{in}. When the input signal (V_{in}) is level "0" and the control gate terminal ("C") is also "0" level, the output signal of the first CMOS inverter is automatically level "1" because the output signal level of the proposed basic element does not reach the V_{LT} of the first CMOS inverter, which is obvious in Fig. 4(b). This means that the output level of the third CMOS inverter which is equivalent to the level of "C" should change to "1" level. Consequently, the output signal level (V_{out}) oscillates. Figure 7(c) shows the dependence of the oscillation characteristic on supply voltage. The circuit oscillates at giga-Hz rate with a low-power dissipation.

Second, we consider the case wherein the V_{LT} of the first CMOS inverter is inside band 3 (see Fig. 4(b)). Simulation results are shown in Fig. 7(d). It should be noted that the output signal level (V_{out}) oscillates only during the transition of V_{in} unlike the former case. The fundamental oscillation mechanism is identical to that in the former case. Since the V_{LT} of the first CMOS inverter lies inside band 3, the first CMOS inverter shows the operation of function (iii) in Fig. 5(b) during the transition of V_{in}. An intermittent pulse is obtained at the output terminal of the proposed logic element. Therefore, the oscillation mode can be modulated by the intermittent pulse to produce a "geyser". The width of the "geyser" is determined by the logic threshold of the CMOS inverter; namely, the width is defined by V_W as shown in function (iii) of Fig. 5(b).

When the CMOS inverter following the proposed logic element is replaced with a NOR block or a NAND block, this function is extended to a multi-input circuit.

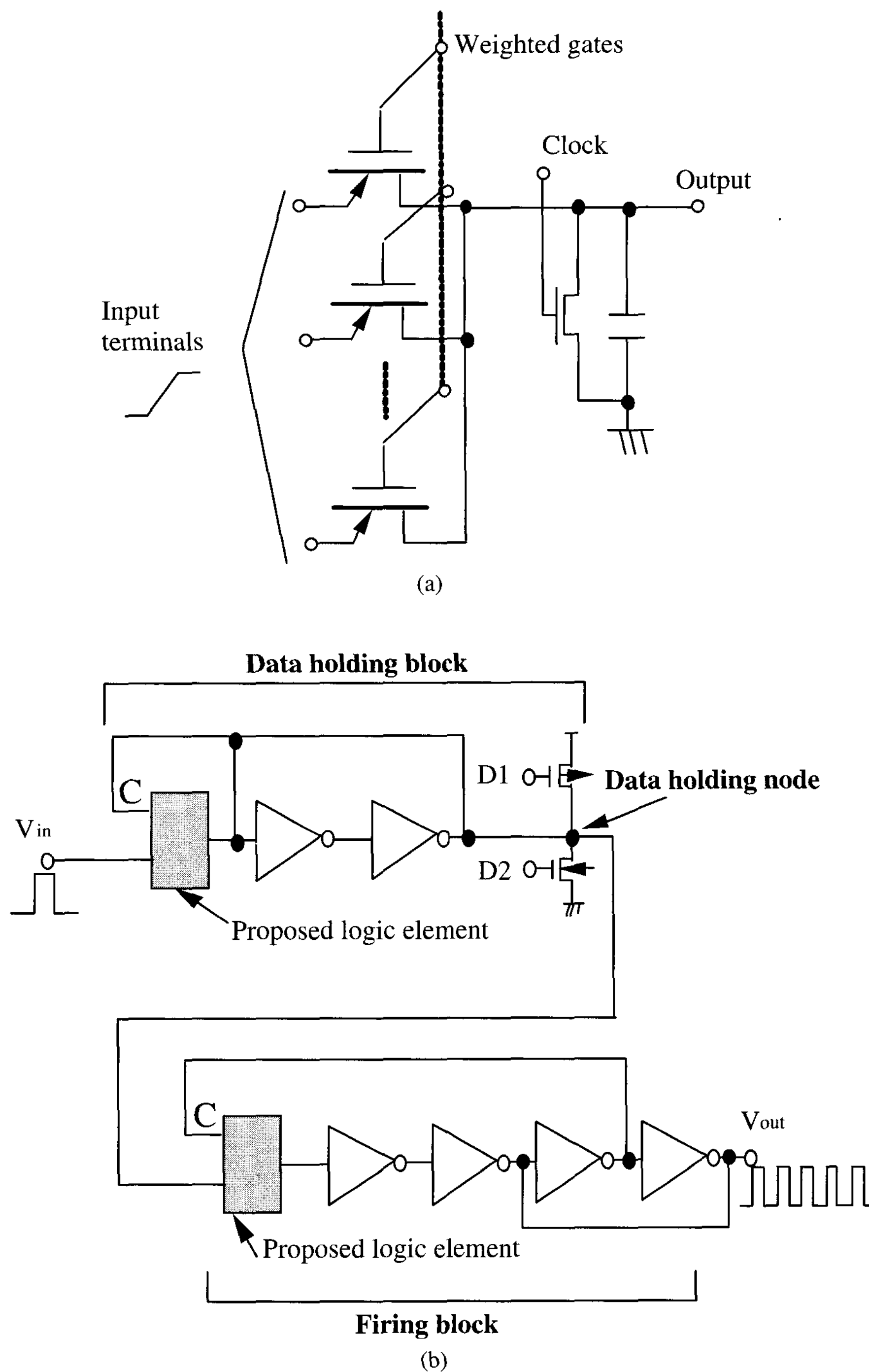

Fig. 8. An example of Boltzmann machine neuron block (a) A sum-of-product unit using Lubistors. (b) A stochastic-response unit.

The number of input terminals is not limited.

The above consideration suggests the proposed basic element is applicable to a Boltzmann machine neuron circuit. The Boltzmann machine is a kind of feed back neural network which can solve various complicated problems [14, 15] and consists of a large network of neurons interconnected bidirectionally with various connection strengths. In its basic form, the Boltzmann machine neuron consists of a sum-of-product unit and a stochastic-response unit. An example of a sum-of-product unit is shown in Fig. 8(a). In Fig. 8(a), the Lubistor plays an important role because it has the nature

of "unilateral" current path. The sum-of-product result is automatically obtained in the capacitor. It can be reset by the MOSFET to yield a "clock" terminal. The weight at each input terminal can be defined by weighted gate pulses which have different heights or widths. Data from input terminals are gathered into the capacitor. A practical example of a neuron block as a stochastic-response unit composed of 9 equivalent CMOS inverters is shown in Fig. 8(b). Since this block includes a memory unit using the data holding function proposed in Fig. 7(a), it is superior to conventional neuron circuits. The stochastic operation to determine whether a neuron fires or not is controlled by a digital pulse from Vin in Fig. 8(b). For example, level "0" of V_{in} results in the continuous oscillation signal ("firing" of neuron) at the V_{out} terminal. On the other hand, level "1" of V_{in} results in the selective oscillation signal depending on the data at the data holding node. The oscillation mode is selected by signals from "D1" and "D2" terminals. In this case, it is preferable to use the output voltage of the circuit in Fig. 8(a) as input to "D1" and "D2" terminals. In other words, the sum-of-product is reflected on the state of neuron; the level "0" signal for "D1" terminal changes the neuron state to "excitatory" state, and the level "1" signal for "D2" terminal changes the neuron state to "inhibitory" state. In this operation, functions (i), (ii) and (iii) in Fig. 5(b) are all used automatically. Consequently, these blocks work as a unit in the Boltzmann machine neuron circuit.

B. On the further improvement of functions of the basic logic element

In this paper, I described the basic logic element to simulate a synapse. In this "synapse", the synaptic strength has to be controlled by the voltage of control gate ("C"). In practical applications, this must be overcome to improve the flexibility of synapse strengths. In other words, the flexibility of synapse means a memory effect in synapses. To realize a synapse with some memory effect, I must use some ferroelectric material as a gate insulator to simplify the complicated circuit.

On the other hand, the design issue of Lubistors is one of remained problems. However, since the device operation is not so complicated and the device model can be simplified, the design technique will be readily developed.

Then, at least, I think the combination with an advanced logic element with the memory effect and the vMOS transistor will result in a greatly improved circuit performance in future.

IV. Conclusion

A basic element for new neural logic operation devices has been proposed and some functions such as a synaptic function have been demonstrated. It has been shown that a key device for the logic operation is the insulated-gate pn-junction device on SOI substrates. The device model for simulations was proposed. By using the model, features of practical circuits were examined. The basic element shows various characteristics depending on the device dimension and the control gate voltage. It has been shown that the operation of the basic element is applicable to neural circuits. One important aspect is that the basic element offers an interface quite compatible to that of conventional CMOS circuits. Therefore, many kinds of circuit applications seem possible.

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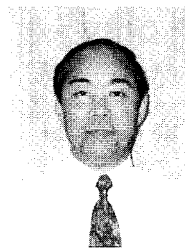

Yasuhisa Omura received the M. S. degree in applied science in 1975 and the Ph. D. Gree in electronics in 1984, both from Kyushu University. He joined the Musashino ctrical Communications Laboratories, NTT, in 1975. He worked on short-chan OS/SIMOX design, LSI processing, and SOI device modeling. In NTT, he contribut Crial demonstratins of 1-kb and 4-kb CMOS/SIMOX SRAM on the device design an rication processing. He moved his position from NTT Atsugi R&D Center to Kans university, Osaka Prefecture, as a professor after April in 1997, and he is presently rking on device physics of ultimately miniaturized MOSFET/SOI, modeling for MOS vice design and development of silicon opto-electronic devices. He has published 75 ular papers and 55 conference proceedings. He is one of authors having published evice and Circuit Cryogenic Operation for Low Temperature Electronics." (2001, wer Publishers) He has invented various SOI devices-for example – the lateral unidirectional Olar-type insulated-gate transistor (Lubistor), the high-gain cross-current tetrode KT) MOS device, and tunneling-barrier junction (TBJ) SOI MOSFET using SIMOX Hnology. He has patents for Lubistor in Japan, U.S.A., Canada, United Kingdom, Germany, Netherland, Italy, and Korea. He has 30 patents in Japan and several ents in U.S.A. for SIMOX device technology. He was honored with the Annual Resercher Award in 1981 from IEICE, Japan. He has worked on ultra-thin SFET/SIMOX device technology over 20 years. He demonstrated 0.1-μm-gate OS/SIMOX devices with a long lifetime in 1991 IEEE IEDM and 1992 Int. Conf. on aracteristics devices and Materials (SSDM). He also demonstrated mesoscopic transport Of 50-nm-channel SOI MOSFETs with 2- or 6-nm-thick silicon film in To indicate perspectives of future SOI devices He served the Technical Committee of IEEE Int. SOI Conf. From 1997 to 1998, and Serves the Program Committee of Int. Symp. On BLSI Technology from 1997. zn Dition he serves the Program Committee of Int. Workshop on Low-Temperature Ctronics (in Europe) from 1998. Dr. Omura is a member of the Japan Society of Applied Physics (JSAP), the Physical Ciety of Japan, the Electrochemical Society, a senior member of the Institute Ctrical and Electronics Engineers (IEEE) and a member of the Insitute of Electronice Ormation and Communication Engineers (IEICE).