Fractional-N Frequency Synthesizer with a 1-bit High-Order Interpolative $\Sigma\Delta$ Modulator for 3G Mobile Phone Application

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Abstract — This paper presents a 18-mW, 2.5-GHz fractional-N frequency synthesizer with 1-bit 4th-order interpolative delta-sigma ($\Delta\Sigma$) modulator to suppress fractional spurious tones while reducing in-band phase noise. A fractional-N frequency synthesizer with a quadruple prescaler has been designed and implemented in a 0.5-μm 15-GHz f_t BiCMOS. Synthesizing 2.1 GHz with less than 200 Hz resolution, it exhibits an in-band phase noise of less than −85 dBc/Hz at 1 kHz offset frequency with a reference spur of −85 dBc and no fractional spurs. The synthesizer also shows phase noise of −139 dBc/Hz at an offset frequency of 1.2 MHz from a 2.1GHz center frequency.

Index Terms — phase-locked loop, fractional-N, frequency synthesizer, fractional spurs, reference spurs, phase noise, delta-sigma modulator, pulse swallow technique.

I. INTRODUCTION

Recent technical trends in wireless communications show a real-time multimedia data transfer, 144 kbps or more in CDMA-2000 1X and WCDMA. In these applications, a RF frequency synthesizer, as a program-

mable local oscillator signal, must satisfy several key electrical performances: fast switching time, fine frequency resolution, low phase noise, and low spurious tones. In the CDMA-2000 1X [1], the inter-frequency hard hand-off and quick paging need a frequency synthesizer that has a switching time of less than 1 ms while keeping the frequency resolution of 10 kHz.

Frequency synthesis technique usually uses phase-locked loop(PLL). The loop bandwidth of a phase-locked loop should have sufficiently smaller bandwidth than the comparison frequency for keeping loop stability. In an integer-N frequency synthesizer, its comparison frequency of phase-frequency detector should be equal to the frequency resolution. Thus, a integer-N frequency synthesizer that provides low frequency resolution may results in slow switching time. For example, an integer-N frequency synthesizer with a 500 Hz loop bandwidth for a 10 kHz frequency resolution would have a switching time of about 10 mS. Such a bandwidth limitation might make the integer-N frequency synthesizer unsuitable for the 3G wireless phone applications such as CDMA-2000 1X and WCDMA.

In fractional-N frequency synthesizer, on the other hand, faster switching time can easily be achieved because the higher comparison frequency than required resolution frequency allows wide loop bandwidth. A fractional-N frequency synthesizer with a 10 kHz loop bandwidth for a 10 kHz frequency resolution would have switching time of about 500 μS.

A fractional-N PLL-based frequency synthesizer allows a lower in-band phase noise than that in an integer-N counterpart because of lower loop divide ratio in the fractional-N PLL-based frequency synthesizer.

Previous published delta-sigma modulated fractional-

Table 1. Summary of measured performance.

Supply voltage (Vdd)	2.7 – 4.0 V
Current consumption for RF and IF FS with $V_{DD}=3V$	7.5 mA
Max. operating frequency	> 2.5 GHz
RF input sensitivity	< -15 dBm
In-band phase noise	-85 dBc/Hz*
Out-of-band phase noise	-139 dBc/Hz at 1.2 MHz*
Reference spurs	< -85 dBc
Fractional spurs	Not observed
Switching time	< 500 μs**

* $f_{pd}=9.6$ MHz and $f_{vco}=2.11485$ GHz
**Loop bandwidth=12 kHz, 59 MHz step change, and tolerance 100 Hz
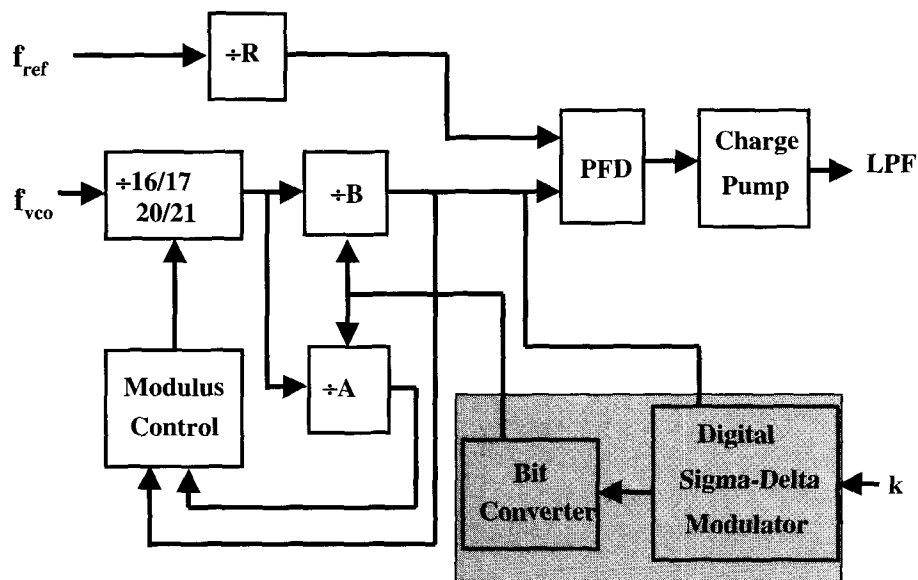
$f_{vco}=f_{ref}$ / R * (N + f), where N=P*B+A and f=k/F (-0.5 ~ +0.5)

Fig. 1. Proposed fractional-N frequency synthesizer.

N frequency synthesizers [2]-[5], [7] have shown good performance in the view points of fast switching time, fine frequency resolution, and negligible fractional spurs. However, they need a further improvement of out-of-band phase noise around 1 MHz offset (usually > -130 dBc/Hz). For the CDMA-2000 1X PCS application, the out-of-band phase noise should be less than −135 dBc/Hz at 1.2 MHz offset, to satisfy the single-tone desensitization requirement [1]. Further more, the

fractional-N frequency synthesizers in [2], [4] suffer large spurs (-45 ~ -50 dBc) at a particular operating condition that results from nonlinearity in the PFD, multi-modulus divider, and the multi-bit modulator [2].

This work proposes a new fractional-N frequency synthesizer with a 1-bit 4th-order single-loop ΔΣ modulator. The proposed fractional-N frequency synthesizer achieves good in-band/out-of band phase noise and fractional spurs while providing a fast
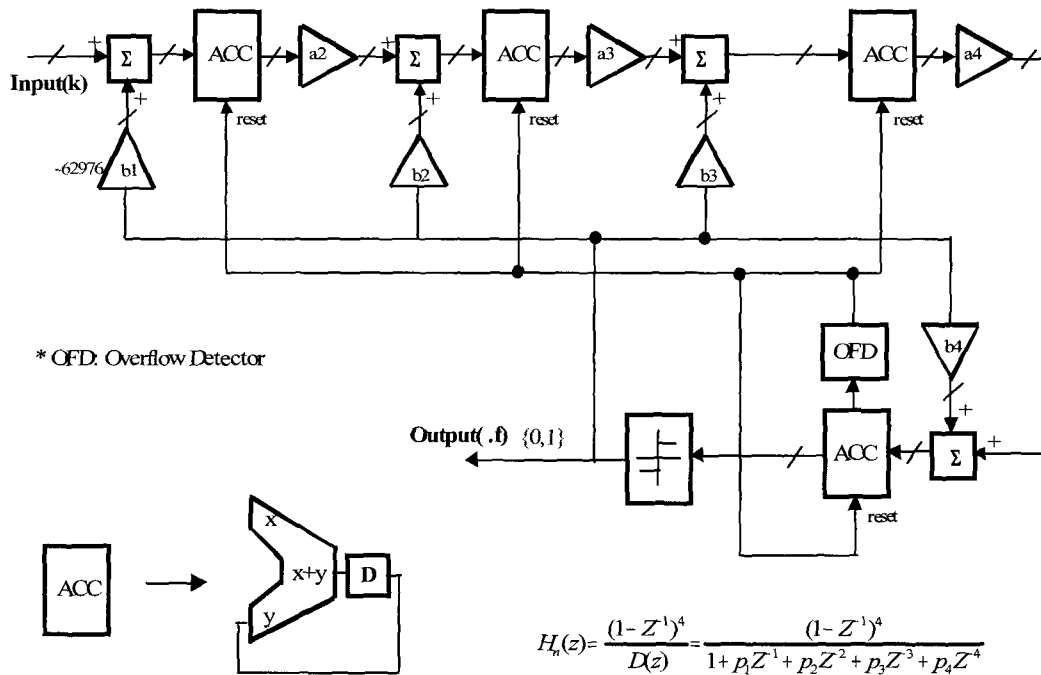
Fig. 2.   Functional block diagram of the 1-bit 4th-$\Delta\Sigma$ modulator.

$$H_n(z) = \frac{(1-Z^{-1})^4}{D(z)} = \frac{(1-Z^{-1})^4}{1 + p_1 Z^{-1} + p_2 Z^{-2} + p_3 Z^{-3} + p_4 Z^{-4}}$$

switching speed and fine frequency resolution.

II. ARCHITECTURE AND CIRCUITS

A. Proposed Synthesizer Architecture

Fig. 1 shows the proposed frequency synthesizer, which consists of a pulse-swallowed quadruple divider, a signle-bit 4th - order$\Delta\Sigma$ modulator with multiple feedback, and a bit converter.

The bit-converter, consisting of a multiplexer and an adder, is an interface circuit that combines the single-bit output of the $\Delta\Sigma$ modulator into the pulse swallow counter. The interface circuit is required to adjust an output range of the modulator to fit into the discrete integer division step of the modulus divider so that the frequency synthesizer can realize same fractional division step in a covered division range. The $\Delta\Sigma$ modulator functions as a fractional division controller whose single-bit output controls a division ratio of the pulse-swallowed quadruple divider through the bit-converter. The single-bit output helps us avoid the nonlinearity problem.

The $\Delta\Sigma$ modulator effectively pushes the quantization noise into out-of-band, resulting in greatly

suppressed in-band noise power. After low-pass filtering by the PLL loop filter, a time-averaged low-frequency fractional value with a high S/N can be obtained from the modulator. The effective value of the modulator output is made to be a fractional number between two contiguous integers, given as .f = k/62976 for −31488 < k < 31488.

When the fractional-N PLL-based frequency synthesizer is in lock state, the RF VCO outputs a stable N.f times the comparison frequency. The total division ratio of the PLL loop becomes N.f = BP+A + k/62976, where B, A, and k are programmable value and P is 16 or 20, and has 62976 times finer resolution than in integer-N frequency synthesis technique. Thus, the fractional-N frequency synthesis technique can use a much higher PFD comparison frequency than in integer-N counterpart, while keeping the same frequency resolution, and allows a larger loop bandwidth and fast switching time.

In the architecture, the single-bit output feature of the $\Delta\Sigma$ modulator and the use of the pulse-swallowed quadruple divider result in a simple architecture, reducing power consumption, and solving the nonlinearity problem, when compared with multi-modulus divider or multi-bit modulator.

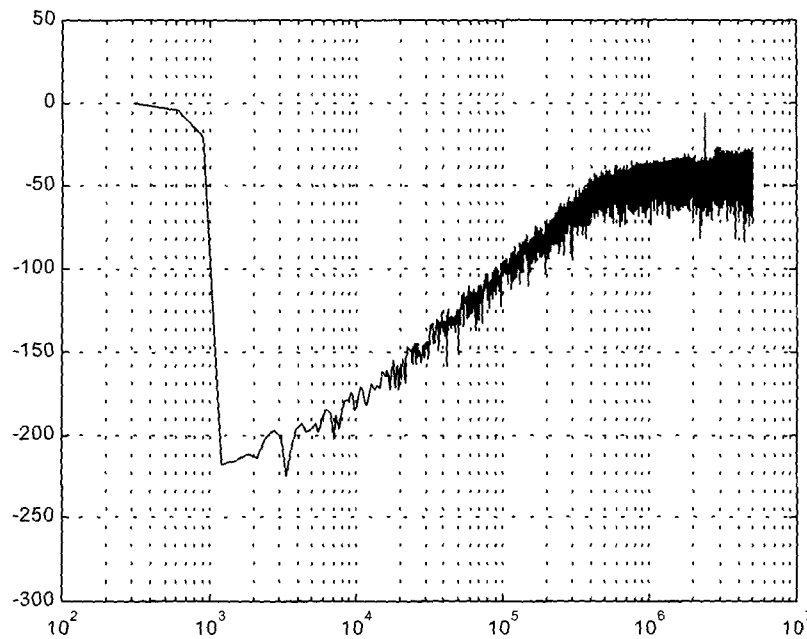To improve out-of-band phase noise in the fractional-

Fig. 3. Measured S/N of the $\Delta\Sigma$ modulator for k = 32768.

N frequency synthesizer, considerable efforts were poured into the design and optimization of the $\Delta\Sigma$ modulator section.

B. Single-Bit 4th-Order $\Delta\Sigma$ Modulator

The single-bit 4th-order $\Delta\Sigma$ modulator with MSB feedback is shown in Fig. 2. The output signal magnitude at dc and noise transfer function (NTF) of the $\Delta\Sigma$ modulator are given as;

Output signal magnitude at dc = k / b_1= k / 62976, and NTF = $(1-z^{-1})^4$ / D(z),

where k is a programmable input data of the $\Delta\Sigma$ modulator and D(z) is a 4th-order polynomial with the Butterworth pole alignment to guarantee loop stability of the modulator.

An optimal selection of the NTF corner frequency improves out-of-band noise performance in the frequency synthesizer. This is due to the fact that the $\Delta\Sigma$ modulator shows a high pass characteristic over the quantization noise and that the LPF in the PLL can not sufficiently filter off its high frequency noise power. For example, when a fraction-N frequency synthesizer uses a MASH [5] 4th-order $\Delta\Sigma$ modulator, D(z)=1, 3rd-order passive LPF, PFD comparison frequency of

about 10 MHz, and divide ratio of 160, a low-frequency portion of the quantization noise (<< -100 dBc/Hz) is sufficiently lower than a low-pass noise in PLL (~ -85 dBc/Hz) while its high frequency portion is no longer negligible than VCO noise (~ -140 dBc/Hz at 1 MHz offset). Thus, the optimization should be done in the $\Delta\Sigma$ modulator with the objective of lowering the quantization noise over out-of-band and of loosing in-band noise.

This can be done by controlling the NTF corner frequency and by lowering a high frequency noise shaping gain. In our design, the NTF has corner frequency of 0.04 times the comparison frequency and approaches to 12 dB lower noise power gain beyond the corner frequency than the MASH modulator, thus has reduced phase noise at out-of-band. The improved effect can be easily understood in the following explanation. As the frequency approaches to a half of the comparison frequency ($z^{-1}\approx$-1), the noise transfer gain becomes about one at the frequency in the proposed modulator because the loop gain approaches zero beyond the corner frequency and a high frequency quantization noise appears directly at the output. Meanwhile, the noise transfer gain is 16 in a 4th-order MASH modulator. Fig. 3 shows the measured S/N of the single-bit 4th-order $\Delta\Sigma$

modulator with the comparison frequency of 9.84 MHz.

The modulator has the input range for normal operation that is limited to the maximum input of 50% of the full range (-0.5 < k/b_1 <0.5) even though it is capable of operation up to 67.5% range. If the input exceeds the limited input range, the on-chip overflow detector operates to reset all the accumulators to zero.

The fractional-N frequency synthesizer using the proposed modulator has some useful features, in addition to less sensitivity to the nonlinearity. First, it provides an exact frequency resolution as rational multiples of 10 kHz so that frequency error in cell phone applications can be minimized. It results from the fact that the achievable frequency resolution is 9.84 MHz / 62976, where 9.84 MHz is a comparison frequency. The modulus, 62976, can be easily realized by setting the feedback coefficient b_1 to 62976, while it needs considerable amounts of additional circuits in the MASH modulator. Second, hardware complexity can be largely reduced due to the following reasons. The inter-stage scaling coefficients (a_j) are set to be small integer power of 2, in order to avoid using multipliers and to implement them with simple bit-shift operations only. A tolerable lower bit truncation with an optimized dynamic range is done at each stage to allow integer arithmetic of the modulator. The coefficients (b_j) are implemented with very simple metal-connected multiplexers since the coefficients are constants. In all, the modulator requires approximately 65 bits of registers and 130 1-bit adders.

C. A Prescaler

For a low power and low noise frequency synthesizer, it is important to take an effort into a prescaler including a high-sensitive input buffer amplifier and high-speed dual-modulus ECL divider. The buffer amplifier [6] is designed using a two-stage differential amplifier to provide high sensitivity and to convert single-ended input from VCO to differential output. The first stage of the buffer amplifier uses active inductor load to compensate for the gain loss due to the reduction in the transconductance of a differential amplifier at high frequencies and, thus, to increase the −3 dB bandwidth of the amplifier even with low power consumption. The input sensitivity of the prescaler is designed in the range of −15 dBm to 0 dBm across the frequency range from 0.1 GHz to 2.5 GHz. In order to achieve the low power

consumption, power optimization is done in the prescaler with the criterion that the slower switching dividers should be biased at the lower currents. The signal swing level of the ECL logic in the prescaler is determined by trade-off between speed and noise margin, and is set to 400 mV. The prescaler has a quadruple modulus division ratio, 16/17/20/21 to cover wide frequency range.

D. PFD/Charge Pump and Bias Circuits

In a phase frequency detector with a charge pump, the PFD [6] uses a reset signal, generated by sensing the charge pump output current, to reset the up and down signals at the PFD output node and then to eliminate the dead-zone problem. For power saving, the charge pump uses dynamic biasing technique by a charge pump enable control that generates a gating signal responding to the two PFD inputs and makes it turn on only during a small time slot of the reference period in lock state. As additional feature of the charge pump, 16-level charge pump current can be programmed in a 50-μA step for easy tuning to a stable loop.

Bias currents generated by a proportional-to-absolute-temperature (PTAT) current generator and a band-gap reference circuit are used for biasing the prescaler to guarantee the operation over temperature from -40℃ to 85℃ and supply voltage range of 2.7-4.0 V.

III. EXPERIMENTAL RESULTS

The experiment was done in a 12 kHz bandwidth PLL loop in which an external 31 MHz/V VCO, a 3rd-order passive LPF, a 9.6 MHz comparison frequency instead of 9.84 MHz, and 450 μA charge pump current were used. The external LPF has one zero and three poles including two out-of-band poles.

Fig. 4 shows the measured VCO output spectrum at 2.11485 GHz (N.f=220.296875). The reference spurs are measured to be less than −85 dBc and no fractional spurs are observed in all frequency band from 900 MHz to 2.5 GHz.

The measured single-sideband (SSB) phase noise at 2.11485 GHz (N.f=220.296875) is shown in Fig. 5, including the phase noise for integer-N frequency synthesizer with the same comparison frequency for comparison. Out-of band phase noise at 1.2 MHz offset
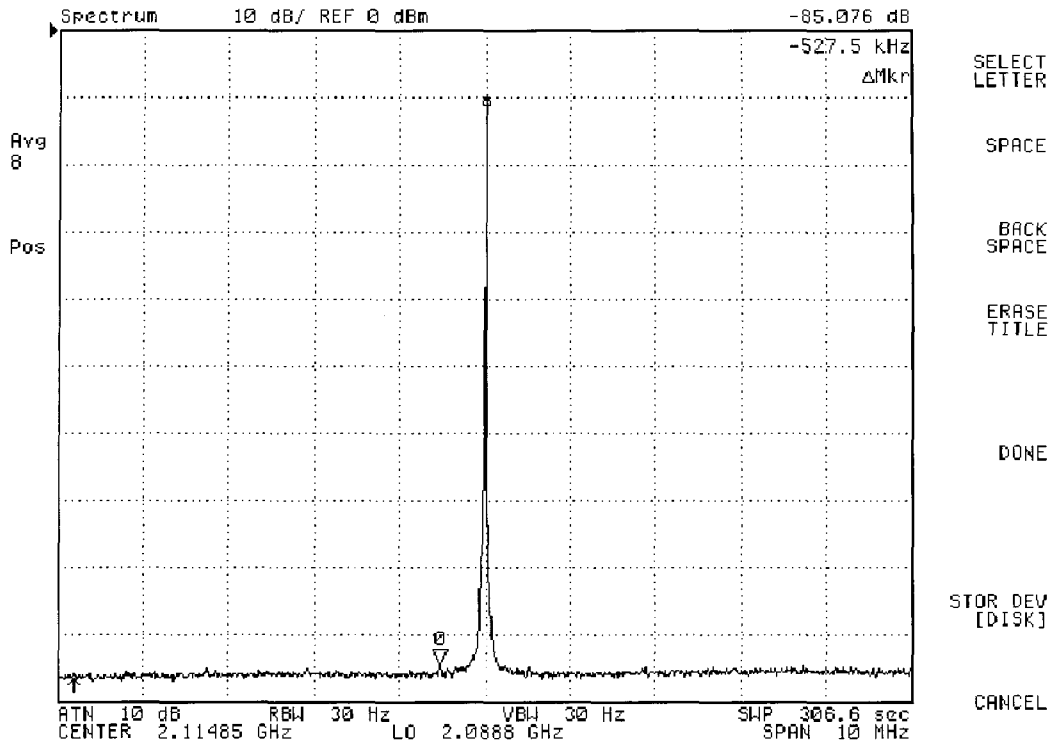
Spectrum   10 dB/ REF 0 dBm   -85.076 dB
                                                       -527.5 kHz
                                                       ΔMkr

Avg
8

Pos

ATN 10 dB   RBW 30 Hz   VBW 30 Hz   SWP 306.6 sec
CENTER 2.11485 GHz   LO 2.0888 GHz   SPAN 10 MHz

Fig. 4.   Measured VCO Spectrum (N.f= 220.296875).

Phase Noise   10 dB/ REF -60 dBc   -63.212 dBc
                                                       100 Hz

Avg
16   CARR 2.11485 GHz

ATN 0 dB   NATN 10 dB   NBW 1 Hz   SWP 7.372 sec
START 100 Hz   LO 2.0909 GHz   STOP 10 MHz

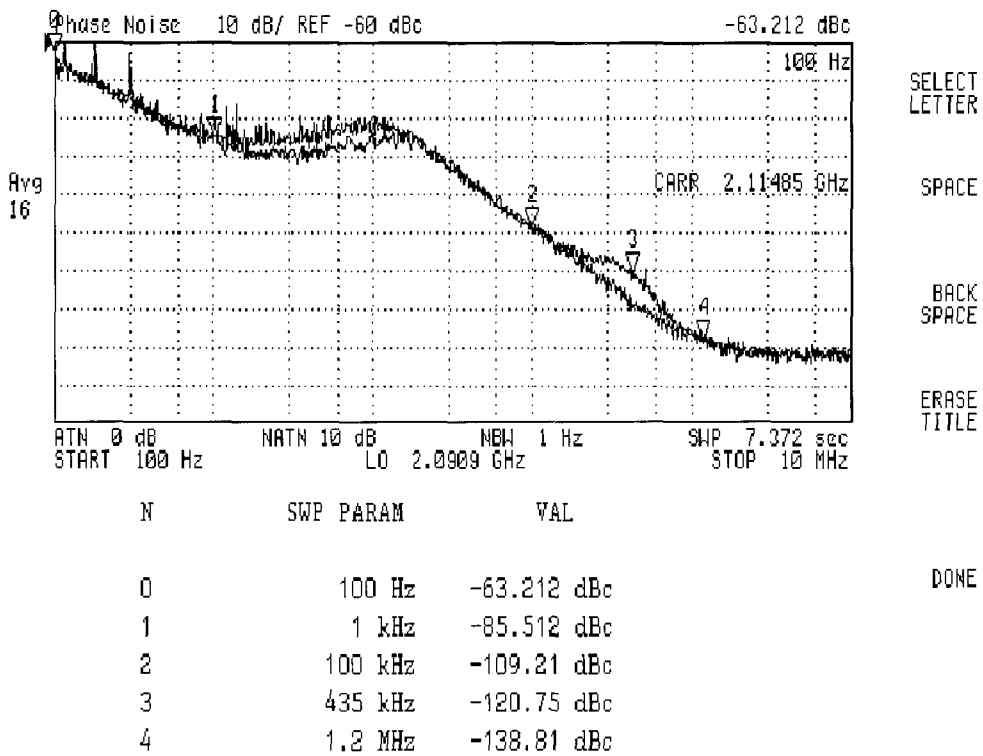| N	SWP PARAM	VAL
0	100 Hz	-63.212 dBc
1	1 kHz	-85.512 dBc
2	100 kHz	-109.21 dBc
3	435 kHz	-120.75 dBc
4	1.2 MHz	-138.81 dBc

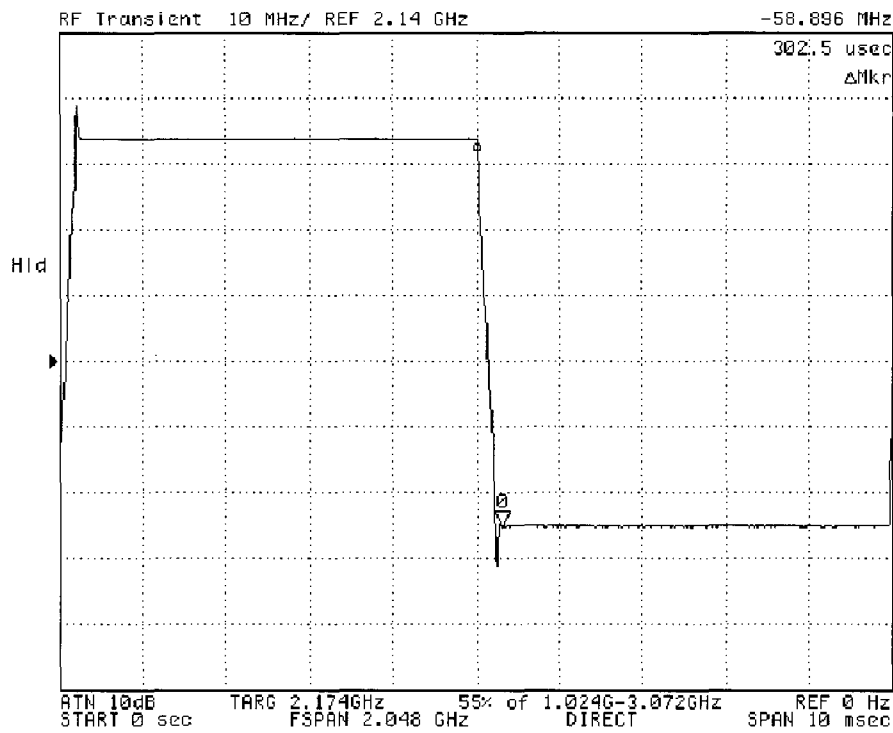Fig. 5.   Measured SSB Phase Noise at 2.11485 GHz.

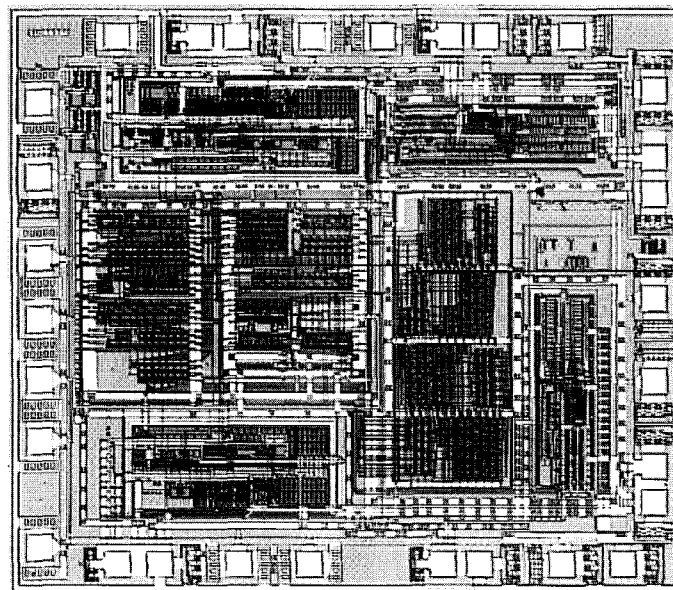**Fig. 6.** Measured Switching Time with a frequency step of 58.9 MHz: 302.5 μs.

Fig.7. Microphotograph of prototype with IF Integer-N frequency synthesizer.

is −138.8 dBc/Hz and in-band phase noise at 1 kHz offset is about −85.5 dBc/Hz.

Fig. 6 shows the switching time for a 59 MHz-step change and the measured lock time is about 303 μs.

The chip works at 2.5 GHz with < -15 dBm input sensitivity. The RF Fractional-N frequency synthesizer part consumes 6.0 mA at 3.0 V while the overall chip including the IF integer-N synthesizer consumes 7.5 mA. An internal band-gap reference guarantees a wide operation temperature range from -40℃ to 85℃ and

supply voltage range of 2.7-4.0 V. Measured performance, summarized in Table 1, meets the specifications for CDMA-2000 1X standard.

A microphotograph integrated with an IF integer-N frequency synthesizer, is shown in Fig. 7. The die area is 2100×2100 μm^2, including 140 μm scribe lane, of which the $\Delta \Sigma$ modulator occupies 420×1040 μm^2. The chip has been fabricated in a 0.5-μm 15-GHz f_t 3-metal BiCMOS process.

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Byeong-Ha Park received the B.S. degree in electronics engineering from Hanyang University, Seoul, Korea, in 1984, the M.S. and Ph.D. degrees in electrical engineering from Georgia Institute of Technology, Georgia, USA, in 1995 and 1997, respectively.

From 1983 to 1992, he was with Samsung Electronics, Ltd., Korea, working mainly on the development of analog video signal processing ICs and tuner ICs for video applications. From 1992 to 1996, he was with Georgia Institute of Technology, Georgia, in analog circuits group, focusing on CMOS radio frequency ICs and PLL-based frequency synthesizers. From 1996 and 1997, he was with Rockwell Semiconductor Systems (currently Conexant Systems), where he designed PLL-based frequency synthesizers, voltage-controlled oscillators, and RF ICs for wireless mobile phones such as CDMA and GSM. Currently, he is with Samsung Electronics, where he is in charge of designing RF/analog front-end ICs of wireless mobile applications such as CDMA, GSM, Bluetooth, and wireless LAN. His principal areas of professional interest include analog circuitry of all types, raging from low level building blocks to high frequency RF communications systems. His present research focus is on RF integrated circuit design.