2.45GHz CMOS Up-conversion Mixer & LO Buffer Design

Jin-Young Choi*, Sang-Gug Lee. Seok-Bong Hyun, Kyung-Hwan Park***, and Seong-Su Park*****

Abstract— **A 2.45GHz double-balanced modified Gilbert-type CMOS up-conversion mixer design is introduced, where the PMOS current-reuse bleeding technique is demonstrated to be efficient in improving conversion gain, linearity, and noise performance. An LO buffer is included in the mixer design to perform single-ended to differential conversion of the LO signal on chip. Simulation results of the design based on careful modeling of all active and passive components are examined to explain in detail about the characteristic improvement and degradation provided by the proposed design. Two kinds of chips were fabricated using a standard 0.35μm CMOS process, one of which is the mixer chip without the LO buffer and the other is the one with it. The measured characteristics of the fabricated chips are quite excellent in terms of conversion gain, linearity, and noise, and they are in close match to the simulation results, which demonstrates the adequacy of the modeling approach based on the macro models for all the active and passive devices used in the design. Above all the benefits provided by the current-reuse bleeding technique, the improvement in noise performance seems most valuable.**

Index Terms — **mixer, CMOS, bleeding, reuse, buffer**

Manuscript received January 16, 2002; revised March 12, 2002.

*School of Electrical, Electronics, and Computer Engineering, Hongik University, Jochiwon, Yongi Gun, Chungnam, 339-701, Korea
**School of Engineering, Information and Communications University, 58-4, Hwaam-dong, Yusong-gu, Daejon, 305-348, Korea
***ETRI-Microelectronics Technology Laboratory, 161 Gajong-dong, Yusong-gu, Daejon, 305-600, Korea
(e-mail : jychoi@www.hongik.ac.kr) Tel : +82-41-860-2548

I. INTRODUCTION

A basic function block of the radio frequency (RF) transceiver is the mixer, which converts the frequency of the input signal to the higher or lower frequency. Among the various mixer topologies, the double-balanced Gilbert-type mixer topology is preferred in mixer design since it suppresses the local oscillator (LO) signal at the output. Even though there have been many efforts to explain the operational mechanism involved and to improve the characteristics [1, 2, 3, 4], the operation of this important function block does not seem to be fully examined. And only a few of successful CMOS design examples based on this topology have been reported at the frequency range above 2GHz [4, 5], where more challenges are solicited for CMOS technology to prove its potential in higher frequency applications.

The double-balanced Gilbert-type CMOS mixer is basically composed of the input transconductance stage, the switching transistors, which operate in switching mode by differential LO signals to perform frequency conversion, and the mixer loads. In mixer design, the higher gain, higher linearity, lower noise and low power consumption are required, but it is not easy to achieve them simultaneously. Higher gain and better linearity can be achieved by increasing the bias current through the transconductance stage [2, 6], but power consumption can be excessive. Furthermore the larger current through the switching transistors can cause voltage headroom problems especially if resistive loads are used. Larger amount of current through the switching transistors also mandates large LO drive, which is desirable for more ideal switching but troublesome in the CMOS technology, since it is not easy to get the large enough

voltage swing at high LO frequency with reasonable power consumption.

Better techniques to improve conversion gain have been introduced, where some sort of current bleeding techniques are utilized [2, 3, 4]. With the current bleeding technique, the bias current through the transconductance stage can be increased without increasing the current through the switching transistors. While not affecting the transconductance of the transconductance stage, the bleeding relaxes the voltage headroom problem, and allows smaller LO drive voltage applied to the switching transistors because of improved switching efficiency, which helps to improve the conversion gain.

The gain can be improved further by the current-reuse bleeding technique [3], where the gates of the PMOS bleeding transistors are connected to the input together with the NMOS gates of the transconductance stage to enhance the transconductance of the transconductance stage. The PMOS transistors act not only as bleeding transistors but also as a part of input transconductance stage, and hence the bleeding current is effectively reused. (See Fig. 2 in section II.)

To drive the switching quad of the mixer, a differential LO signal is required. Single-ended to differential conversion of the LO signal can be done by external transformer, but it not only complicates the design with more external components but also mandates the use of a large LO drive due to the unavoidable loss. On-chip transformers can be utilized, but it is not easy to make them provide good performances and they produce even larger loss [7]. Therefore it is desirable to include a single-ended to differential LO buffer in the mixer design.

In this paper, a 2.45GHz double-balanced modified Gilbert-type CMOS up-conversion mixer design utilizing the current-reuse bleeding PMOS transistors is examined based on simulation and measurement results, which may provide design guidelines in applying this type of mixers both in up and down conversion. An LO buffer is included in the mixer design to perform single-ended to differential conversion of LO signal on chip.

In section II, the ideas behind the chosen mixer topology and the LO buffer topology are explained in terms of characteristic improvements. In section III, the characteristic changes of the mixer in gain, linearity and other important behaviors as a function of the current-bleeding ratio are discussed, and the simulated results of the proposed LO buffer are also discussed. Modeling efforts to increase the accuracy of simulations are briefly introduced. In section IV, the measurement results of the mixer chips with and without the LO buffer, which were fabricated utilizing a 0.35μm standard CMOS process, are given and compared to the simulation results. In section V, the results are summarized briefly.

II. Mixer Topology

Fig. 1 shows the block diagram of the designed up-conversion mixer chip. As shown in Fig. 1, IF, RF, and LO frequencies are assumed as 350MHz, 2.45GHz, and 2.1GHz, respectively, which are chosen in accordance with the Bluetooth specifications. The differential IF input is assumed.

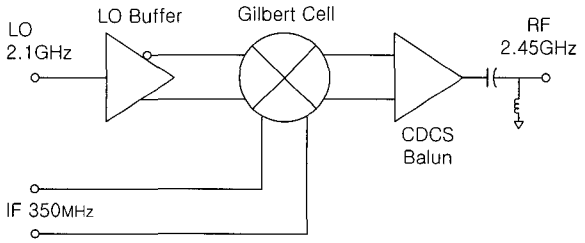


Fig. 1. Block diagram of the designed mixer chip.

Fig 2 shows the proposed double-balanced modified Gilbert-type CMOS up-conversion mixer excluding the LO buffer stage in Fig. 1. The cascode configuration of the transconductance stage is adopted to suppress the 2nd-order harmonic of the LO (2LO) signal at the mixer output since the higher output impedance of the transconductance stage helps to suppress the 2LO signal. This can be explained by the fact that the amplitude of 2LO at the source of the switching transistor is about the same as that of the applied LO signal as it forms a source follower and the amplitude of the 2LO at the drain of the switching transistor is proportional to the ratio of the load impedance to the output impedance of the transconductance stage.

In Fig. 2, the IF port is resistively matched to the 200Ω differential input at 350MHz, which was chosen in accordance with the IF filter characteristic. Resistive matching was chosen since the reactive matching

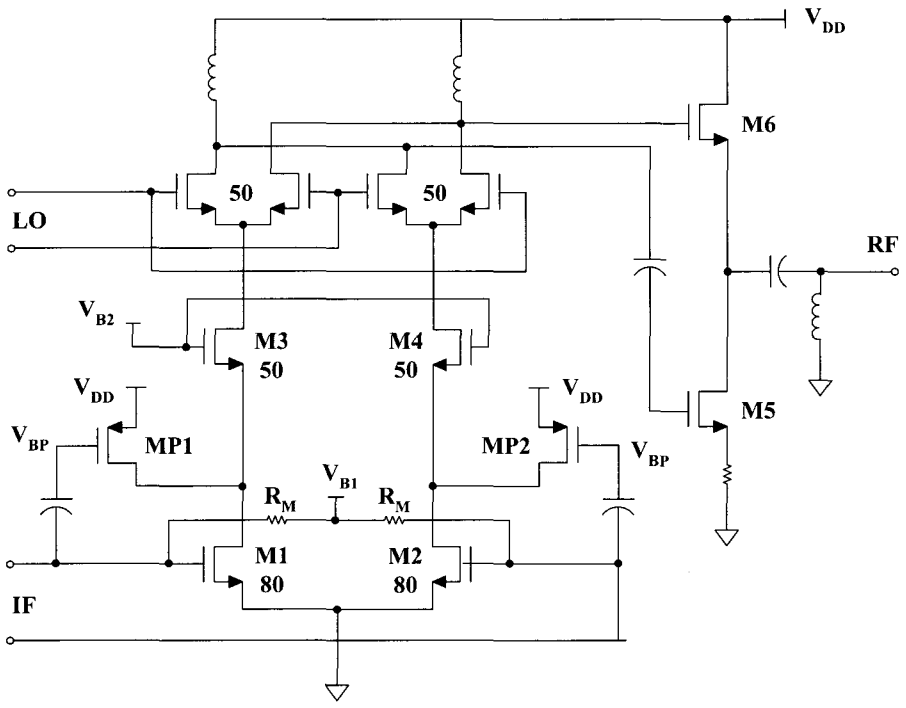


Fig. 2. Proposed up-conversion mixer topology including the output balun. (Bias circuits are not shown.) Numbers shown beside the transistors indicate the number of 5μm-width gate fingers.

requires too large L or C for on-chip matching and also the noise performance is not critical in the up-conversion mixer specification.

The source terminals of the transconductance stage are connected directly to the ground. The differential IF drive allows class AB operation of the transconductance stage, which helps to achieve higher conversion gain and linearity [8]. The on-chip inductors are used as loads to reduce headroom problems and to utilize the frequency tuning behavior at the mixer output. The 3-level on-chip inductors utilizing metal 2, 3, and 4 layers are used to reduce the chip area.

In Fig. 2, the PMOS transistors (M_{P1} and M_{P2}) are incorporated for the current-reuse bleeding [3] to improve the conversion gain. The PMOS transistors are biased separately and coupled capacitively with the NMOS transistors (M_1 and M_2). The current-reuse bleeding is also expected to improve the linearity since the effective dc current of the transconductance stage increases [6] because PMOS and NMOS transistors effectively form a single transistor.

In Fig. 2, the common-drain-common-source (CDCS) buffer balun stage, composed of M_5 and M_6, is adopted at the output stage to get the single-ended output, which is matched to the 50Ω RF load at 2.45GHz by the combination of the transistor transconductance, the on-chip capacitor, and the bond wire. To match the gain of the common-drain path to that of the common-source path, a series resistor is included at the source of M_5.

Since no special metal-insulator-metal (MIM) capacitor is available in the chosen process, the n-well accumulation-type MOS capacitors and the poly1-poly2 capacitors were used for on-chip coupling, bypass, and matching purpose. The poly2 resistors were used for biasing.

Fig. 3 shows the proposed single-ended-to-differential LO buffer topology. Basically it is a 3-stage differential amplifier. In the 1st stage, the single-ended-to differential conversion is performed, and the 2nd stage is inserted to improve the symmetry of the differential signal.

In the 1st and 2nd stages, we adopt the resistive loads to focus on getting the more symmetrical differential signal rather than the higher voltage gain. In the 3rd stage, the inductive loads are adopted to utilize the tuning capability and get large enough signal swing. The

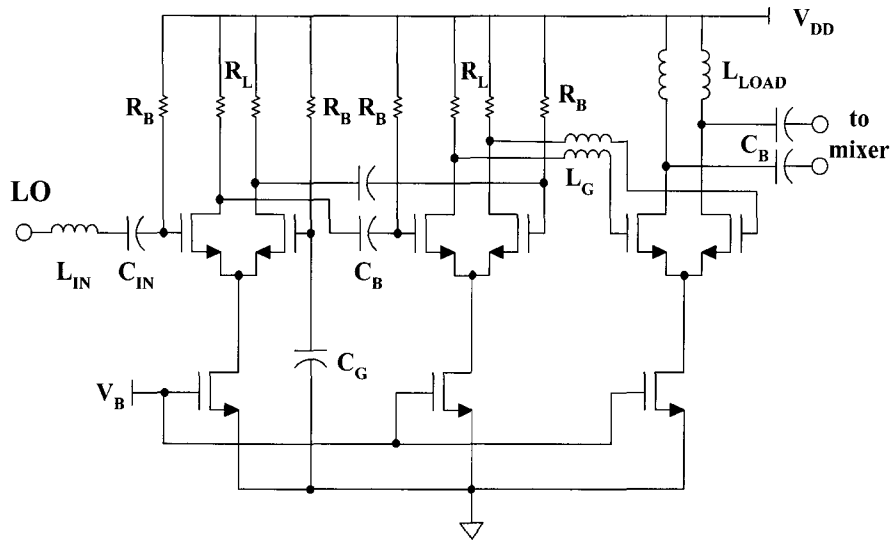


Fig. 3. Proposed single-ended-to-differential LO buffer topology.

series inductor L_G is inserted between the 2nd and the 3rd stages to perform gain boosting by introducing an additional pole near the LO frequency.

In Fig. 3, all the passive components are made on chip. L_{IN} and C_{IN} together with the bond wire form the impedance matching network, which transforms the input impedance value to 50Ω at 2.1GHz. C_{IN} also acts as a dc blocking capacitor. C_G is the bypass capacitor and C_B is the coupling capacitor. The n-well accumulation-type MOS capacitor has limitation in its use in that the potential of the poly1 node should be about 1V higher than the n-well node to keep the surface in accumulation. Therefore the poly1-poly2 capacitors are used for the coupling capacitors (C_B) in Fig. 3 since the voltage difference between the capacitor nodes is not large enough. Compared to the n-well capacitors, the poly1-poly2 capacitors have disadvantages in that they consume larger areas and the signal loss to the substrate through the poly1-substrate capacitance is larger.

III. Performance Evaluation

A. *Mixer characteristics*

As mentioned in the introduction, several papers concerning the mixer topologies incorporating the current bleeding and/or current reusing technique have been reported [1, 2, 3, 4], but the results have not been analyzed thoroughly. In this section, the proposed mixer performances are analyzed with the help of circuit simulations to characterize the benefits and drawbacks in adopting the current-reuse bleeding technique in mixer design.

Simulations on this work are based on the bsim3v3 model parameters of a standard 0.35μm CMOS process. The width of transistor fingers was chosen as 5μm to minimize the gate resistance. The measured cutoff frequency and maximum frequency of oscillation of the fabricated NMOS transistors were all about 25GHz. All the components including transistors, inductors, capacitors, resistors and pads have been previously fabricated using the same technology and carefully modeled as macro cells to fit the measured s-parameters up to 10GHz. The three in/out ports, V_{DD} and ground pads are assumed to be connected to the outside through the minimal bond wire, which was simply modeled by the series inductance and the resistance of 0.8nH/mm and 200mΩ/mm, respectively.

In Fig. 4, we compare the simulated characteristics of the bleeding mixer with and without current reusing. To examine the characteristics of the mixer itself, the LO port is assumed to be driven by an ideal differential signal with the amplitude of $0.6V_p$. The currents through the transconductance stage transistors M_1 and M_2 are about 6mA, and the CDCS output balun consumes 4.5mA of current at V_{DD}=3V. In Fig. 4, the bleeding ratio is defined as the ratio of the current through the bleeding PMOS transistors (M_{P1} and M_{P2}) to the current through

M_1 and M_2, and is varied by changing the PMOS size with a fixed gate bias. 0% represents the case where no bleeding PMOS transistor is used.

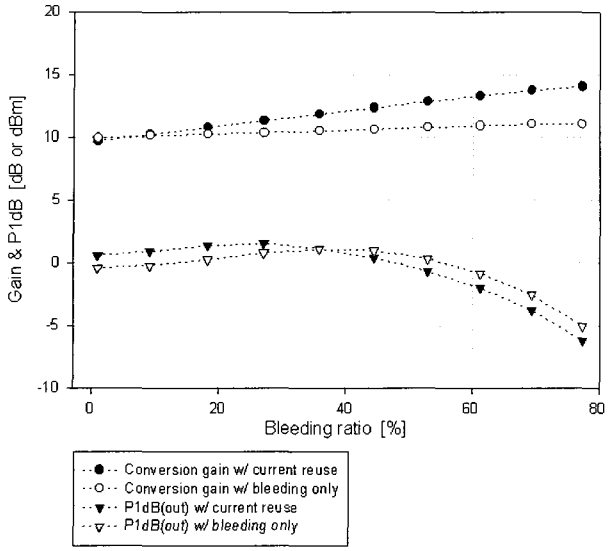


Fig. 4. Simulated conversion gain and output P_{1dB} characteristics with and without current reusing. IF= -30dBm, LO=0.6V_p (differential).

As can be seen in Fig. 4, the conversion gain with bleeding only improves in some extent as the bleeding ratio increases. The gain improvement is caused by the enhanced switching efficiency of the switching transistors with the reduced current by the bleeding, however it is weakened since there is a signal loss in the on-chip coupling capacitor between the gates of the PMOS and the NMOS transistors. The improvement in conversion gain with current reusing is very effective in Fig. 4, which is caused by the enhancement of transconductance with the increased reuse current.

In Fig. 4, linearity improves and then degrades with current-reuse bleeding, and it seems there exists some optimal condition for the bleeding ratio. When the bleeding current is about 30% of the drive current, the output P_{1dB} shows its maximum. The simple bleeding mixer without current reusing also shows similar behavior, but the maximum output P_{1dB} occurs at the higher bleeding ratio.

The linearity degradation had been monitored in the down-conversion mixer incorporating the current bleeding technique [4], however, detailed explanation for the mechanism has not been given. To figure out the mechanism involved in the linearity variation in Fig. 4, internal voltage and current variations have been monitored, and it turned out that the linearity characteristics in Fig. 4 involve two mechanisms.

Firstly, the linearity improves with more bleeding as the current through the switching transistors decreases. In this regime, the linearity is determined by voltage limiting, where the transistors in the common-gate stage and the switching transistors go out of the saturation region of operation as the amplitude of IF signal increases. Since the gate-source voltage required for the reduced dc current decreases with more bleeding, the required drain-source voltage to maintain the saturation region of operation diminishes. Therefore the output P_{1dB} improves as the bleeding ratio increases. When smaller transistors are used for the switching transistors to enhance the switching efficiency and hence to increase the conversion gain, the required gate-source voltage of the switching transistors increases and so does the drain-source voltage. In this case, the linearity at 0% bleeding ratio degrades, but the linearity improvement with bleeding is more prominent.

Secondly, the linearity degrades by current limiting as the bleeding ratio exceeds certain amount, as can be seen in Fig. 4. Since the bias current through the common-gate stage decreases monotonically with more bleeding, with excessive bleeding, the lower bound of current swing reaches zero faster. The drain current of the common-gate transistor experiences more severe distortion as the amplitude of IF signal increases. Therefore, in this aspect, the dc current through the common-gate transistor should be maintained large enough to extend the linearity above some specific level.

These two mechanisms counteract with each other, and result in best linearity when the bleeding current through PMOS transistor is about the 45% of the driving current in Fig. 4. When current reusing is incorporated, the transconductance increases by the added transconductance of the PMOS transistor, leading to higher current swing. And hence the current limiting occurs at lower bleeding ratio. Therefore, compared to the bleeding-only case, the resulting output P_{1dB} with current reusing is getting somewhat worse at higher bleeding ratio, as can be seen in Fig. 4.

In case of the non-cascoded structure, the initial improvement in linearity in Fig. 4 cannot be shown since

fewer transistors are stacked between supply voltage and ground, and hence the voltage headroom for each transistor is enough. In the non-cascoded case, the output P_{1dB} simply worsens noticeably above some bleeding ratio [4]. Note that even in the design with a non-cascoded structure, there can be a voltage-headroom problem if the design stacks more devices for any purpose, and then the improvement in the linearity with bleeding shown in Fig. 4 can be effective.

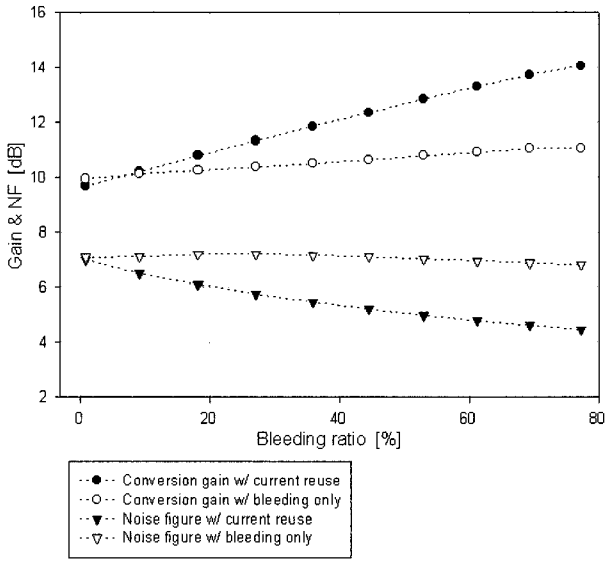


Fig. 5. Simulated conversion gain and noise figure characteristics with and without current reuse. IF= -30dBm, LO=0.6V_p (differential).

Fig. 5 shows the simulated conversion gain and the single-side-band (SSB) noise figure (NF) variations as a function of bleeding ratio when the amplitude of differential LO is 0.6V_p. In Fig. 5, the characteristics with and without current reusing are compared. Improvement in noise characteristic with current-reuse bleeding is clearly shown even though the NF value itself is somewhat lower than expected, which is the result of utilizing the inaccurate noise model defined in the simulator. The noise model includes thermal noise, drain channel noise, and flicker noise. The induced-gate noise model [9] is missing, but it was effectively incorporated through the gate resistance included in the transistor macro model, which matches well with the measured s-parameters of the transistor used. However we believe that the drain channel noise model in the simulator somewhat underestimates the noise generated in the short channel transistors we are using, since the noise coefficient used may be only good for long channel transistors [10].

To figure out the reasons concerning the improvement in noise figure, we have examined the output noise contribution of each component in the circuit. Note that noise figure can be defined as the ratio of the total output noise power to the output noise due to input source resistor. The noise characteristics can be improved with current bleeding by two mechanisms that occurs, one of which is the increased conversion gain and the other is more ideal switching of the switching transistors, both of which are available with smaller current flowing through switching transistors. The ideal switching tends to reduce noise generated in the switching transistors by reducing the amount of time that both transistors are on. This characteristic is confirmed by the fact that the drain-channel noise contribution of the switching transistors and the thermal noise contribution of the LO source resistor is reduced with increase in the bleeding ratio. As the conversion gain increases with more bleeding, the total output noise power increases since the noise components prior to the gain stage are multiplied by the increased gain, but the noise generated in the switching transistors decreases due to more ideal switching, and therefore the percentage output noise contribution of the input source resistor increases to result in the reduced noise figure. However in Fig. 5, the noise figure with bleeding only does not improve with more bleeding. This is because as the size of PMOS transistor is increased, the amount of noise generated by the PMOS bleeding transistor itself increases and the noise figure may degrade since the noise contribution of the current source connected in parallel with the signal path becomes larger as the transconductance of the current source increases [11]. As a result, the reduction in the noise figure with bleeding only is not effective as shown in Fig. 5.

The improvement in noise figure when adopting the current-reuse technique is mainly due to gain improvement provided by the additional transconductance of the PMOS bleeding transistor. The percentage output noise contribution of the input source increases to result in the reduced noise figure.

To reduce the noise contribution of the bleeding current source, a design that incorporates common-mode

current injection through the LC resonance tank has been suggested [2]. However the LC resonator may not be effective as it blocks the noise component only at one frequency. The image and high frequency noise contributions still exist. However with the current-reuse bleeding technique suggested in this work, the noise contribution of the PMOS bleeding transistor can be minimized as it becomes a part of the transconductance stage.

The simulated mixer characteristics without the LO buffer are compared to the measured ones in section IV.

B. *LO buffer characteristics*

The object in the design of the LO buffer in Fig. 3 was simply to make it generate the well-balanced differential signal with large enough swing. The designed LO buffer consumes 14.58mA of current at V_{DD}=3V. As mentioned in section II, due to the signal losses in the poly1-poly2 coupling capacitors in Fig. 3, the power consumption is relatively large, which can be reduced if MIM capacitors are available. There is a voltage loss rather than a gain in the 1st stage, which is intended so as to get the better-balanced differential signal. The gain is obtained in the 2nd and 3rd stages and the overall voltage gain in the buffer ends up to 11.27dB. The distributions of the voltage gain are summarized in Table 1. As shown in the Table 1, the gain mismatch is quite good as 0.26dB. However the phase mismatch is about 22degree, which is excessive and tends to generate the mismatch problem in the mixer core to produce a larger LO component at the mixer output. The design with the gain boosting inductor helps to increase the voltage gain by 2dB and also helps to get slightly better symmetry compared to the design without it.

The output components of the mixer incorporating the LO buffer was monitored by simulations as a function of LO power with the IF power of -30dBm at 350MHz. With -10dBm of the LO power, the conversion power gain is comparable to the design in section III-A with the ideal $0.6V_p$ differential LO drive. However, when incorporating the LO buffer, the LO component at the output port is increased to -46.8dBm, which is acceptable but relatively large due to the asymmetry present in the differential LO signal. Comparison between the simulated and measured data is given in section IV.

Table 1. Distributions of the voltage gain in the LO buffer.

Stage or component	Voltage gain[dB]	
	Left	Right
Input matching circuit	4.83	
1st stage	-0.24	-2.63
2nd stage including boosting inductor	4.59	7.22
3rd stage	8.59	9.13
Coupling capacitors	-6.5	-7.02
Total	11.27	11.53

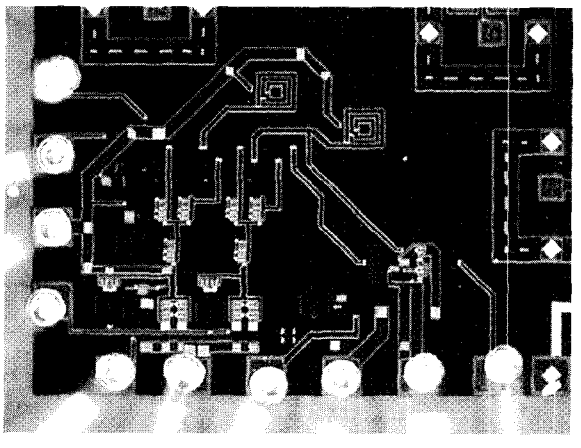


Fig. 6. Photograph of the fabricated chip without the LO buffer.

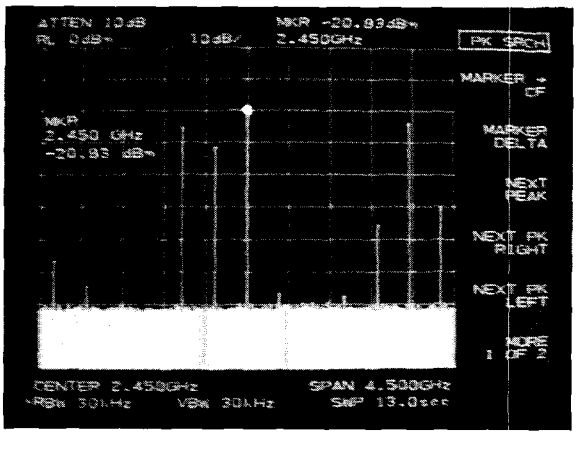


Fig. 7. Measured output frequency spectrum of the up-conversion mixer. IF= -30dBm at 350MHz.

IV. Measurement Results

A. *Mixer without the LO buffer*

The mixer circuit shown in Fig. 2 utilizing the current-

Table 2. Comparison between simulated and measured data of the mixer without the LO buffer.

Specifications		Simulation	Measurement
Conditons		IF= -30dBm at 350MHz, f_{LO} = 2.1GHz, f_{RF}= 2.45GHz, V_{DD} = 3V	
		LO=0.6V_p (differential)	LO=2dBm (single-ended),
DC current	Mixer Core	11.94mA	12mA
	Output Balun	4.52mA	4.9mA
Conversion gain		11.85dB	12.17dB
P_{1dB}(out)		1.15dB	0.5dB
OIP3		10dBm	10.3dBm
SSB noise figure		5.5dB	7.1dB
LO power at the output		-102dBm	-30.5dBm
Image power at 1.75GHz		-25.1dBm	-24.5dBm

reuse bleeding technique was fabricated using a standard 0.35μm 4-metel and 2-poly CMOS process. The PMOS transistor size was chosen as 200μm to set the bleeding ratio of 35%, which seems to provide good performances in terms of conversion gain, linearity, and noise. The photograph of the chip is given in Fig. 6. The chip size is about 1.14×0.84mm^2.

Fig. 7 shows the measured output frequency spectrum of the fabricated up-conversion mixer without the LO buffer when the IF power is -30dBm at 350MHz. The LO power is 2dBm at 2.1GHz, which needs to be large since the LO signal is applied through an external transformer balun with about 2dB of loss. For the IF input port also, an external transformer balun was used to generate the required differential signals. The measurement includes external transformer balun and cable losses. The bias current through each of the transconductance stage was about 6mA, and the output balun consumed 4.9mA of current at V_{DD}=3V. The measured signal reflections at the IF port and RF port were -14.5dB and -19.5dB, respectively. The marker (white spot) positioned at 2.45GHz in Fig. 7 indicates the RF power of -20.83dBm. Considering about 3dB power loss through the external IF balun and the cables, the conversion gain is about 12.2dB. The frequency component just left to the RF component is the LO leakage to the output, and the one left to it is the image power at 1.75GHz. The frequency components on the right hand side of Fig. 7 are the 2nd harmonics of the components mentioned above. The simulated and measured characteristics are compared in Table 2.

In Table 2, the measured characteristics are in a good agreement with the simulated results, and the overall performance of the fabricated up-conversion mixer is respectable. Compared to the simulated results which assumes an ideal differential LO drive, the LO component at the output is quite large with relatively large chip-to-chip variation. This indicates that asymmetry problem certainly exists in the fabricated mixer core, whose layout is in lack of transistor matching by not adopting mismatch-free structures such as a quad structure [12]. It is worth while to mention that the coupling between RF signal and LO signal is possibly not the main reason for the large LO leakage since the LO port is pretty well isolated from RF port in the layout.

As shown in Table 2, the measured SSB noise figure is 7.1dB at 2.45GHz. The noise figure of 7.1dB is a respectable value especially when considering that the mixer incorporates the resistive matching at the IF input. This is truly the most important benefit we can get by adopting the current-reuse bleeding technique, as explained concerning the result in Fig. 5. The disagreement between the measurement and the

simulation is expected due to the inaccuracy in the MOS transistor noise model inside the simulator.

B. *Mixer incorporating the LO buffer*

The photograph of the mixer chip incorporating the LO buffer is given in Fig. 8. The chip size is about $1.14\times1.14mm^2$.

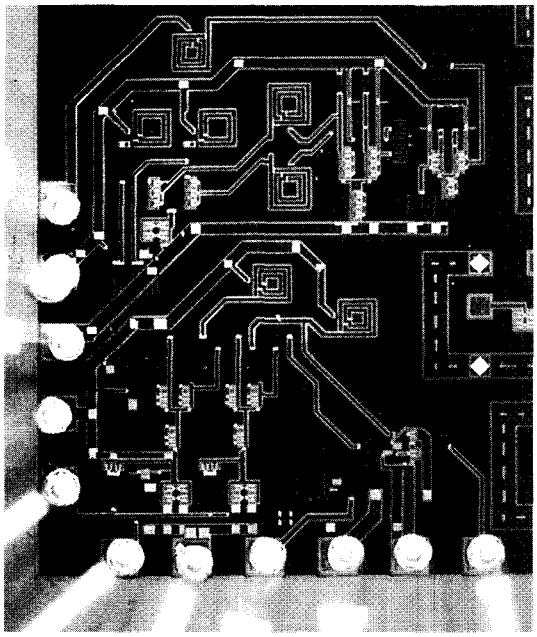


Fig. 8. Photograph of the fabricated chip incorporating the LO buffer.

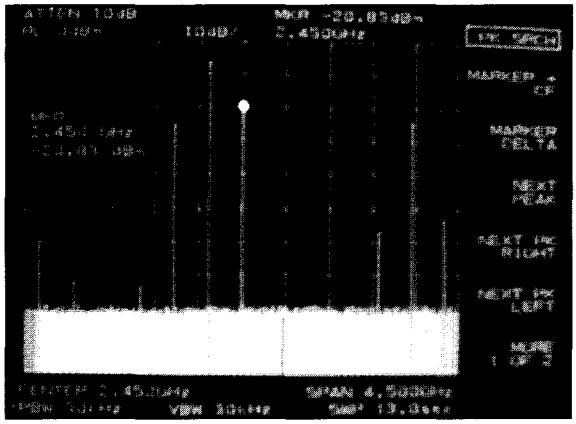


Fig. 9. Measured output frequency spectrum of the up-conversion mixer incorporating the LO buffer. IF= -30dBm at 350MHz, LO= -10dBm at 2.1GHz.

Fig. 9 shows the measured output frequency spectrum of the fabricated up-conversion mixer incorporating the LO buffer when the IF power is -30dBm at 350MHz and the LO power is -10dBm at 2.1GHz. Only for the IF port, an external transformer balun was used to generate the required differential input signals. The measurement includes external transformer balun and cable losses. The bias current through each of the transconductance stage was about 6mA, and the output balun consumed 5mA of current at V_{DD}=3V. The measured signal reflections at the IF port, RF port, and LO port are -13.5dB, –16.6dB, and –8.7dB, respectively. The marker (white spot) positioned at 2.45GHz in Fig. 9 indicates the RF power of -20.83dBm. Considering the power loss through the external IF balun and the cables, the conversion gain is about 12.2dB. The simulated and measured characteristics are compared in Table 3.

In Table 3, the measured characteristics are in a good agreement with the simulated results except the LO feedthrough to the output port. LO component at the output is very large, which seems to be firstly caused by the asymmetry present in the differential LO signal generated in the LO buffer as mentioned concerning the results of Table 1. However the resulting value is quite larger than the simulated value in Table 3, which again indicates that asymmetry problem exists in the mixer core. More efforts in making the layout symmetrical seem to be essential to make the chip more immune to the causes of asymmetry in the fabricating process.

V. SUMMARY

A 2.45GHz double-balanced modified Gilbert-type CMOS up-conversion mixer design utilizing the current-reuse bleeding technique has been examined based on simulations to demonstrate advantages achievable when adopting the current-reuse bleeding technique in the mixer design. A single-ended to differential LO buffer is included in the mixer design, which is aimed to provide a well-balanced differential LO signal to the mixer on chip.

Two kinds of chips were fabricated using a standard 0.35μm CMOS process, one of which is the mixer chip without the LO buffer and the other is the one incorporating the LO buffer. The measured mixer performance is quite excellent in terms of conversion gain, linearity, and noise, and the measured characteristics are in close match to the simulations, which demonstrates the adequacy of the modeling

Table 3. C omparison between simulated & measured data of the mixer incorporating the LO buffer.

Specifications		Simulation	Measurement
Conditons		IF= -30dBm at 350MHz, f_{RF}= 2.45GHz, V_{DD} = 3V LO= -10dBm at 2.1GHz	
DC current	Mixer Core	16.46mA	17mA
	LO buffer	14.58mA	14.2mA
Conversion gain		12.29dB	12.2dB
P_{1dB}(out)		1.77dB	0.7dB
OIP3		10dBm	11.5dBm
SSB noise figure		5.6dB	7.5dB
LO power at the output		-46.8dBm	-5.6dBm
Image power at 1.75GHz		-24.94dBm	-24.4dBm

approach based on the macro models for all the active and passive devices used in the design. The asymmetry problem has been monitored in the measured characteristics, which requests more careful layout of the chip.

The current-reuse bleeding technique certainly seems to provide benefits in terms of gain, linearity and noise characteristics. In the mixer incorporating the current-reuse bleeding technique, the conversion gain improves monotonically with more bleeding, which is the benefit provided both by the current bleeding and the current reusing. The current bleeding improves linearity when the voltage headroom is not enough. However with excessive bleeding, linearity degrades by the current-limiting phenomena, which defines the optimal bleeding ratio. Noise performance improves monotonically with more bleeding, which is also the benefit provided both by the current bleeding and the current reusing. Above all the benefits provided, the improvement in noise performance seems most valuable. There is trade-offs in determining the current-reuse bleeding ratio, which implies that the benefits can be optimized to get most out of it.

REFERENCES

[1] A. N. Karanicolas, , "A 2.7-V 900-MHz CMOS LNA and Mixer," IEEE J. Solid-State Circuits, vol. 31, pp. 1939-1944, Dec. 1996

[2] L. A. MacEachern and T. Manku, "A charge-injection method for Gilbert cell biasing," *in Proc. IEEE Canadian Conf.*, 1998, pp. 365-368.

[3] S.-G. Lee and J.-K. Choi, "Current-reuse bleeding mixer," *Electronics Letters*, vol. 36, pp. 1-2, Apr. 2000.

[4] T.-P. Liu and E. Westerwick, , "5-GHz CMOS radio transceiver front-end chipset," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1927-1933, Dec. 2000.

[5] K. Runge, D. Pehlke, and B. Schiffer, "On-chip matched 5.2GHz differential integrated mixer with RF and LO preamplification, fabricated in 0.35μm CMOS technology," *Electronics Letters*, vol. 35, pp. 1545-1546, Sept. 1999.

[6] K. L. Fong and R. G. Meyer, "High-frequency nonlinearity analysis of common-emitter and differential-pair transconductance stages," *IEEE J. Solid-State Circuits*, vol. 33, pp. 548-555, Apr. 1998.

[7] J. R. Long, "Monolithic transformers for Silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1368-1382, Sept. 2000.

[8] K. L. Fong, C. Dennis, and R. G. Meyer, "A class AB monolithic mixer for 900-MHz applications," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1166-1172, Aug. 1997.

[9] A. van der Ziel, Noise in Solid State Devices and Circuits. New York: John Wiley & Sons, 1986.

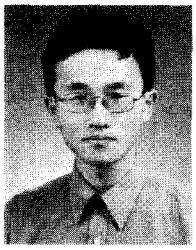
[10] P. A. Layman and S. G. Chamberlain, "A compact thermal noise model for the investigation of soft error rates in MOS VLSI digital circuits," *IEEE J. Solid-State Circuits*, vol. 24, pp. 79-89, Feb. 1989.

[11] B. Razavi, Design of Analog CMOS Integrated Circuits. New York: McGraw-Hill, 2000.

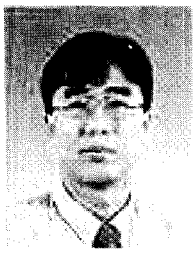
[12] J. Bastos, M. Steyaert, B. Graindourze, and W. Sansen, "Matching of MOS transistors with different layout styles," in Proc. *IEEE International Conf. Microelectronic Test Structures*, vol. 9, pp. 17-18, Mar. 1996.

Jin-Young Choi was born in Seoul, Korea in 1956. He received the B.S. degree in electrical engineering from the Seoul National University, Korea, in 1979, and the M.S. and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1986 and 1991, respectively. His doctorial research was in the area of thin-film SOI MOSFET device modeling. In 1991, he joined Samsung Electronics Memory Division, Korea, where he was engaged in high-speed SRAM development. In 1992, he moved to the Hongik University, Jochiwon, Korea, where he is now an associate professor. His recent research interests include the high-frequency modeling of CMOS devices, CMOS RF circuit design, and analysis & design for ESD protection.

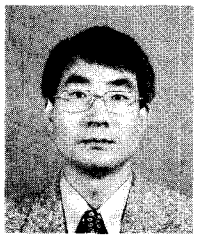
Sang-Gug Lee was born in Gyungnam, Korea in 1958. He received the B.S. degree in electronic engineering from the Gyungbook National University, Korea, in 1981, and the M.S. and Ph.D. degrees in electrical engineering from the University of Florida, Gainesville, in 1989 and 1992, respectively. In 1992, he joined Harris Semiconductor, Melbourne, Florida, USA, where he was engaged in silicon-based RF IC designs. From 1995 to 1998, he was with Handong University, Pohang, Korea, as an assistant professor in the school of computer and electrical engineering. Since 1998, he is with Information and Communications University, Daejon, Korea, where he is now an associate professor. His research interests include the silicon technology-based (BJT, BiCMOS, CMOS, and SiGe BICMOS) RF IC designs such as LNA, mixer, oscillator, power amp, etc. He is also active in the high-speed IC designs for the optical communication such as the TIA, driver amp, limiting amp, CDR, mux/demux, etc.



Seok-Bong Hyun was born in Suwon, Korea, in 1969. He received the B.S., M.S., and Ph.D. degrees in physics from the Korea Advanced Institute of Science and Technology (KAIST) in 1991, 1993, and 1998, respectively. In 1999 he joined Electronics and Telecommunications Research Institute (ETRI), Korea, where he has been involved in the design of RF and analog integrated circuits for short-range wireless communication systems and Bluetooth. His research interests include analog and mixed IC design for wireless communications.



Kyung-Hwan Park received the B.S degree in electronic engineering from Hanyang University, Korea, in 1991, and the M.S degree, Ph. D degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Korea, in 1993 and 1997, respectively. He worked for DACOM R&D Center as a senior engineer from 1997 to 2000. He executed some projects on B-WLL, DBS antenna & system, Smart Antenna, and VDSL. In 2001, he joined Advanced Micro-Electronic Research Laboratory in Electronics and Telecommunications Research Institute (ETRI), Korea. His current research interests include RF IC design based on CMOS process and RF module design for short- range communication terminal.



Seong-Su Park received the B.S. degree in metallurgy from Yonsei University, Korea, in 1984, and the M.S. and Ph.D. degrees in materials science from the Korea Advanced Institute of Science and Technology (KAIST), Korea, in 1986 and 1992, respectively. In 1993, he joined Electrical and Telecommunications Research Institute (ETRI), Korea, as a Senior Research Staff. Until the middle of 1998, he had involved in the area of MMIC design and optical device packaging. Since 1999, he has been in charge of the development of Bluetooth chips and system.