Single-ended Differential RF Circuit Topologies Utilizing Complementary MOS Devices

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Abstract— Single-ended differential RF circuit topologies fully utilizing complementary characteristics of both NMOS and PMOS are proposed, which have inherent advantage of both single-ended and differential circuits. Using this concept, we propose a CCPP (Complementary CMOS parallel push-pull) amplifier which has single-ended input/output with differential amplifying characteristics, leading to more than 30 dB improvement on IIP_2. In addition, complementary resistive mixer is also proposed, which provides not only differential IF outputs from single-ended RF input, but much better linearity as well as isolation characteristics. Experimental results using 0.35 μm CMOS process show that, compared with conventional NMOS resistive mixer, the proposed mixer shows 15 dB better LO-to-IF isolation, 4.6 dB better IIP_2, and 4.5 dB better IIP_3 performances.

Index Terms — Single-ended, differential, RF, complementary, MOS

I. INTRODUCTION

By virtue of continuous advances in fabrication technologies [1] – [3], CMOS is now ready to proceed to

the sea of wireless RF market. Recent reports on CMOS RF circuits and systems show that it has performances good enough to be applied to 1 – 3 GHz applications such as GSM (Global System for Mobile communications), PCS (Personal Communication Services), bluetooth, GPS (Global Positioning System), etc. Moreover, there are some reports even for 5 GHz band WLAN (Wireless Local Area Network) application [4] – [6].

Until now, the leading application for wireless communication market has been for mobile cellular phones, which are GSM for Europe and CDMA for U.S. and Korea, etc. In these systems, mobile users communicate with base stations, which are several kilometers away from them. Because of signal attenuation, power amplifiers and LNA (low noise amplifier) specifications are relatively tight for these applications. Large output power (~ 28 dBm for CDMA and ~ 33dBm for GSM) with high linearity is required for power amplifier, and low noise figure (less than 1.5 dB typically) is required for LNA. Low power consumption is mandatory for both receiver and transmitter. Because of these tight specifications, transceiver IC designers have been choosing the best-performance fabrication technology, such as GaAs MESFET, Si bipolar, and SiGe bipolar rather than low cost technology like CMOS.

However, the situations for short-range communication such as bluetooth, HomeRF and WLAN are definitely different from that of cellular phone. In these applications, a mobile user communicates with indoor devices, and the distances between them are normally within 100 m. In other words, much higher noise figure for receiver and much lower output power for transmitter can be accepted. For these applications, low cost and low power consumption are the first consideration factors.

CMOS is attractive for these short-range communication in that it is much cheaper than SiGe or GaAs process, and moreover, it can integrate digital modem part together in one-chip. This is the reason why most bluetooth and WLAN transceiver chips are designed and fabricated with CMOS process nowadays [4], [5], [7]. Moreover, there is some effort to integrate full CMOS RF transceiver even for high performance mobile cellular application like GSM [8]. In summary, CMOS RF IC's are now rushing out of academic institutes into battlefield of RF markets.

Together with process technology selection, system architecture is another issue for recent wireless receiver design. Until now, almost all of wireless receiver adopted heterodyne architecture because of its high sensitivity and selectivity. Heterodyne is the best-performance architecture at the cost of large-volume, high-power, high-cost SAW filters and image rejection filters. Recently, IC designers have investigated direct conversion receiver (DCR) and low-IF architectures to remove large-volume and high-cost filters, some of which show performance comparable to that of conventional ones [9] – [13].

In DCR and low-IF receivers, because IF is DC or near DC, not only odd order nonlinearity, but also even order nonlinearity has significant effects on total nonlinearity [14]. In other words, IP_2 (second order intercept point) as much as IP_3 (third order intercept point) is an important specification for a receiver, and because of this reason, most direct conversion and low-IF receiver adopt fully differential signal structure, where even order nonlinearities can be canceled out. However, it requires large-volume baluns, which connect single-ended antenna to differential input stage in front RF circuits. Usually, baluns are implemented using large-size off-chip inductors and capacitors, which results in narrow band characteristics. Although wideband baluns can be implemented using resistors, it is not desirable because these low-Q elements increase signal loss and noise figure. These problems will be discussed further in section II and III.

In this paper, we propose several amplifier and mixer circuits for wireless RF application that fully utilize CMOS devices, i.e., both NMOS and PMOS. The complementary nature of these circuits inherently provides single-ended differential signal processing

capability, alleviating the use of baluns, or, differential signal generating circuits. One good example is the static CMOS digital logic circuit, which is undoubtedly one of best complementary circuits ever invented. Push-pull drive amplifier consisting of NMOS and PMOS source followers is another example.

Previous efforts to fully utilize CMOS RF circuits will be reviewed in Sec. II. Sec III describes characteristic features of complementary circuits specifically for RF applications, followed by some amplifier and mixer application examples in Sec. IV. Sec. V demonstrates experimental results for the proposed circuits in Sec. IV, followed by conclusion.

II. REVIEW OF PREVIOUS WORKS

As mentioned above, there have been many efforts on RF building blocks [15], [16], receivers [17], [18] and transceivers [19], [20], implemented using recent CMOS technologies. However, most of the RF core circuits consist only of NMOS, and PMOS is just used in bias circuits. This is quite in contrast with digital world where full utilization of complementary characteristics of CMOS leads to extremely low power and high-speed digital circuits and systems. High speed is due to shorter gate length and low parasitics, and low power is mainly due to complementary characteristics of NMOS and PMOS.

As mentioned above, in RF world, there are many technologies such as BJT, HBT, MESFET, HFET, etc., competing with each other. Among these, CMOS is the only viable technology in providing true complementary performance at RF, that is, although PMOS has lower ft and fmax than NMOS, the values are still well above 10 GHz [1], and that is enough to be used in 1 ~ 3 GHz application. In other words, complementary characteristics of NMOS and PMOS can indeed be fully utilized in RF core circuits without significant RF performance degradation.

Actually, there were several efforts to use PMOS as RF core circuit element. For example, PMOS cross-coupled pair that generates negative resistance for VCO was used to utilize its low phase noise characteristics [21]. They obtained phase noise of –128.5 dBc/Hz at 600 kHz offset from 2.05 GHz center frequency.

The use of both NMOS and PMOS was first adopted in VCO [22-25], where negative resistance generation circuits consisting of NMOS cross-coupled pair stacked with PMOS cross-coupled pair rather than NMOS-only or PMOS-only pair can lead to less power consumption. According to the analysis in [25], complementary and symmetric characteristics of NMOS and PMOS gives additional benefit of suppressing phase noise of RF oscillator. This is a good example of the use of complementary characteristics of NMOS and PMOS in RF analog circuit. Other examples include the power amplifier circuits [26] - [28], where PMOS is used as an active load to replace large size inductor load.

III. SINGLE-ENDED DIFFERENTIAL RF SIGNAL PROCESSING METHODS USING COMPLEMENTARY DEVICES

In analog/digital circuits, signal lines are constructed with either single-ended or differential. Single-ended topology has advantages of simpler structure, smaller DC power consumption, lower noise figure, etc. On the other hand, differential topology provides inherent immunity to signal interference, as well as generates much less electromagnetic interference signal. Moreover, by virtue of symmetrical characteristics, it can eliminate even-order distortions. The former characteristics is important in integrating various mixed mode circuit blocks in one chip, and in implementing mixer which requires high isolation among RF, LO, and IF ports. The latter feature is important in implementing amplifier or mixer that require even order suppression. As discussed earlier, modern direct conversion receiver has stringent specification on 2nd order non-linearity because of its DC offset problem. Moreover, in power-efficient class B or class AB mode operation, single ended structure has a problem that the signal could be clamped which results in generation of large amount of harmonic components. Thus differential circuits are quite preferred.

One of the obstacles for differential scheme is that baluns are required to convert single-ended signal to differential inputs. Generally, baluns are large and heavy, difficult to integrate on chip in the case of passive implementation. In active version, it requires DC power consumption as well as its accuracy is not as good as

passive ones. Therefore, in current RF applications, differential core is integrated on-chip, and passive baluns are implemented on PCB using discrete passive elements, which are large and heavy. Passive baluns also require more time and labor in mass production.
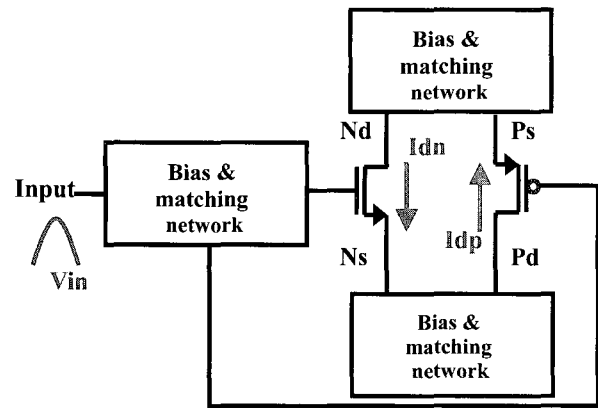

Fig. 1. Schematic of the generic single-ended differential RF circuits using complementary devices.

In this paper, we show that, by using NMOS and PMOS connected as complementary fashion, single-ended differential RF signal processing is possible, which has advantages of both single-ended and differential schemes. Fig. 1 shows the generic schematic of single-ended differential circuit topology using complementary devices. In this figure, though input signal is tied together at the gates of NMOS and PMOS, core is operating as differential mode because of complementary action of NMOS and PMOS. When the outputs at drain nodes of NMOS and PMOS are tied together, we can obtain single-ended output, because they have the same phase. The situation is the same when both source nodes are used as output ports. In these cases, input is single-ended, core operates as differential, and output is single-ended again. However, it is interesting to note that differential (out-of-phase) outputs can also be obtained by selecting Nd and Ps, and vice versa. In summary, by selecting in-phase nodes as outputs, it is possible to implement single-ended differential amplifier, which eliminates even order distortion without input and output baluns. On the other hand, by selecting out-of-phase outputs, it is possible to implement a mixer which has single-ended input and differential output.

Generally, drain current of MOSFET is expressed by

(a)

(b)

(c)
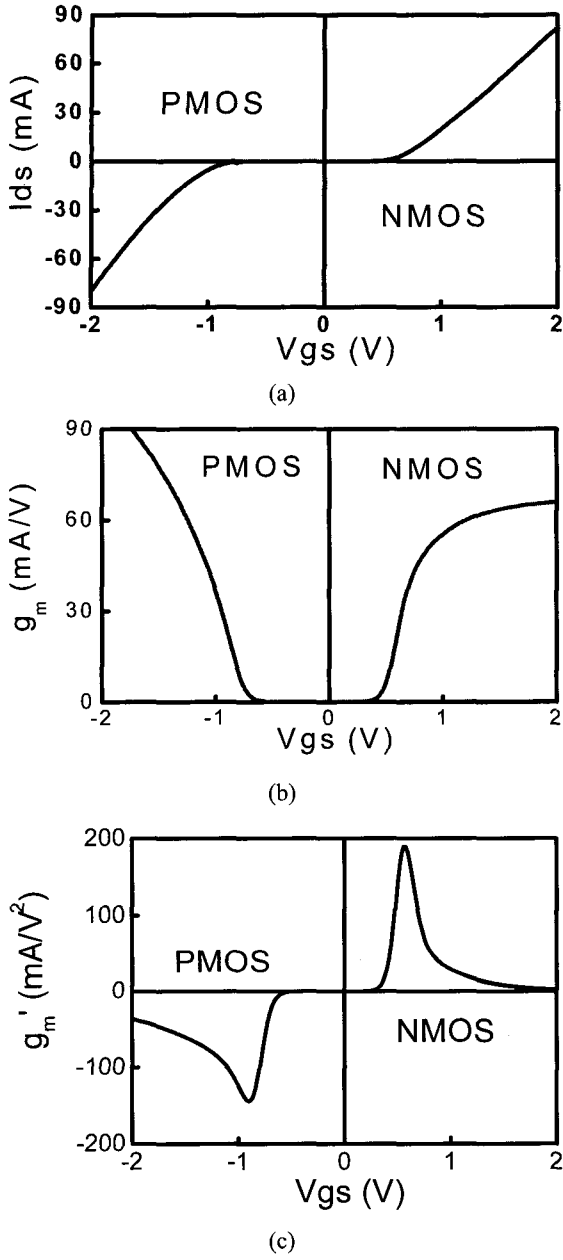
Fig. 2. Simulated DC characteristic of 300 μm/0.35 μm NMOS and 900 μm/0.35 μm PMOS FETs. (a) drain current, (b) transconductance, g_m and (c) $g_m' = \partial g_m / \partial V_{gs}$.

$$i_{DS} = I_{ds} + g_m v_{gs} + \frac{1}{2!} g_m' v_{gs}^2 + \frac{1}{3!} g_m'' v_{gs}^3 + \cdots \qquad (1)$$

Nonlinear characteristic of CMOS RF circuit is dominated by g_m nonlinearity [29] – [31], and second order nonlinearity is mainly due to g_m', which is the derivative of g_m with respect to v_{gs}. Because g_m' of NMOS and PMOS have opposite sign [32], by

combining them properly, it is possible to suppress 2nd order nonlinearity significantly, which enhances IP_2 of LNA's and mixers.

In summary, complementary characteristics of NMOS and PMOS makes it possible to implement single-ended input and output LNA with high IP_2, and single-ended input, differential output mixer with high IP_2. For direct conversion receiver, this front-end architecture is highly preferable because it connects single-ended antenna to differential baseband blocks without any balun with high IP_2 performance.

In section IV, the implementation of RF amplifier and mixer examples designed using the basic concept developed in this section will be given.

IV. High IP_2 Amplifier and Differential Mixer Circuits using Complementary Characteristic of Cmos

Fig. 2 shows simulation results of I_{ds}, g_m and g_m' of typical 0.35 μm NMOS and PMOS. W/L's are 300 μm/0.35 μm and 900 μm/0.35 μm for NMOS and PMOS, respectively. As shown in the figure, g_m' of NMOS and PMOS has opposite signs. Note that if we adjust the gate bias voltages for NMOS and PMOS so that, when they are combined together in such a way that negative g_m' values of PMOS can cancel out the positive g_m' values of NMOS, significantly higher IP_2 is expected. Fig. 3 shows AC equivalent circuit schematic of NMOS common source amplifier and CCPP (Complementary CMOS parallel push-pull) one which was invented on the basis of this concept [32]-[33]. IIP_2 performances of two topologies are simulated using ADS and the results are shown in Fig 4. Simulation is done at RF frequencies of 899.5 MHz and 900.5 MHz for NMOS V_{gs} of 0.8 V and V_{dd} of 3 V. As shown in Fig. 4, for the given V_{gs} of NMOS, there are two PMOS V_{gs} points, where IIP_2 peaks are obtained. Note that these are exactly the points where negative values of g_m' of PMOS cancel out the positive g_m' values of NMOS. One is at V_{gs} of around - 0.7 V. In this region, because PMOS operates in subthreshold regime, no additional current is needed to boost up the IP_2 value. However, because of parasitic loss of off-state PMOS, gain of the amplifier is decreased as shown in Fig. 4 (a). Another peak is
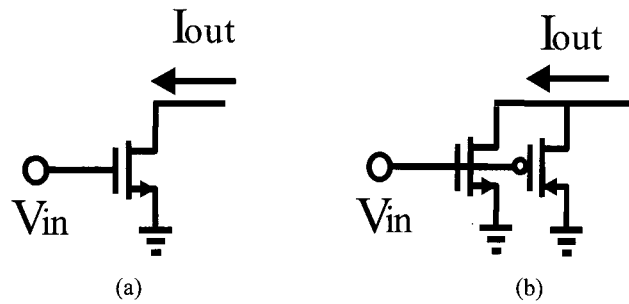
Fig. 3. AC equivalent circuits for (a) NMOS common source amplifier and (b) CCPP (Complementary CMOS parallel push-pull) amplifier [32].
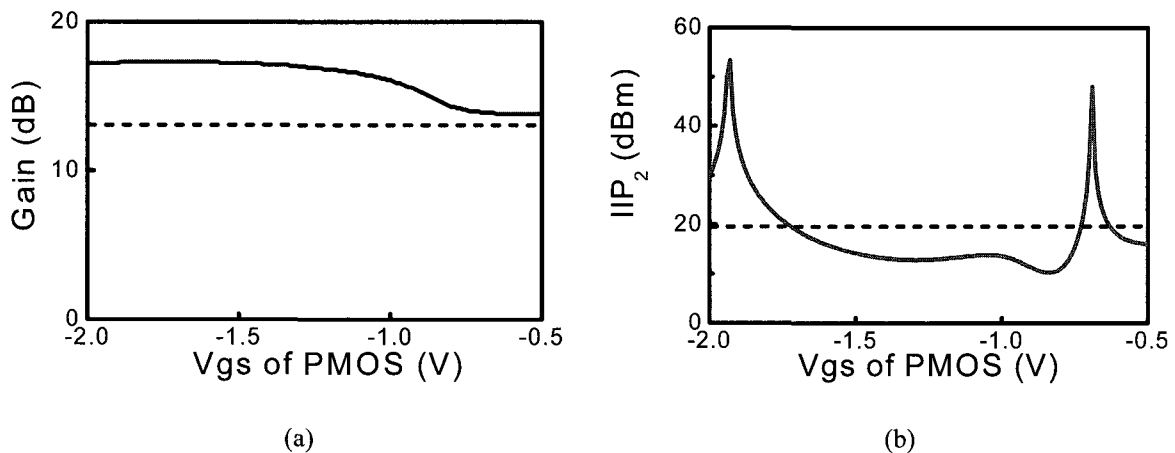
Fig. 4. Simulated (a) gain and (b) IIP_2 vs. PMOS bias voltage. Solid and dashed lines are for CCPP and NMOS common source amplifier, respectively.

obtained at PMOS V_{gs} of around -1.9 V. At this bias, PMOS operates as an amplifying element like NMOS. Thus, IIP_2 can be increased with higher gain as shown in Fig. 4 (a).

In summary, CCPP amplifier has single-ended input and output with differential amplifying characteristics. There are two PMOS gate bias points where IMD_2 (second order intermodulation distortion) components are canceled out and IIP_2 values are boosted up significantly. It is shown that with proper size PMOS and optimal bias circuits, it is possible to enhance peak IIP_2 by amount of more than 30 dB. Considering, however, margin against process and temperature variation, we can say that about 10 dB improvement in IIP_2 can be obtained in general.

Now let us apply the concept developed in the section III to resistive mixer. Fig. 5 shows conventional unbalanced single-ended resistive mixer and its operation principle. M1 is operating in linear region,

being turned on and off by LO signal. RF input is connected to drain of M1, and IF output is extracted from drain of M1. Assuming LO signal as large switching signal, output waveform can be drawn as in Fig. 5 (c). When LO signal turns off the switch transistor M1, RF signal appears at the drain node of M1. Although this passive mixer has the advantage that it is highly linear because of linear region operation, it has some problems with being used in modern direct conversion receivers. First of all, isolations among RF, LO and IF ports are poor. In direct conversion receiver, LO-to-RF isolation is critically important because of DC offset and LO emission problems. Additionally, because LO signal is much larger than RF and IF signal, LO signal should be attenuated sufficiently at IF port to prevent following stages from being saturated. Lastly, because IF or baseband blocks prefer to use differential signal structure rather than single-ended, this simple resistive mixer needs some modifications.
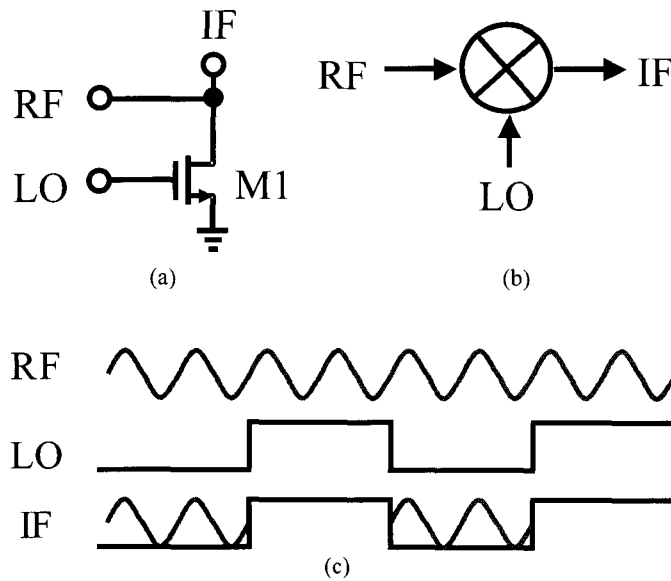
Fig. 5.   (a) schematic, (b) symbol, and (c) waveforms for unbalanced single-ended NMOS resistive mixer.
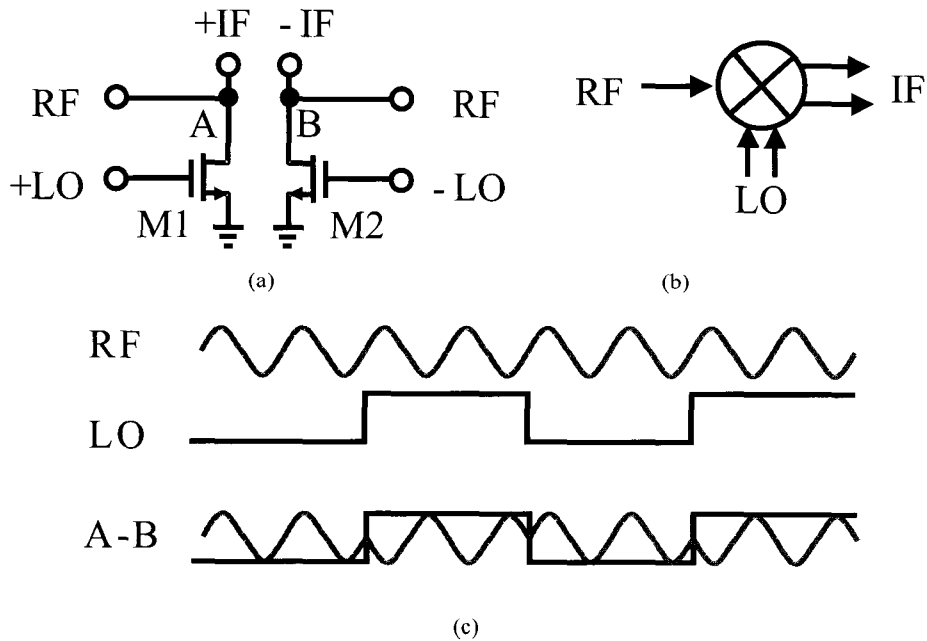

Fig. 6.   (a) schematic, (b) symbol, and (c) waveforms for single-balanced differential NMOS resistive mixer [34].

Fig. 6 shows single-balanced differential version of passive resistive mixer [34]. In this structure, differential LO input signals are connected to gates of M1 and M2, differential IF outputs are extracted from the respective drains of M1 and M2. The signal waveforms at nodes A and B are shown in Fig. 6 (c). At node A, RF signal appears during the first half cycle of LO as explained in Fig. 5. Similarly, at node B, RF signal appears during the second half cycle of LO signal. By selecting nodes A and B differentially, we can obtain IF signal as shown in Fig. 6 (c). Because RF power is transmitted to drain nodes during full cycle of LO, conversion loss is smaller than the case of Fig. 5. However, because both LO and IF signals are taken as differential, large LO signals appear at IF ports as shown in Fig. 6 (c). This is well-known inherent problem of single balanced mixer. This problem can greatly be alleviated by using complementary characteristic of NMOS and PMOS.
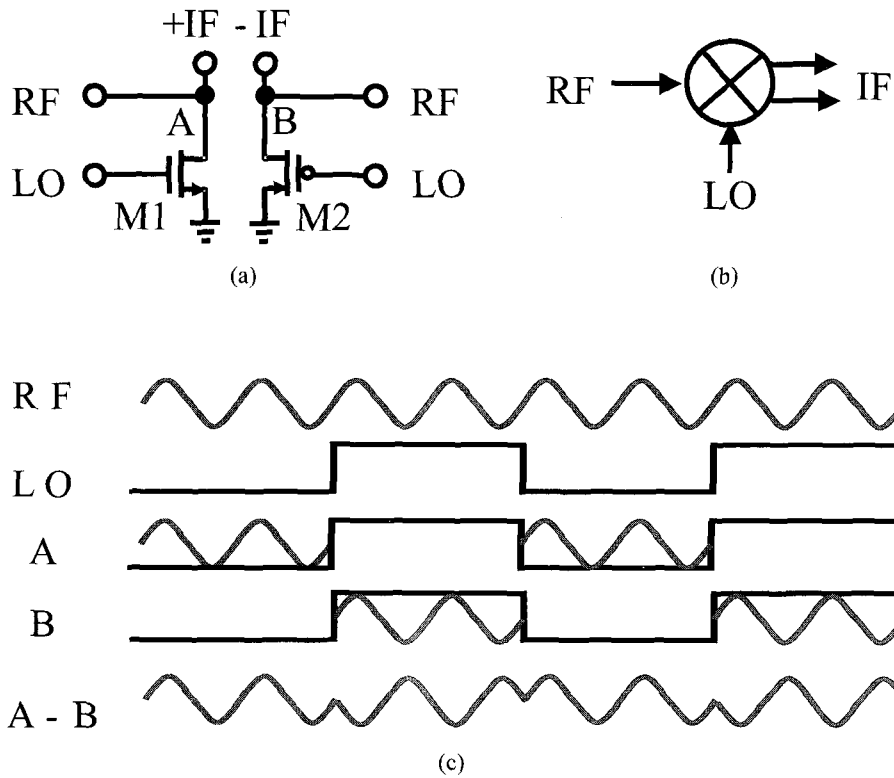
Fig. 7. (a) schematic, (b) symbol, and (c) waveforms for unbalanced complementary resistive mixer.

Table 1. Performance comparison of 4 types of passive mixers.

	Unbalanced NMOS	Single-balanced NMOS	Unbalanced Complementary	Single-balanced Complementary
DC Power Consumption	0	0	0	0
Conversion Loss	poor	medium	medium	medium
IIP_2	medium	good	good	good
IIP_3	medium	good	good	good
LO-to-IF Isolation	poor	poor	good	excellent
LO-to-RF Isolation	poor	good	poor	good
Device matching	excellent	excellent	medium	medium

Fig. 7 (a) shows AC equivalent circuit schematic of complementary unbalanced resistive mixer. This structure has advantage of availability of differential IF from single-ended RF and LO as shown in the figure. Note here that, although LO signal is single-ended, NMOS and PMOS operate differentially by virtue of complementary action as shown in Fig. 7 (c). Therefore, this structure has advantages that, although LO signal is single-ended, LO signal is greatly suppressed at IF output. Note, however, common mode LO signals still
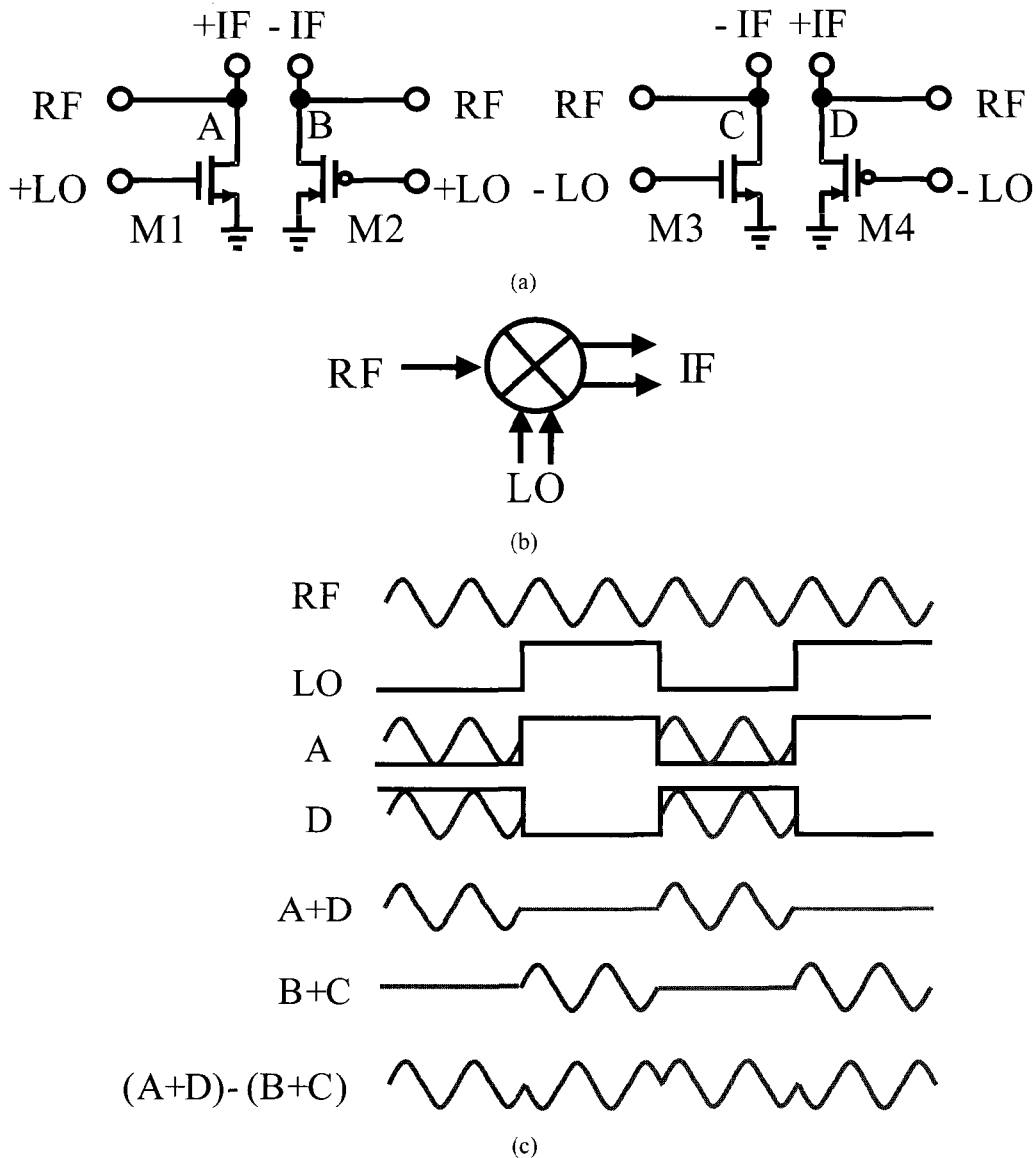
Fig. 8.   (a) schematic, (b) symbol, and (c) waveforms for single-balanced complementary resistive mixer.

exist at nodes A and B, which can be removed at differential IF output. In summary, complementary characteristic eliminates the need of differential LO signals and LO interference can be removed at differential IF ports.

Note that, however, because nodes A and B are tied at RF frequency, LO-to-RF isolation is still poor. Another potential problem is that, although differential LO does not appear at IF, large common mode LO signal still exists, which can possibly saturate the following stages.

These problems can greatly be alleviated by using complementary single-balanced passive mixer as shown

in Fig. 8. In the figure, another NMOS (M3) – PMOS (M4) pair is added, whose gates are connected to – LO signal. As shown in Fig. 8 (c), common mode LO signals can also be completely eliminated by connecting nodes A and D, and B and C. Because RF port is symmetrical about + LO and –LO ports, there is no LO signal leakage at RF port, either.

Table 1 compares the performance of four types of passive mixers, which can be summarized as follows. Single balanced complementary passive mixer using single-ended RF and differential LO signals, is very attractive because it provides differential IF signal with
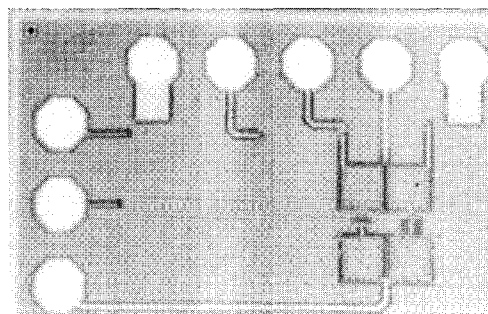
Table 2. Experimentally measured performance summaries for conventional unbalanced resistive mixer and unbalanced complementary resistive mixer fabricated using 0.35 μm CMOS process.

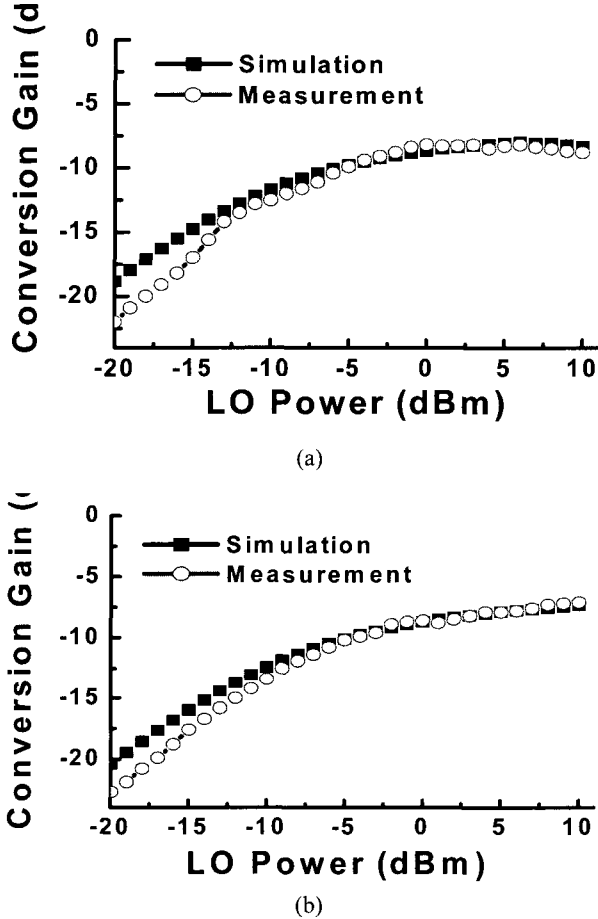|	Conventional unbalanced mixer	Unbalanced complementary mixer
DC Power Consumption	0	0
LO input power	4 dBm	4 dBm
Conversion loss	8.5 dB	7.9 dB
IIP_2	42.4 dBm	47 dBm
IIP_3	11.5 dBm	16 dBm
NF (simulation)	8.3 dB	8 dB
LO-IF isolation	25 dB	40 dB
LO-RF isolation	21 dB	17 dB
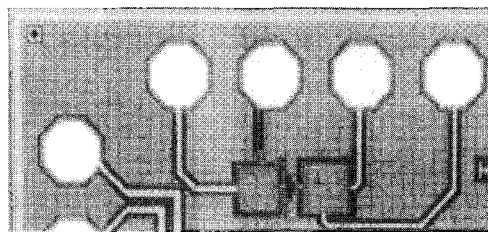
(a)

(b)

Fig. 9. Micrograph of (a) conventional unbalanced NMOS resistive mixer and (b) unbalanced complementary resistive mixer fabricated using 0.35μm CMOS process.

sufficient suppression of LO signal at both of IF and RF ports. In addition, it provides inherent advantage of high linearity due to linear region operation of MOSFETs. We think this is a very promising mixer topology to be used in all types of direct conversion and low-IF receivers, which requires both high even order linearity and high isolation among LO, RF and IF ports.

V. FABRICATION AND MEASUREMENTS

Conventional unbalanced mixer (Fig. 5) and proposed unbalanced complementary mixer (Fig. 7) prototype circuits were fabricated using only CMOS in 0.35 μm, 3-layer metal SiGe BiCMOS process and the performances are compared. The die area of the conventional

unbalanced mixer and proposed mixer is 0.47 mm ×
0.207 mm and 0.677 mm × 0.423 mm, respectively. To
obtain symmetrical characteristics, the size of NMOS
and PMOS is chosen as 100 μm/0.35 μm(W/L) and 350
μm/0.35 μm(W/L), respectively. The chip micrographs
are shown in Fig. 9.

(a)

(b)

Fig. 10. Measured conversion gain vs. LO power for (a)
conventional unbalanced NMOS resistive mixer and (b)
unbalanced complementary resistive mixer.

Fig. 10 compares the simulated and measured
conversion gain vs. LO power for the conventional
unbalanced mixer in (a) and the unbalanced
complementary mixer in (b), respectively. As seen in Fig.
10, the conversion gain of the proposed unbalanced
mixer is similar to that of the conventional unbalanced
mixer. However, as LO power increases and the
switching operation becomes more efficient, the
conversion gain of the unbalanced complementary mixer
becomes higher than that of the conventional unbalanced
mixer, as expected.

(a)

(b)
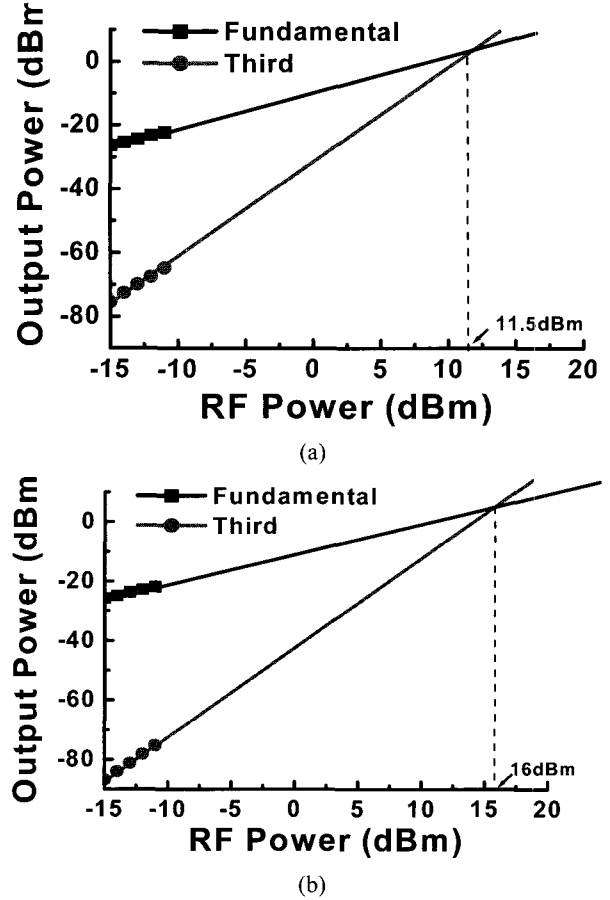
Fig. 11. IIP$_3$ measurement plots for (a) conventional
unbalanced NMOS resistive mixer and (b) unbalanced
complementary mixer.

Fig. 11 shows IIP$_3$ measurement of the conventional
unbalanced mixer in (a) and those of the proposed
unbalanced mixer in (b) measured with two tones at 2.1
GHz and 2.101 GHz at LO input power of 4 dBm. IIP$_3$
of the proposed unbalanced mixer is 4.5 dB higher than
that of the conventional unbalanced mixer at the same
LO input power. While the LO-to-RF isolation and LO-
to-IF isolation of conventional unbalanced mixer are 21
dB and 25 dB, those of the proposed unbalanced mixer
are 17 dB and 40 dB, respectively. Table 2 summarizes
the measured results. As expected, LO-to-IF isolation
improves drastically from 25 dB to 40 dB, while LO-to-
RF isolation is still poor (Table I). As was shown in Fig.
8, we could increase LO-to-RF isolation by using single
balanced structure.

VI. CONCLUSIONS

We propose several RF circuit topologies which fully

utilize complementary characteristics of NMOS and PMOS. Firstly, we introduce CCPP amplifier which has single-ended input/output and differential amplifying characteristics, leading to more than 30 dB improvement on IIP_2. In addition, complementary resistive mixer is also proposed, which not only provides differential IF from single-ended RF, but much better linearity as well as isolation characteristics. Experimental results using 0.35 μm CMOS process show that the proposed mixer has 15 dB better LO-to-IF isolation, 4.6 dB better IIP_2, and 4.5 dB better IIP_3 characteristics, compared with conventional NMOS mixer. This proposed circuit topologies are expected to be a viable choice for integration of RF circuit in a single chip.

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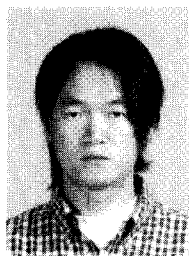
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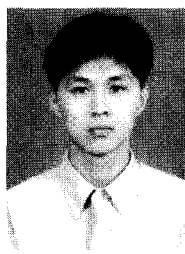
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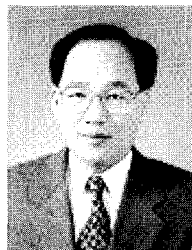
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