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Gate CD Control for Memory Chip using Total Process Proximity Based Correction Method

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In this study, we investigated mask errors, photo errors with attenuated phase shift mask and off-axis illumination, and etch errors in dry etch conditions. We propose that total process proximity correction (TPPC), a concept merging every process step error correction, is essential in a lithography process when minimum critical dimension (CD) is smaller than the wavelength of radiation. A correction rule table was experimentally obtained applying TPPC concept. Process capability of controlling gate CD in DRAM fabrication should be improved by this method.

OCIS codes : 110.3650, 110.5220.

I. INTRODUCTION

Several optical enhancement techniques such as high numerical aperture (NA), modified illumination, phase shift mask, optical proximity correction (OPC), and process proximity correction, have been introduced very successfully to extend the lifetime of current lithography technology [1]. Bottom anti-reflective coating (BARC) has become commercialized to overcome wafer topology. All the technologies mentioned above are closely related to CD (critical dimension) control [2-4]. Gate CD control has become a critical issue in recent VLSI circuits as minimum feature size drops below the wavelength of radiation. Gates with various sizes and pitches should be formed precisely to function correctly according to their original characteristics (Fig. 1). This means that specification of gate CD must be controlled within 10 % of minimum line width. Fig. 2 represents V_{th} (threshold voltage) characteristics vs. gate length of MOSFET. Distribution of gate CD without TPPC was broader, and some values are found to be out of specification.

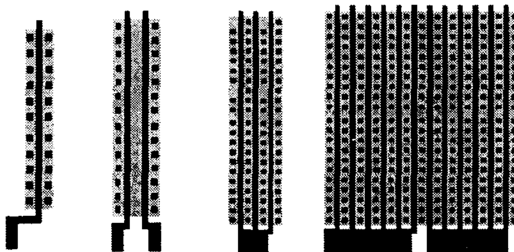

FIG. 1. Overview of gate layer. There are CD difference issues between sparse and dense patterns.

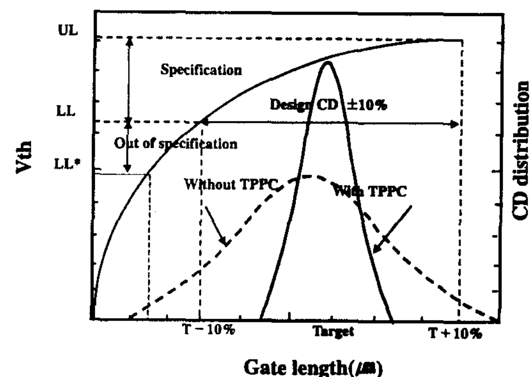

FIG. 2. V_{th} vs. gate length difference between the process with TPPC and that without TPPC is represented by the distribution curves of gate CD.

CD variation by process errors not only degrades device performance but also becomes the main cause of inferior goods. Thus, it is required to correct process errors to control gate CD within the specification. We can define process capability constant (Cp) in the lithography process as follows to control the degree of correction statistically [5,6],

C_p = Design Tolerance / Process Capability
= Range of Line Width Specification
/ [3σ (Iso.) + 3σ (L/S) + Δ(Prox.)]

where 3σ (Iso.) is line width variation of isolated lines, 3σ (L/S) is that of lines and spaces. These variation include those of intra- and interfield, chip to chip, wafer to wafer, and lot to lot. The line width specification is 20 % of the minimum line width, and Δ (Prox.) is maximum OPE (optical proximity effects) value. If we set control specification as 3σ, C_p equals 1 meaning 2700 parts per million (PPM) inferior goods. $C_p = 2$ realizes 3.4 PPM inferior goods when specification is controlled within $\pm 6\sigma$. Therefore, it is essential to adopt TPPC to improve device performance and product yield. In this study, we investigated process proximity effects in mask fabrication, optical proximity effects in resist patterning, and loading effects in the etch process.

II. PROCESS PROXIMITY EFFECTS

1. Process proximity effect in mask fabrication

Process proximity effect (PPE) in mask fabrication is generated by unwanted electron scattering of the electron beam and appears as a form of mask CD errors. There are several methods to correct the process proximity effect such as E-beam dose modulation, pattern biasing, ghost pattern, software, etc. Even by compensating the process proximity effect, complete correction of mask CD errors is difficult. Only a partial correction is possible. We investigated mask CD errors and the result is shown in Fig. 3. Mask CD errors differ depending on the pattern density as represented. However, the non-linearity of the mask CD

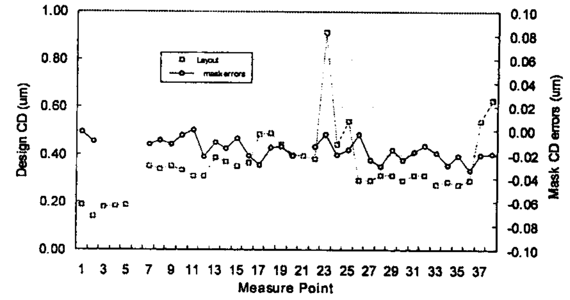

FIG. 3. Mask CD errors vs. design CD of pitch for various CDs. Process proximity effects are shown during E-beam writing on mask.

error is becoming a serious problem as the design rule shrinks to sub quarter micron scale. The isolated pattern CD is smaller than the designed CD because positive resist and electron scattering were used in the mask fabrication process.

2. Optical proximity effect

Optical proximity effect (OPE) is generated by diffraction or interference of light through optical the imaging system. OPE causes CD difference and degradation of pattern fidelity like edge rounding or tip shrinkage. To name a few, lens aberration, mask characteristics, resist performance, illumination condition, wafer topology and substrate reflectivity are the parameters that affect OPE. An experiment was designed to analyze OPE as described in Table 1. Cross-sectional view of substrate structure is displayed in Fig. 4. Experimental results in Fig. 5 clearly shows that isolated line increases nonlinearly development inspection (DI) CD error (DI CD - mask CD) of the isolated line increases nonlinearly as mask CD increases, the trend of which is different from that of line and space. The optical proximity effect was larger in the isolated line case compared to dense line and space.

TABLE 1. OPE experimental condition.

Exposure tool	KrF stepper (248 nm)
Lens NA	0.63
Illumination mode	Annular ratio (2/3 mean the shape ratio of a circular ring)
Mask	Attenuated PSM
Photo resist type and thickness	Chemically amplified positiveresist, 5850 Å
BARC thickness	750 Å
L/S ratio	1:1, 1:1.5, 1:2, Isolated line, various pitch, etc
Target CD	0.18, 0.20, 0.22, 0.24, 0.26, 0.28, 0.30, 0.32, 0.34, 0.36, 0.38, 0.40, 0.45, 0.50, 0.60, 1 μm, etc.

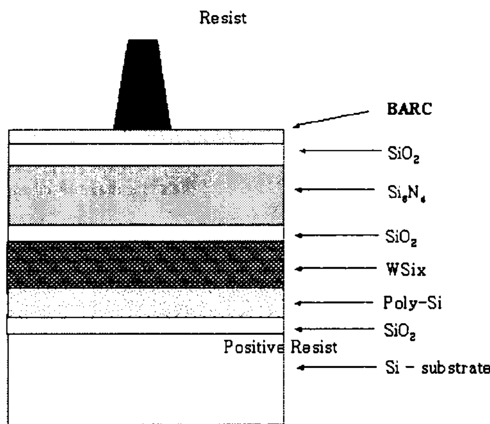

FIG. 4. Cross sectional view of sub structure for PPE measurement.

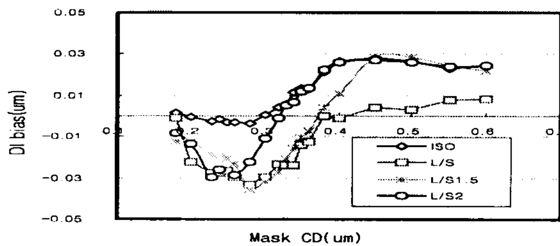

FIG. 5. DI CD error dependence on mask CD is shown for isolated and dense lines.

3. Etch loading effects

Etch loading effect differs depending on the pattern density and appears as a CD difference between ADI (after development inspection) and AFI (after final inspection). It becomes larger as the distance to the nearest neighboring pattern increases. Etch bias could be described as a logarithmic function of the distance to the nearest neighbor (Fig. 6). Wafers number 1 and 2 showed a similar trend, with less than 10nm error range. Generally, design tolerance should be within

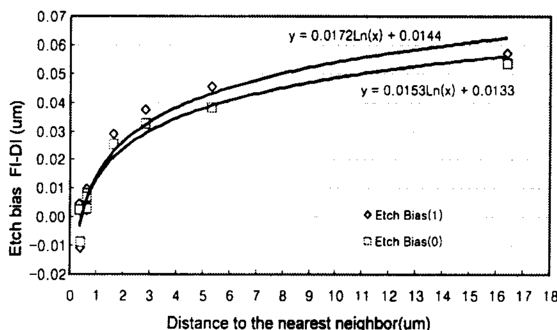

FIG. 6. Etch bias is shown as a log function of the distance to the nearest neighbor.

TABLE 2. Sample of the TPPC rule (? means input data and result data).

Feature Width(W)	Feature spacing(S)	Bias(B)
??? < W ≤??? nm	??? < S ≤??? nm	+ or - ?? nm
??? < W ≤??? nm	??? < S ≤??? nm	+ or - ?? nm
??? < W ≤??? nm	??? < S ≤??? nm	+ or - ?? nm

10 % of target CD. Etch error should be corrected since it can be more than 60 nm in some cases. Distinctive correction according to distances to the nearest pattern is necessary to effectively compensate for etch errors.

III. TOTAL PROCESS PROXIMITY-BASED CORRECTION (TPPC)

1. TPPC rule setup

Using masks with diverse pattern size, shape, and pitch, experimental data was gathered such as mask CD, ADI, AFI. All process proximity errors were collected and combined to produce total process proximity errors. We corrected total process proximity errors once for all. Parameters of bias rules consist of feature width, feature spacing and bias. For example, suppose the bias (B), to be applied to a gate shifter edge, depends on the width of the feature(W) and the spacing of the feature (S) to which the correction is applied. Then, the bias is a function of feature width and feature space. The mapping from W and S to the bias can be specified using TTPC rule table in the following form. By filling in TPPC rules tables we define the mapping from the input variables (in this case W and S) to the output variables (the bias). TPPC bias rule is based on 1-dimension, but bias can be applied step by step for different space of the feature width. Any parameters that are not TPPC rule are considered to be constant parameters. The concept diagram of TPPC is shown in Fig. 7. Without TPPC concept, each step process proximity effect was corrected separately. When etch bias is negligible due to small etch loading effect, OPC only can compensate for total process errors. In the case of large etch bias, TPPC is essential to DRAM fabrication. Fig. 8 is a real mask CD data of TPPC-compensated mask.

2. TPPC results

Fig. 9 shows gate CD compensation results using TPPC-based bias

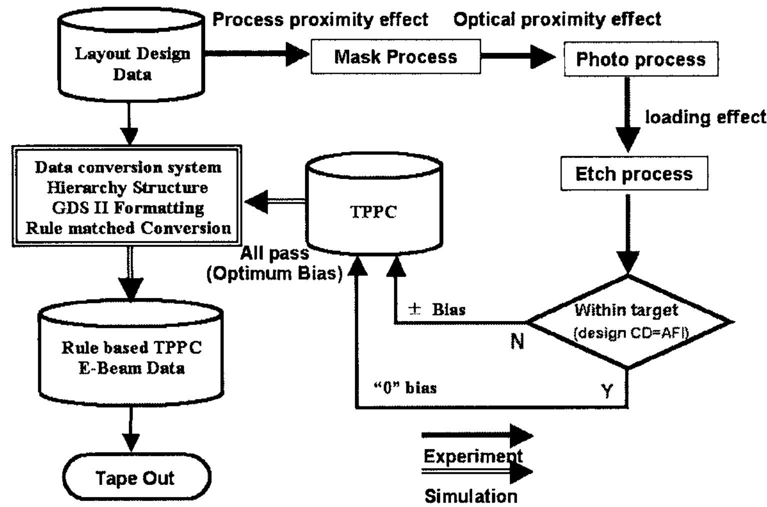

FIG. 7. Rule setup flow of TPPC.

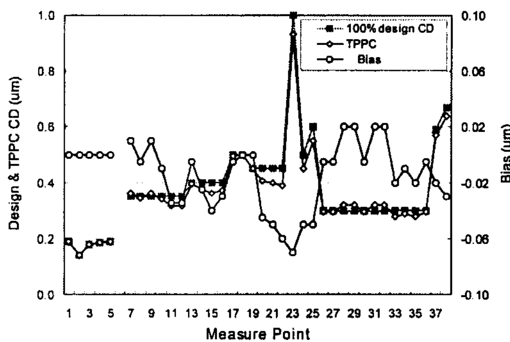

FIG. 8. E-beam data which was biased as rule table after TPPC differs from original design data.

rule. The TPPC is realized on the layout by employing a tool, TROPiC, which was recently developed by Numerical Technologies, Inc. Data volume difference between before TPPC and after TPPC rule was about 17 Mega bytes, and data enhancement was 10 % less than original layout data. Conversion time was about 1 hour. We obtained excellent experimental results of which the difference between AFI and designed CD is within specification (±10%) with wide process margin. Top view image of gate on CD SEM is displayed in Fig. 10. Difference between inner and outer gate CD is present after DI but absent after FI. Gate CD C_p value of 0.8 before TPPC was improved to be 2 after TPPC compensation.

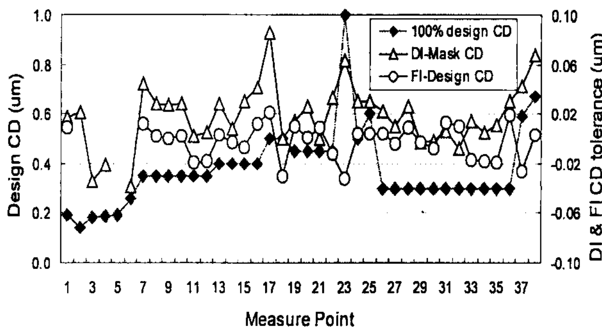

FIG. 9. Gate CD compensation results using TPPC-based bias rule.

IV. CONCLUSION

An effective method to control gate CD within specification was developed using TPPC, a concept of merging all the process proximity effects altogether. Process capability constant (C_p) could be improved by simply applying TPPC concept. Considering all the advantages of TPPC application in mask manufacturing, defect inspection, and so on, it is expected that dramatic improvement in device performance and product yield should be obtained.

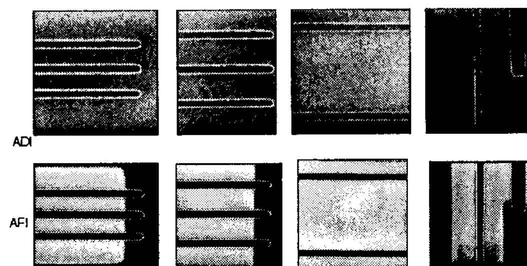

FIG. 10. Top view between after development inspection(ADI) and after final inspection(AFI).

V. ACKNOWLEDGEMENT

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