Improved Transmitter Power Efficiency using Cartesian Feedback Loop Chip

Young-Jun Chong[1] · Il-Kyoo Lee[1] · Seung-Hyeub Oh[2]

Abstract

The Cartesian loop chip which is one of key devices in narrow-band Walky-Talky transmitter using RZ-SSB modulation method was designed and implemented with 0.35 μm CMOS technology. The reduced size and low cost of transmitter were available by the use of direct-conversion and Cartesian loop chip, which improved the power efficiency and linearity of transmitting path. In addition, low power operation was possible through CMOS technology.

The performance test results of transmitter showed −23 dBc improvement of IMD level and −30 dBc below suppression of SSB characteristic in the operation of Cartesian loop chip (closed-loop). At that time, the transmitting power was about 37 dBm (5 W). The main parameters to improve the transmitting characteristic and to compensate the distortion in feed back loop such as DC-offset, loop gain and phase value are interfaced with notebook PC to be controlled with S/W.

Key words : Cartesian Feedback Loop, Narrow-band Radio System, RZ-SSB

I. Introduction

It has been drawing attention to occupy channel in LMR (Land Mobile Radio) or PMR (Private Mobile Radio) system using VHF/UHF frequency band. In the radio communications system of LMR, FM modulation method has been used since it has advantage in dynamic range, fading and power consumption compared with AM modulation. In order to deal with the channel shortage due to a rapid increase of demand, analog narrow-band has been developing (25 kHz →12.5 kHz →5 kHz) in U.S.A, Japan and England. ACSSB (Amplitude Companded Single Side Band) and TTIB/LM (Transparent Tone In Band/Linear Modulation) are used in U.S.A. In England, the specifications of 5 kHz narrow-band transceiver, MPT 1376, was established and service will be offered with 70 MHz, 160 MHz and 220 MHz frequency band and NTT in Japan developed RZ-SSB (Real Zero-Single Side Band) radio communications system. The narrow-band technique has been working with UHF (335.4～470 MHz) and VHF (138～174 MHz) in domestic[1].

High frequency stability and power amplifier linearisation are main issues in linear modulation method for analog narrow-band. There are several methods such as feed forward, linear amplification with nonlinear device, Cartesian feedback and adaptive pre-distortion. Among them, the Cartesian feedback method is most available to a narrow-band radio system due to feasible implementation[2].

The RZ-SSB radio system developed with Cartesian loop using discrete circuits has some drawbacks as follows:

· Hardware complexity and adjustable functions (phase and amplitude control, DC-offset correction) are increased,
· Takes a long time to improve the linearity of power amplifier due to various adjustable points,
· Performance variation is expected due to inaccuracy of discrete devices.

The ASIC of Cartesian feedback loop is essential not only to reduce the transmitter size and manual adjustment but also to add frequency selection filtering and signal detection functions.

II. Cartesian Loop Linearisation Technique

2-1 Cartesian Loop Operation Principle

For the Cartesian loop technique, the transmitter output is sampled just after the final RF amplifier, and synchronously demodulated, to recover quadrature Cartesian components of the modulation. These signals are used to provide negative feedback, subtracting from the modulated signals to generate a loop error signal, which drives the modulators. The configuration of Cartesian loop is shown as Fig. 1. It is composed of differential amplifier (e_I & e_Q) which is amplifying the difference between input signals (I & Q) and feedback signals (I_F & Q_F), loop filter, I/Q modulator & demodulator, RF amplifier, and phase shifter which is compensating signal delay with adjustment of carrier phase.
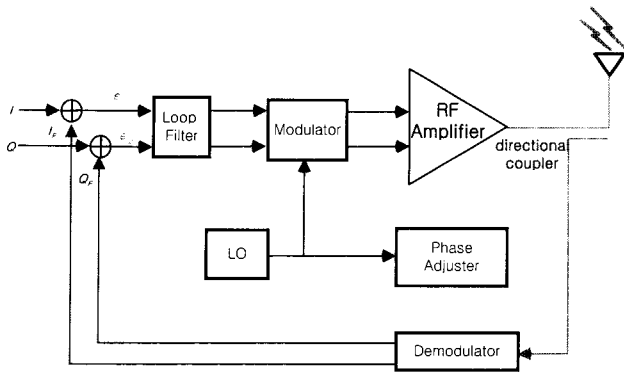
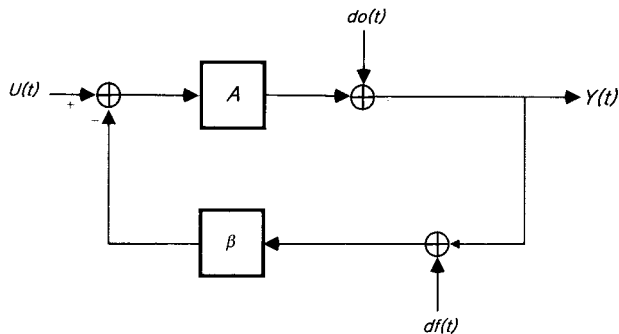Fig. 1. Block diagram of the Cartesian feedback loop.

Fig. 2. Equivalent model of the Cartesian feedback loop.

An effect of feedback loop non-linearity on system is analyzed with equivalent modeling as in Fig. 2.

Assuming open loop distortion as $do(t)$ and feedback loop distortion as $df(t)$ which are generated from RF amplifier and modulator, and loop gain $A\beta \gg 1$, the output $Y(t)$ can be approximated as eq. (1)

$$Y(t) \approx \frac{U(t)}{\beta} + \frac{do(t)}{A\beta} - df(t) \qquad (1)$$

where, $U(t)$ is the input signal, β is the feedback loop gain and A is the open loop gain.

The distortions generated from RF amplifier and I/Q modulator are reduced by increasing loop gain, however the distortions of feedback loop itself are appeared at the output port. Therefore, the devices used in feedback loop must not produce distortion.

Consequently, a high loop gain gives cancellation of distortion components and at the same time the feedback loop would be unstable. Therefore, the loop gain and cut-off frequency of loop filter must be adjusted properly. Since loop bandwidth of loop filter is limited due to stability conditions, the amplification of narrow-band signal (channel bandwidth < 100 kHz) is easier than wide-band signal[3].

2-2 Cartesian Loop Design Considerations

The performance of Cartesian feedback loop (how much cancellation of distortion components) depends on system loop gain, loop bandwidth and delay time multiplication. However, in practical system design, since loop bandwidth and delay time product are fixed, loop gain is a main factor. The method of increasing loop gain is required to improve system performance and to keep system stability. The distortion components are produced at RF output due to non-linearity of I/Q demodulator, DC-offset of OP amplifier and I/Q phase & amplitude imbalance of feedback path. By decreasing input level of demodulator with attenuator, adding DC-offset correction circuit to feedback loop and adjusting amplitude & phase of I/Q path, the distortion components would be cancelled[3]-[5].

III. Cartesian Loop Chip Designs and Specifications

The designed Cartesian feedback loop chip is shown in Fig. 3 and the functions are as follow.
· Improvement of transmitter power efficiency
· Adjust gain and phase Cartesian loop
· DC-offset correction
· Carrier suppression

3-1 Forward Path Design

The forward path of designed Cartesian feedback loop chip is composed of input amplifier, image filter, error amplifier, I/Q modulator and DC-offset correction circuit in Fig. 4.

The baseband I/Q signals are amplified through input amplifier. Image filter is designed with the second-order Sallen-key to reject image signals. The difference between distorted feedback signals and applied input signals are amplified through error amplifier. The error amplifier has an additional circuit to correct DC-offset at the input of modulator. The loop filter affecting system stability is composed of the first-order RC type. DC-offset correction circuit in Fig. 4 is composed of comparator and 10-bit SAR (Successive Approximation Register) ADC (Analog-to-Digital Converter). The comparator becomes high or low according to the variation of DC value at the input stage of modulator. Thereby the DC-offset correction is operated by the change of DAC (Digital-to-Analog Converter) output.

The I/Q modulator modulates baseband signals with transmitting carrier (138~225 MHz) using DBM (Double Balanced Mixer) as in Fig. 5. It also includes differential amplifier negative feedback circuit to maintain linearity and Rs resistor to keep constant loop gain.
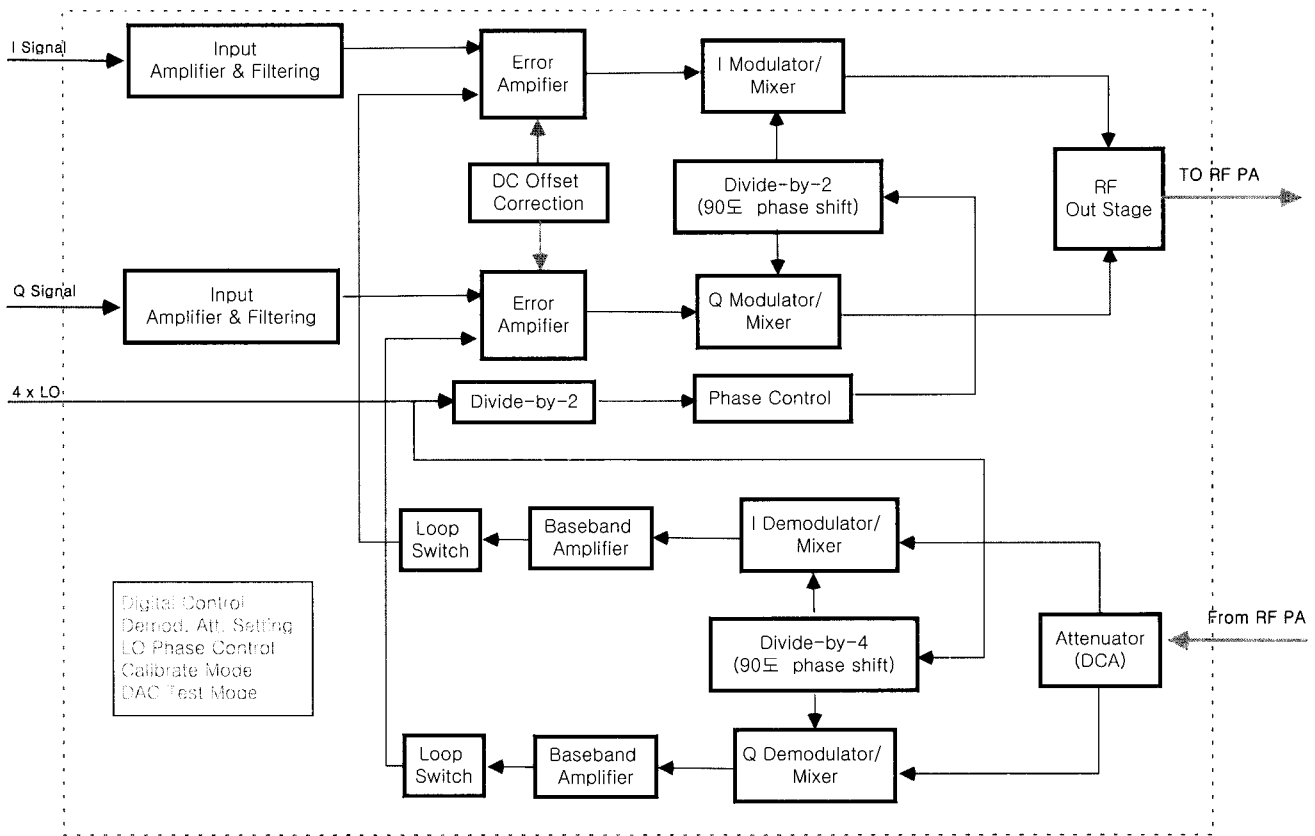
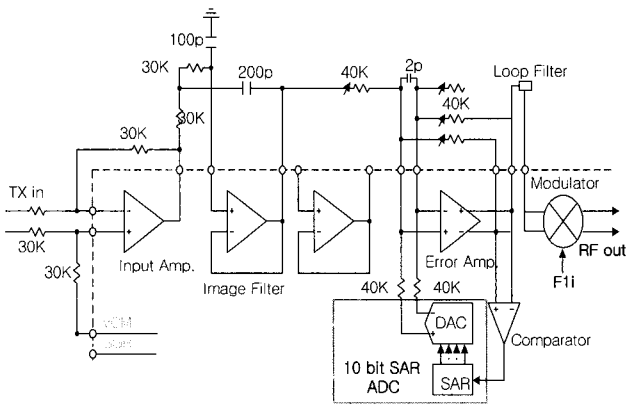Fig. 3. Block diagram of the Cartesian feedback loop chip.
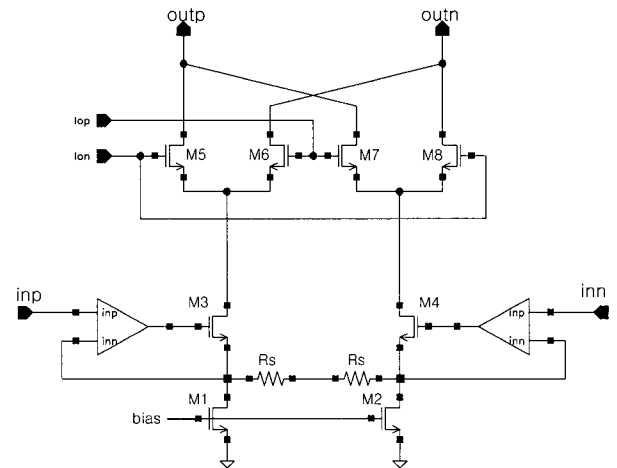

Fig. 4. Block diagram of forward path.

3-2 Feedback Path Design

The feedback path of the designed Cartesian feedback loop is composed of DCA (Digital Controlled Attenuator), I/Q demodulator and baseband amplifier as in Fig. 6.

The DCA in Fig. 7 is used to keep the linearity of I/Q demodulator by adjusting the feedback signal level and is available to 8 steps control for 17.5 dB attenuation range. The

Fig. 5. Schematic diagram of I/Q modulator.

I/Q demodulator in Fig. 8 is similar to I/Q modulator in Fig. 5, however it has additional CMFB (Common Mode Feedback) circuit to remain normal operation in spite of temperature and voltage variation. It demodulates the modulated transmitting signal (138~225 MHz) to baseband signal. The baseband amplifier adjusts feedback loop gain by amplifying I/Q signal
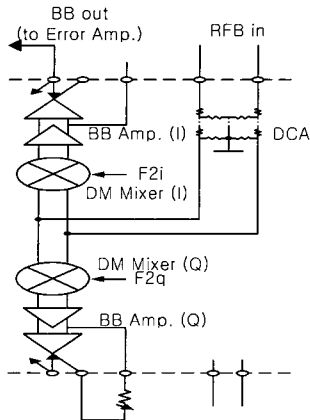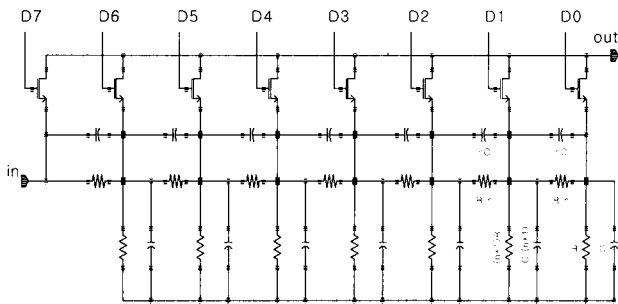
Fig. 6. Block diagram of feedback path.

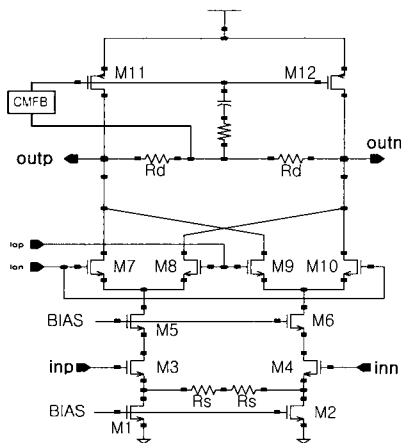

Fig. 7. Schematic diagram of DCA.

Fig. 8. Schematic diagram of I/Q demodulator.

level from demodulator.

3-3 Clock Generation Design

The phase error between I/Q modulator in forward path and I/Q demodulator in feedback path cause an another distortion components. In this paper, the phase shifter using 16-PSK
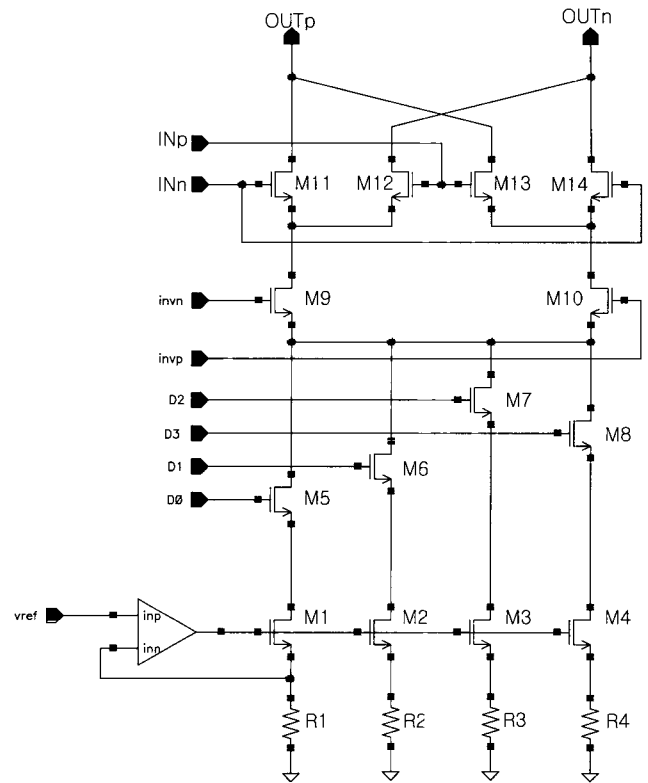

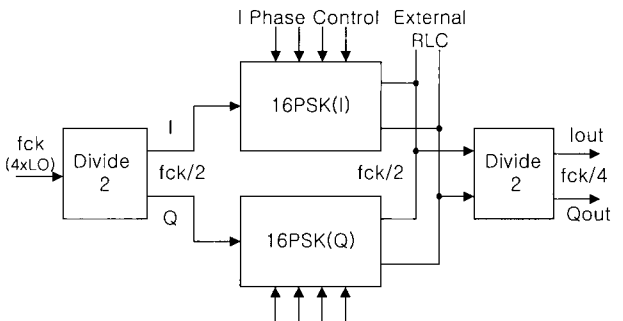Fig. 9. Schematic diagram of 16-PSK modulator.

Fig. 10. Block diagram of clock generation circuit for I/Q modulator.

modulator was designed as in Fig. 9 to reduce the phase error.

The designed variable phase shifter can control phase $0° \sim 348.75°$ with $11.25°$ step.

The LO frequency of I/Q demodulator is generated with 4-times transmitting carrier frequency ($552 \sim 900$ MHz) to keep $90°$ phase difference and to avoid injection pulling due to direct conversion method[6],[7].

The LO frequency of I/Q modulator is generated after adjusting phase by the use of 16-PSK modulator which is operating at 2-times transmitting frequency ($276 \sim 450$ MHz) as
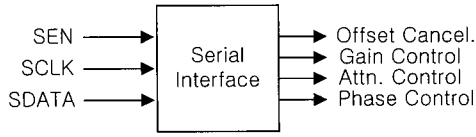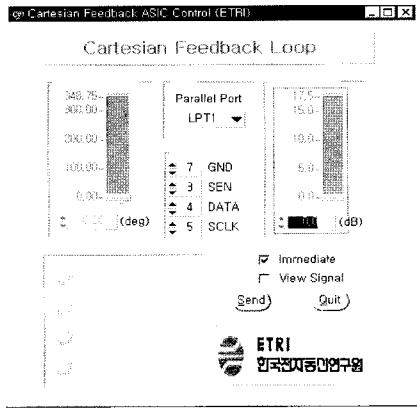
Fig. 11. Block diagram of external serial interface.

Fig. 12. Control Screen of the Cartesian loop chip.

in Fig. 10. The external RLC tank circuit is tuned to 2 × LO frequency so as to suppress the harmonic components.

3-4 External Interface of Cartesian Loop Chip

The external interface of Cartesian feedback loop chip is designed to cancel DC-offset and adjust amplitude & phase (refer to Fig. 11). Control screen and signal flow chart of the Cartesian loop chip are composed as in Fig. 12 and Fig. 13, respectively.

3-5 Requirement Specifications of Cartesian Loop Chip

The requirement specifications of Cartesian feedback loop chip are described in Table 1.

IV. Experiment Results

Table 1. Cartesian loop chip design specifications.

Items	Specifications
Input Signal Amplitude	2V p-p (Max.)
Operating Frequency	138~225 MHz
Cartesian Loop Output Power	−15±2 dBm
IMD	<−25 dBc
SSB Suppression	<−30 dBc
Loop Gain e & Steps	0~17.5 dB, 8 steps
Phase Shifter Range & Steps	360° , 32 steps
LO Input Frequency & Power	552~900 MHz, −5~0 dBm
RF Feedback Input Power	−20±3 dBm

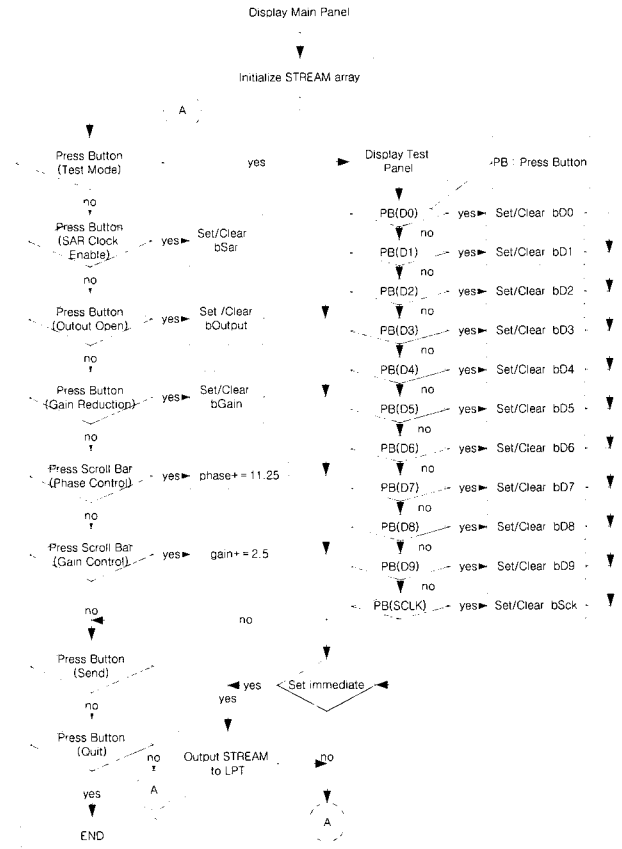
Fig. 13. S/W flow chart of the Cartesian loop chip.

The size of implemented Cartesian feedback loop chip using 0.35 μ m CMOS technology is 3.7 × 2.9 mm as in Fig. 14 and the test board using FR 4 is shown in Fig. 15.

The characteristic of open-loop output and closed-loop output is shown in Fig. 16 and in Fig. 17, respectively. The power amplifier module of FM portable M57783H was used and 30 dB attenuator is added to measure the output characteristic.

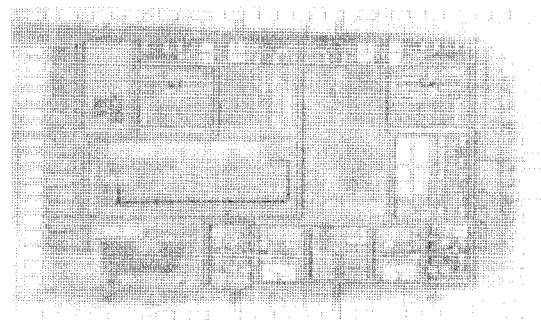From the test results, −23 dBc of IMD level was improved

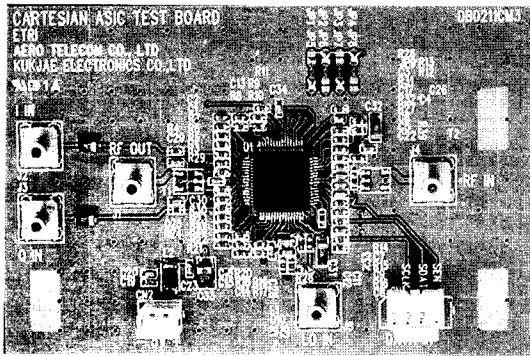Fig. 14. The implemented Cartesian feedback loop chip. (3.7 × 2.9 mm)

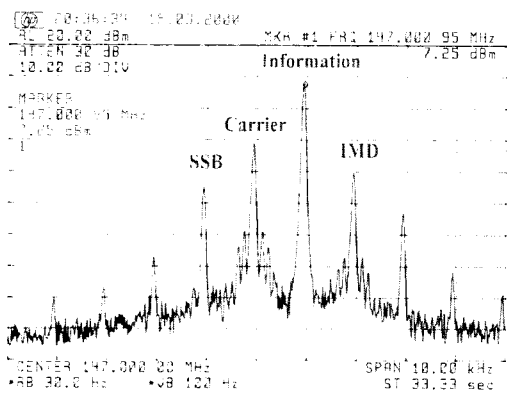Fig. 15. Test board of the Cartesian feedback loop chip.

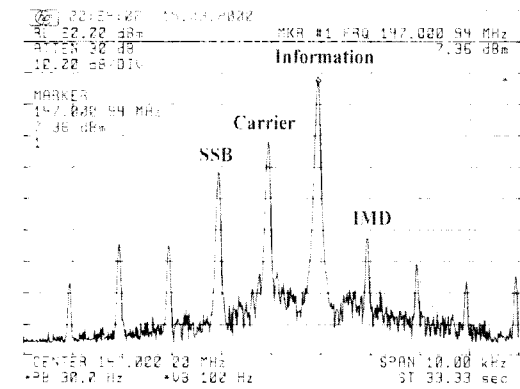Fig. 16. Open-loop characteristic of the transmitter. (Pout = 37.25 dBm)

Fig. 17. Closed-loop characteristic of the transmitter. (Pout = 37.36 dBm)

and −30 dBc above suppression of SSB is obtained at 37.36 dBm of output power.

The performance comparisons to other product (LMT-Linear Modulation Technology) using the same Cartesian feedback loop are summarized as in Table 2. There is advantage over most of aspects such as cost and power consumption and so on except

Table 2. The summary of Cartesian feedback loop chip measurement result.

	This Paper	LMT
Technology	CMOS (0.35 μm)	BiCMOS
Current Consumption	90 ~ 100 mA	120 mA
Operating Voltage	4.0 ~ 5.5 V	4.65 ~ 5.25 V
Chip Size	3.7×2.9 mm	5×3.5 mm
Circuit Architecture	Fully differential	Partly differential
SSB Suppression	> 30 dB	> 25 dB
IMD Level	− 23 dBc	− 29 dBc
Functions	DC-offset correction, Gain/Phase control, Attenuator Level control	Left same
Cost	Low	Medium

IMD level (6 dB of degradation).

V. Conclusions

This paper describes the implemented Cartesian feedback loop chip using CMOS technology which is an essential device to improve transmitting power efficiency and miniaturization of a improve transmitting power efficiency and miniaturization of a Walky-Talky. −23 dBc of IMD improvement and −30 dBc about SSB suppression was acquired. These results meet the performance requirements of a Walky-Talky.

It is required to work further on improving method to suppress IMD level (< −25 dBc) and spurious level in Cartesian feedback loop chip itself due to the increase of gain and accomplish more accurate nonlinear modeling of CMOS process.

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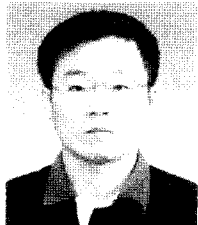
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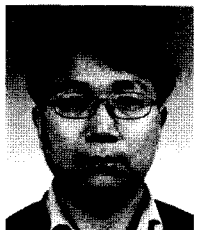
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