특 집

Technology trends in direct conversion receivers

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Abstract

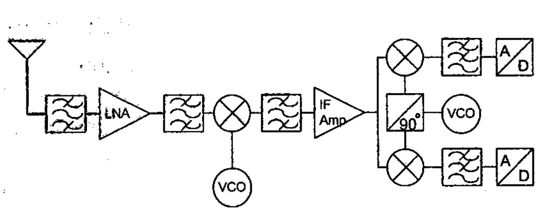
Basic introduction to direct conversion architecture was given in comparison with heterodyne one. Principal difficulties in implementation of direct conversion receiver were presented, current state of research in this field and possible solutions were summarized and classified, on the basis of extensive analysis of published materials.

I. Introduction

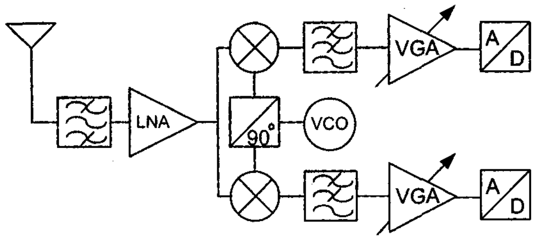
Aggressive design goals like low cost, low power dissipation and small form factors are the attributes of the recent trends in RF transceiver development. Together with the usual requirements of communication standard, as well as steeply increasing demand for multi-standard operation, these goals call for circuit and architecture breakthroughs.

Direct conversion was invented many decades ago, but became a subject of active research only around one decade ago, and the efforts are increasing from year to year. Now, activity on direct conversion is present in most of the research institutions in the field of RF IC and communication system design, and commercial products based on this architecture enter more and more application areas and frequency bands. In order to reveal the reasons of this glorious return of direct conversion, we compare it with the most established architecture-heterodyne one, which was the basis for around 98% of all receivers since its introduction in 1918.

⟨Fig. 1⟩ shows general block diagram of a single-IF heterodyne receiver, designed for operation in a standard with quadrature modulation. After selection of a band of communication standard, RF signal is applied to a low-noise amplifier and subsequently to an image-rejection filter. The result is mixed with the output of local oscillator, producing an intermediate frequency signal. Channel selection and main amplification is performed at IF-frequency, after that, signal is applied to quadrature demodulator input, in which extraction of base-band data is performed. Despite image



⟨Fig. 1⟩ Example of heterodyne receiver.



〈**Fig. 2**〉 Direct conversion receiver.

problem and trade-off between image rejection and adjacent channel suppression, heterodyne architecture can provide high selectivity and sensitivity, which have made it the architecture of choice through all its history.

Now consider direct conversion receiver block diagram, shown in 〈Fig. 2〉. It implements natural approach to downconvert a signal from RF to baseband using quadrature signal from local oscillator, which frequency is equal to that of the carrier of received RF signal. The quadrature I and Q channels are necessary because two half-spectrum of typical phase- and frequency-modulated signals contain different information and irreversible data corruption occurs if they overlap each other in down-converted dc-centered spectrum without being separated into two channels. Main amplification and channel selection by means of low-pass filters is performed in baseband.

If we can satisfy communication standard requirements using this architecture, it becomes extremely attractive and preferable compare to heterodyne one. First, the need for image-rejection and IF-filters is eliminated, since in direct conversion frequency scheme RF and LO frequencies are equal and the signal is image for itself, and channel-selection is performed by low-pass filters. Note that while usage of external image-rejection filter can be avoided by means of image-rejection mixer, IF filters, which are external bulky and expensive SAW filters, constitute principal and currently unavoidable impediment on the way of increasing integration of RF transceiver system. The last advantage of direct conversion becomes critical in the light of multi-standard operation capability. In fact, in heterodyne receiver operating in different standards with different channel bandwidth, separate SAW filter would be necessary for every standard, therefore, the overall cost would be seriously increased. Whereas, in direct conversion receiver, active tunable low-pass filter can be integrated on chip. This consideration is directly applicable to the case of 3rd generation communication standard with variable channel bandwidth. In addition to this, because of the absence of external filters, LNA need not drive 50 Ω load, and matching of LNA output and mixer input is not critical, providing more freedom in design.

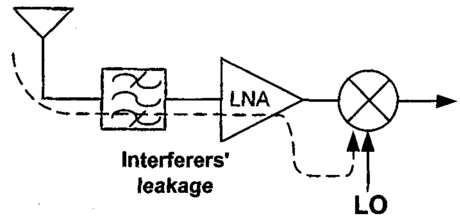
II. Design issues and existing solutions

The previous chapter argues that direct conversion architecture is very attractive for the creation of highly integrated, low-power and low-cost radio. However, before this time it had much less application than conventional heterodyne one. This is so because it entails a number of specific issues, which do not exist or are not so serious in heterodyne receivers.

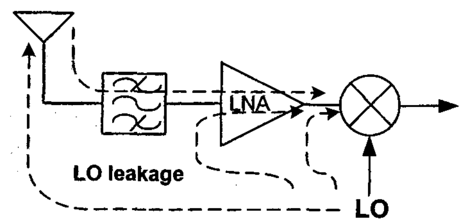
1. DC offset

1) Problem description

The problem of DC offset is usually considered as the most serious one. Since in direct conversion architecture the down-converted band extends to zero frequency, extraneous offset voltages can corrupt the signal and, more importantly, saturate the following stages. A numerical examples can be given as illustration of feasibility of described scenario[1]. DC offset has three main origins: first, self-mixing of LO signal due to different kinds of leakage. Because of insufficient port-to-port isolation, substrate and wire coupling, LO signal can leak to RF port of a mixer, input of LNA, or to antenna. In case of leakage to antenna, irradiated and received after reflection, LO signal propagates through signal path to mixer and by mixing with itself produces insidious time varying offset ⟨Fig. 3⟩. Any leakage to RF path and reflection from ports of building blocks can depend on operating condition of front-end, for example, on gain settings, and therefore, corresponding offsets can also exhibit time variance. Second, self-mixing of strong interferers, when they leak to the LO input of mixer, resulting in obviously non-static offsets ⟨Fig. 4⟩. And third, device mismatches and non-ideal duty circle of LO signal will produce some amount of DC signal throughout signal path, both RF and base-band. Existence of this phenomenon is currently inevitable, so any direct conversion receivers must incorporate some means of offset removal.



⟨**Fig. 3**⟩ Self-mixing offset origins: interferers' leakage.



⟨**Fig. 4**⟩ Self-mixing offset origins: LO leakage.

2) Existing solutions

The simplest solution is high-pass filtering. In the direct conversion pager receiver, DC offset removal by capacitive coupling of the baseband circuits is the common way. Owing to the high impedance levels of active filters, the coupling capacitors are small enough to be integrated on-chip. However, this simple solution only works because of the specific spectral features of FSK-modulation: the paging spectrum peaks at ± 4.5 kHz and dips at DC by at least 25 dB relative to its level at the peaks. Simulation shows that a first-order capacitive coupling, with a lower cutoff at 1 kHz causes no loss in receiver sensitivity when the channel filter captures the valuable signal spectrum between 1 and 10 kHz[2].

The spectra of most of the spectrally efficient modulation schemes, like GMSK and QPSK, exhibit peak at DC. Following downconversion, offset will now will be added to the peak of the spectrum. It is no longer practical to null the offset by capacitive coupling, because signal energy will surely be lost from the central peak. For example, simulation on a representative 200 kHz-wide spectrum suggest that at a target bit-error rate of 10^{-3}, a 5 Hz notch at DC causes about 0.2 dB loss in receiver sensitivity, yet this notch need only widen to 20 Hz when the receiver will cease to function[2]. It would require impractically large capacitors to produce this narrow notch, and the phase-distortion due to the RC coupling would cause the receiver performance to deteriorate further. Moreover, during burst-mode communications, the capacitor would produce intolerably long transients.

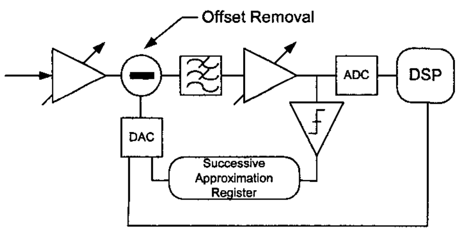
In such receivers, offset can be estimated and removed digitally, with the aid of various adaptive and gain-phase compensation[3][4][5]. One of the possible realiza-tions is shown in 〈Fig. 5〉. Here baseband signal is digitized and averaged in DSP, while successive-approximation A/D converter measures the analog signal polarity. These measurements are weighted together in a DAC, which subtracts an estimate of the offset from the baseband signal. The effective spectrum loss around dc is only few hertz, and digital filtering does not distort group delay[2].

Digital-to-analog feedback method can as well be realized in such a way: after calculating DC component in digital domain, feedback can be applied not to subtraction block, but directly to the mixer, changing its DC balance and thus implementing adaptive DC-offset cancellation mixer[18].

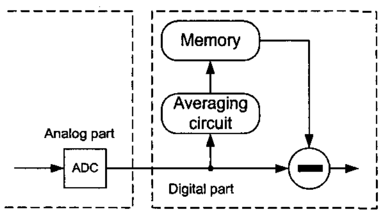
The offset cancellation can also be realized within DSP, without feeding back to analog signal path. For example, 〈Fig. 5〉 shows how procedure, essentially identical to previously described, can be implemented entirely in digital domain.

In order for the last technique to operate properly, baseband section must convey DC-offset along with desired signal to ADC without being saturated, as well as ADC must have dynamic range wide enough to digitize offset and desired signal for further procession. Therefore, in practical implementations of digital offset removal, it is desirable to add additional one-time offset cancellation on the output of the mixer. Such cancellation block will deal with static offset and therefore reduce required dynamic range of baseband section and ADC[3].

DC-feedback and high-pass filtering are feasible methods of DC offset removal in receivers for communication standards with spread-spectrum or DC-free modula-



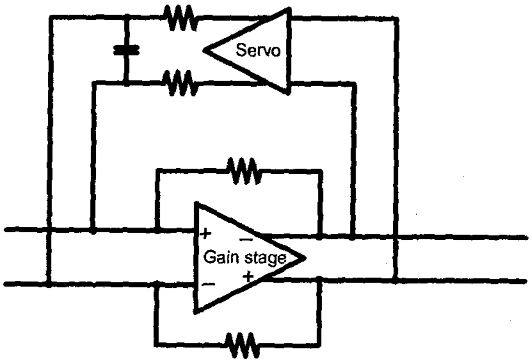
〈**Fig. 5**〉 Digital/analog feedback for DC offset removal.



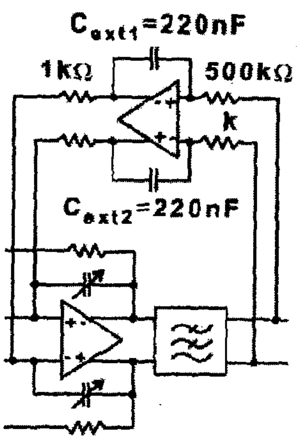
〈**Fig. 6**〉 Digital DC-offset removal.

tion schemes. DC canceling feedback loop can be realized with an amplifier followed by low-pass filter ⟨Fig. 7, [6]⟩ or with an active integrator ⟨Fig. 8, [7]⟩. Low-pass filter without additional amplification in feedback loop has also been reported[8].

Some wide-band standards even permit integration of passive high-pass filters with cut-off frequencies of few tenths of kHz in the signal path. Large values of RC constant, corresponding to low cut-off frequencies, can be obtained using high-value capacitors[9] or high on-mode resistance of MOSFETs biased in deep triode region[10].



⟨**Fig. 7**⟩ DC offset canceling loop as an amplifier and LPF.



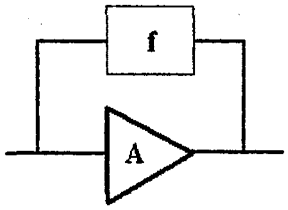
⟨**Fig. 8**⟩ DC offset canceling loop as an integrator.

(1) DC-feedback and AC-coupling as a means of DC-offset removal

Since DC-feedback and AC-coupling are quite feasible and popular means of offset removal in receivers for such fast-growing field as spread-spectrum communications, here we give brief design guideline on the subject.

Where it is applicable, AC coupling as a means of DC offset removal has advantage of simplicity. The obvious restrictions are large capacitor values and die size required. Also, AC coupling only blocks offset propagation, but does not provide stabilizing action, in other words, the propagation of offset can be blocked after certain stage, but that stage nevertheless may be saturated by offset at its input. Note, that baseband section of direct conversion receiver usually contains quite many blocks, which produce their own offset, not related with self-mixing in RF part. In general, inserting capacitor in baseband signal path cannot guaranty its functionality, and designer must look for strategically important place of offset blocking. Moreover, using one HPF in the baseband signal path may not be enough, for example in[25] and[28] baseband signal paths are DC-blocked twice.

As opposed to AC-coupling, DC feedback loop reduces gain at DC, so the baseband stage can withstand larger amount of offset at its input. But feedback cannot reduce the gain to zero, therefore, cannot provide infinite offset rejection. In order to get a feeling of DC-feedback operation, we will investigate the model of DC-offset cancellation loop, shown in ⟨Fig. 9⟩. In this feedback amplifier, let feedback



〈**Fig. 9**〉 Model of DC-offset cancellation loop.

$$f=\frac{f_0}{1-j\frac{\omega}{p}},\ |f|=\frac{f_0}{\sqrt{1+\left(\frac{\omega}{p}\right)^2}},\ p\ \textit{is real.} \quad (1)$$

factor f exhibit one-pole frequency dependence:

Assume that there is a frequency range where only the transfer function of feedback loop exhibits frequency dependent behavior because of the low-pass filter incorporated, while the main amplifier and servo-amplifier transfer functions are flat at those frequencies. Therefore, transfer function of main amplifier is represented by its low-frequency value A, which is real. Also assume that all parameters are calculated in such way that we can use ideal feedback equation. Then, for closed-loop transfer function we obtain

$$\begin{aligned} a&=\frac{A}{1+Af}=\frac{A}{1+A\frac{f_0}{1-j\frac{\omega}{p}}} \\ &=\frac{A\left(1-j\frac{\omega}{p}\right)}{Af_0+\left(1-j\frac{\omega}{p}\right)} \\ &=\left(\frac{A}{Af_0+1}\right)\left(\frac{1-j\frac{\omega}{p}}{1-j\frac{\omega}{p(Af_0+1)}}\right). \end{aligned} \quad (2)$$

In other words, the feedback network with one real-pole feedback factor leads to one-zero and one-pole closed-loop response, where the magnitude of the closed-loop real zero is equal to the magnitude of feedback pole, and the magnitude of the new real pole is .

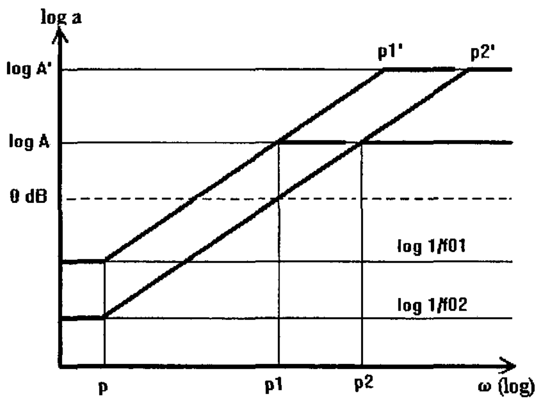
$$p_1=p\cdot(1+Af_0). \quad (3)$$

Consider two value of the main amplifier gain $A'>A$, and two value of the servo-amplifier gain $f_{02}>f_{01}$. Then the magnitude of the resulting closed-loop transfer function can be plotted as shown in 〈Fig. 10〉. The magnitudes of the new real poles, which correspond to different combinations of A and f, can be expressed as

$$\begin{aligned} &p_1=p(1+Af_{01}),\ p_2=p(1+Af_{02}), \\ &p_1'=p(1+A'f_{01}),\ p_2'=p(1+A'f_{02}) \end{aligned} \quad (4)$$

As can be seen from 〈Fig, 10〉, at high values of loop-gain, Af_0, DC rejection is determined by f_0, which can be increased by increasing the gain of servo-amplifier.

Increasing the gain of servo amplifier will increase the frequency of closed-loop high-pass pole p_1. To maintain reasonably small cut-off frequency we must increase capacitor values in the feedback loop (de-



〈**Fig. 10**〉 Magnitude of the closed-loop transfer function of baseband amplifier with DC-feedback loop.

crease p), because of this DC-offset cancellation loop required external capacitors in majority of cases.

The magnitude of high-pass pole depends on loop-gain, rather than servo-amplifier gain only, $p_l = p \cdot (1 + Af_0)$. So, when servo-loop encloses larger gain A (more stages), p_l and required capacitance are higher and increase quicker with servo-amplifier gain. Besides, as any feedback, servo loop will inject noise into signal path, the earlier in signal path we apply feedback signal, the more noise impact we get. But this effect looks not very serious compare to other high noise contributions in baseband section.

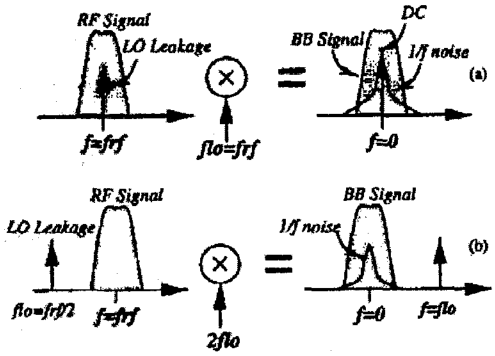
Even if we use external components and large values of capacitance are available, increase of capacitance will reduce the system capability to handle quick varying (step-like) offsets and will increase other undesirable transients.

(2) Sub-harmonic mixers

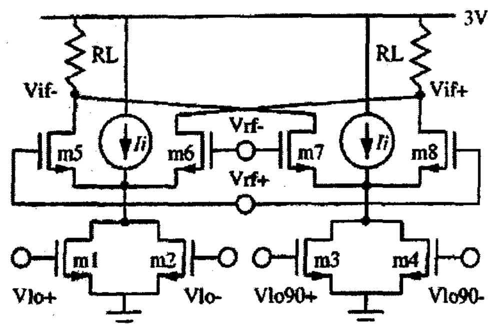
The part of DC-offset originating from both LO and interferers self-mixing exists because of the fact that signals with equal frequencies present at the LO and RF ports of a mixer will produce DC-component. This is not the case in so called sub-harmonic mixers, and such mixers open new dimension in searching for solutions of DC-offset problem.

Consider the effect of sub-harmonic mixers on DC-offset problem. Suppose, second harmonic of ω_{LO} takes part in downconversion process, in other words, if signal ω_{LO} is present at LO port, and signal ω_{RF} is present at RF port of a mixer, the output frequency is equal to $|2\omega_{LO} - \omega_{RF}|$. Then, as illustrated on 〈Fig. 11〉, LO leakage to the RF port of a mixer generates no DC component but an output signal, which is still situated at LO frequency.

One of the possible realizations of sub-harmonic mixer at RF frequency is shown in 〈Fig. 12〉. The LO stage is actually a rectifying cell which converts the differential LO voltage to the time-varying current which contains the second harmonic. In principle, fundamentals and all odd harmonics of the LO will be cancelled out at the connected drain terminals. Offset performance of this mixer is 44 dB better then that of conventional one. Using double-balanced mixer shown in 〈Fig. 12〉, authors also demonstrated self-mixing free front-



〈**Fig. 11**〉 Conventional a) and harmonic b) mixing for $\omega_{LO} = \omega_{RF}/2$.



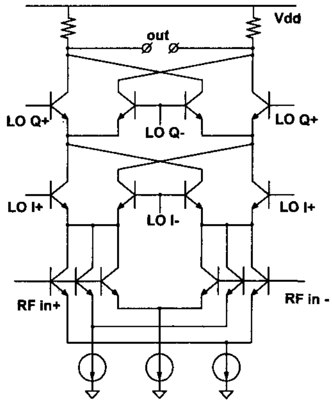
〈**Fig. 12**〉 Double-balanced harmonic mixer.

end[20] and implement this front-end in 4-FSK receiver[21]. Unfortunately, they were not able to maintain good linearity while generating harmonics right inside the mixer, and applications of this mixer and front-end are restricted to those with relaxed linearity requirement, for example, paging receivers. The same topology was published in bipolar technology as well[29].

Sub-harmonic mixing (the term harmonic is used as well), when the frequency of downconverted product is $|n\omega_{LO}-\omega_{RF}|$, was widely utilized in microwave area, where obtaining $\omega_{LO}=\omega_{RF}$ was either too difficult, power consuming, or impossible. There, mixing with LO frequency being sub-harmonic of RF frequency was implemented by designing a block with specific nonlinear transfer characteristic. Conversely, in RF field, ideal mixer corresponds to linear but time-varying system (with respect to RF signal). Therefore, in all of RF sub-harmonic mixers reported up to now, desired mixing is obtained by using larger number of LO signals of frequency ω_{LO} with appropriately selected phases, which create the switching action that would be created in conventional mixer excited by LO signal of frequency $n\omega_{LO}$.

Here we continue with review of reported sub-harmonic mixer topologies. Switching action required for sub-harmonic mixing with $\omega_{LO}=\frac{\omega_{RF}}{2}$ can be obtained using the topology, known in analog field as three-signal multiplier, which is in fact two stacked Gilbert-cells, shown in ⟨Fig. 13⟩[30].

The authors of this topology have defined LO rejection as LOR=(Conversion Gain from RF frequency)/(Conversion Gain from LO frequency), where the signals are present at RF port. For conventional direct conversion mixer LOR defined in such way is equal to 0 dB (note that this value does not account for LO-to-RF leakage). Proposed mixer achieves LOR of 30 dB and 39 dB working with RF frequency of 1 GHz and 2 GHz correspondingly. While adopting this switching stage topology, the increase of noise contribution from switching stage is usually small, but higher supply voltage is needed and LO power required is roughly double of that for usual mixer[30].

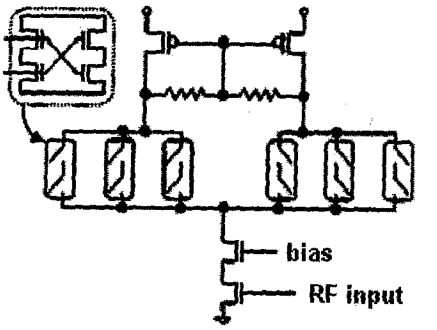


⟨**Fig. 13**⟩ Sub-harmonic mixer based on three-signal multiplier.

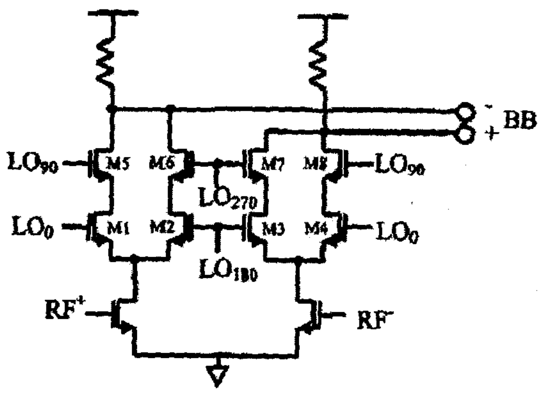
Another possible topology of a mixer with $\omega_{LO}=\frac{\omega_{RF}}{2}$ is shown on ⟨Fig. 15⟩[31].

By proper synthesis of switching action, it is also possible to design a single-balanced mixer which accommodates 6 LO signals $\omega_{LO}=\frac{\omega_{RF}}{3}$ with appropriately selected phases and operates effectively as conventional mixer with single-phase LO signal with $\omega_{LO}=\omega_{RF}$ ⟨Fig. 14⟩. In overall, 12 single-ended LO signal are required for I/Q mixer pair in direct conversion front-end[27][32].

Attempts were made to use advantages



〈**Fig. 14**〉 Simplified schematic of sub-harmonic mixer with.



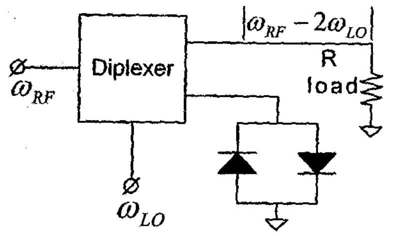
〈**Fig. 15**〉 Sub-harmonic mixer, single-balanced version.

of passive-mixer approach in direct conversion receivers. The only passive mixer that has being seriously considered in direct conversion research is even-harmonic type mixer using anti-parallel diode pair (APDP)[12]. It provides usual benefits of passive approach and exhibits a number of advantages over conventional diode double-balanced mixers. The particular interest of direct conversion architecture is the low level of second-order intermodulation products (will be discussed in details later). In APDP-mixers operating as direct conversion mixers, LO is running at half-RF frequency.

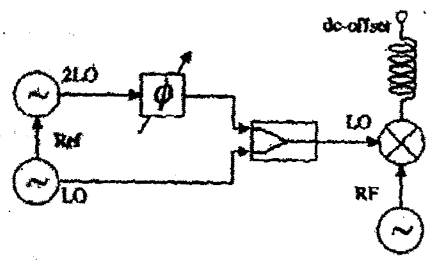
General scheme of basic even-harmonic mixer using anti-parallel diode pair is shown in 〈Fig. 16〉. The ring-type APDPs are used more frequently in order to increase isolation between LO and RF ports[13][14].

A number of APDP mixers were evaluated as a part of receivers for PHS, GSM, W-CDMA and satellite CDMA standards[15]. The main conclusion of the authors is the possibility of fulfilling standard requirements by using passive approach. Just like any passive mixers, APDP mixers require higher LO power, external components, and exhibit conversion loss. Reported values of IIP2 are high, but similar performance can be achieved in active approach nowadays[16].

An interesting method for removing DC-offset in anti-parallel diode pair was proposed recently[17]. The authors derived



〈**Fig. 16**〉 General scheme of basic even-harmonic mixer using anti-parallel diode pair.



〈**Fig. 17**〉 Block diagram of DC-offset cancellation experiment for anti-parallel diode pair mixer.

equation of mixer action of mismatched APDP, and found out that DC offset can be eliminated by generating another DC component by down-conversion of additional tone at 2^{nd} harmonic of LO. The analytical approach shows that varying the phase and magnitude of 2^{nd} harmonic varies the sign and magnitude of this canceling DC component. Experiment 〈Fig. 17〉 has verified offset cancellation below the noise floor. Remarkably, this method deals with both self-mixing and mismatch offsets. Since precision tuning of the phase and amplitude can be easily performed by on-chip active components, authors pointed out the possibility of monolithic realization of this technique using LO frequency doubler, phase shifter and variable attenuator. Also, when implemented in a closed loop system similar to PLL, the DC-offset output of the mixer can be used as feedback to vary the 2^{nd} harmonic tone until a zero offset and locked condition occur. The authors stated that they were able to cancel DC-offset below the noise floor while maintaining a 2^{nd} order IIP2 of +16 dBm and an average conversion loss of 10 dB for input RF frequencies of 4 to 6 GHz. Even though they do not speak about IIP2 degradation, the value of IIP2 of +16 dBm is much smaller then typical reported values for APDP mixers, which can exceed 50 dBm.

2. I/Q mismatches

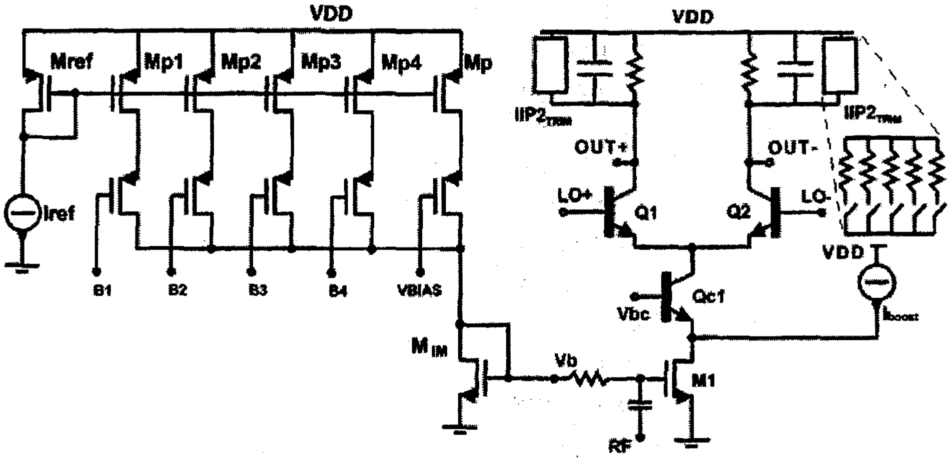
1) Problem description

Every direct conversion receiver must incorporate quadrature downconversion. This requires either shifting of LO signal by 90° or using LO with quadrature output (shifting the phase of RF signal has many disadvantages and is not used in majority of direct conversion receivers). In either case, the errors in the nominally 90° phase shift and mismatches between the amplitudes of I and Q LO signals corrupt the downconverted signal constellations, thereby raising the bit error rate. Since in direct conversion receiver the I and Q phases are separated at frequencies one or two orders of magnitude higher then in heterodyne one, the signal paths tend to introduce more phase and amplitude errors due to device mismatches. The term I/Q mismatch denotes gain and phase mismatches in both LO and information signals before and after downconversion.

2) Existing solutions

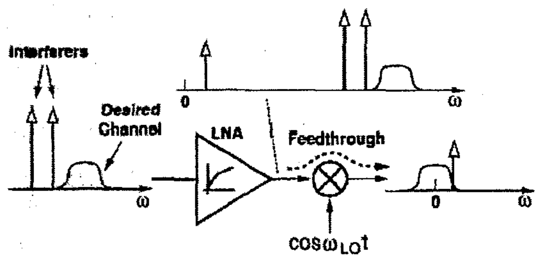
Our search has shown that almost all authors rely on good design of phase shifting networks and careful symmetrical layout as their solution of I/Q mismatch problem. Note, that even with higher probability of phase difference between I and Q channel of LO signal, direct conversion architecture is much less sensitive to these mismatches than image-rejection mixer architecture[1].

Since I/Q mismatches vary negligibly with time, analog or digital calibration can be employed to reduce their effect[1]. In recent article, a method was demonstrated, in which amplitude equalization of the signal channels was done at RF frequencies immediately after the received signal is fed into I and Q mixers. The imbalance in I/Q amplitudes is corrected by adjusting the drain current through the mixer transconductance element using a 4-bit digitally



〈**Fig. 18**〉 Mixer with gain-balancing bias arrangement and IIP2-trimming load.

controlled bias arrangement, shown in 〈Fig. 18〉. The gain equalization performed in this way has moderate effect on the channel phase balance and small effect on channel noise figure[33].



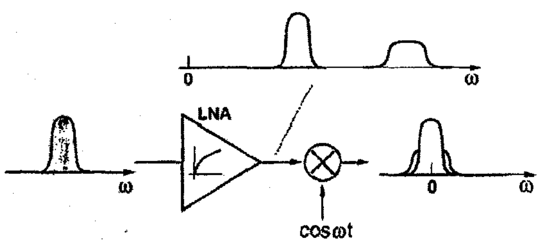
〈**Fig. 19**〉 2nd order distortion:generation and feedthrough of IM2.

3. Even-order distortion

1) Problem description

Due to the frequency translation scheme, typical RF receivers are susceptible to only odd-order intermodulation effects. In direct conversion, on the other hand, even-order distortion is usually treated as one of the most serious problem, as much as troublesome as DC offset. Even-order nonlinearity (with second order nonlinearity being the most significant) has three main manifestations. First, the squaring action of second-order nonlinearity will generate a low-frequency (difference-frequency) component, which falls inside the band of channel-select LPF under the presence of two close interferers in the band of interest 〈Fig. 18〉.

Second, in addition to phase or frequency modulation, received signal can exhibit some spurious amplitude modulation as well. This could arise from filtering in t -ansmitter or because of disturbance and fading during propagation. If useful input signal exhibit quadrature modulation with carrier frequency ω_C, then the same signal with spurious amplitude modulation can be



〈**Fig. 20**〉 2nd order distortion:downconversion of signal harmonics.

represented as $x_{in}(t) = (A + \varepsilon\cos\omega_m t)(a\cos\omega_C t + b\sin\omega_C t)$, where $\varepsilon\cos\omega_m t$ represents a low-frequency amplitude-modulating signal. In this situation, second-order distortion will yield a spurious base-band term $(a^2+b^2)A\varepsilon\cos\omega_m t$.

Because of device mismatches and deviation of LO duty cycle from 50%, a fraction of the low frequency components (on the order of 1%[1]) generated by two described mechanism in LNA or in the transconductance stage of the mixer will appear at the output of switching stage without frequency translation, thereby corrupting the down-converted signal of interest.

And third, suppose, due to second-order nonlinearity the second harmonic of the desired signal is present at the RF port of the mixer. In this situation, if second harmonic of LO frequency is present at the LO port, it will downconvert the second harmonic of the RF signal to the baseband, further degrading signal-to-noise ratio 〈Fig. 20〉.

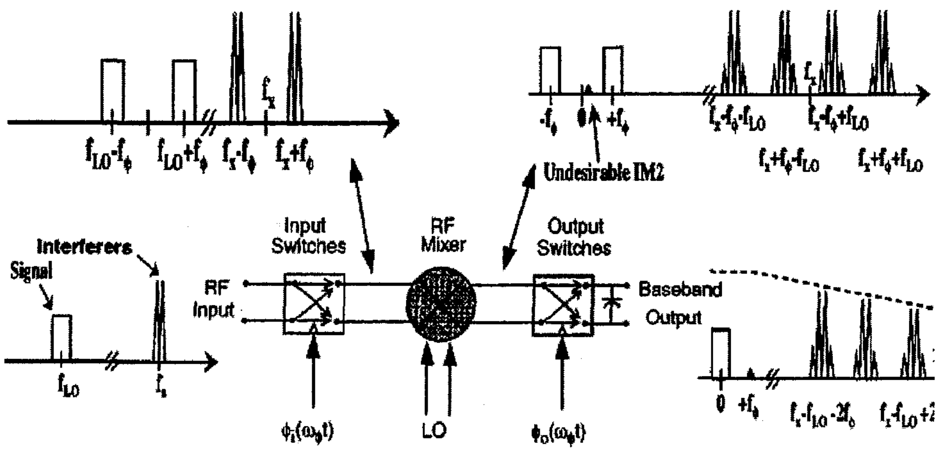
As interferer environment becomes more aggressive, all these distortions will degrade the sensitivity of a direct conversion receiver more rapidly than that of the heterodyne one.

3) Existing solutions

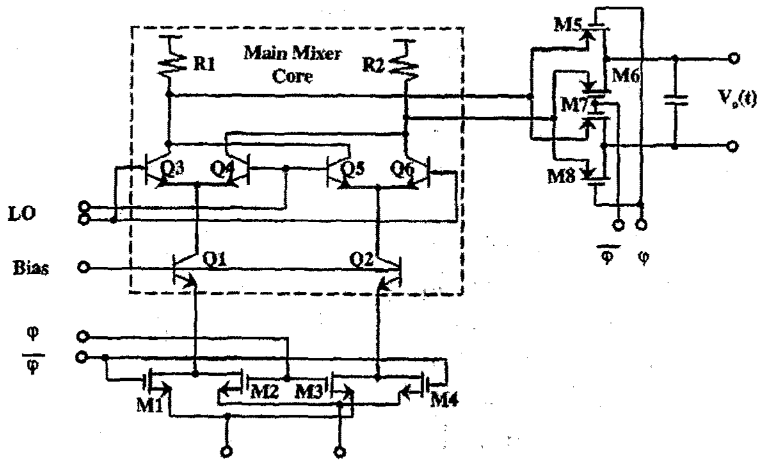
The basic solution of this problem is to reduce the 2nd order intermodulation products by using differential LNA and double balanced mixers. AC-coupling interface between LNA and mixer, in other words, filtering the low-frequency intermodulation products of LNA can be applied as well[7].

Few more techniques were developed to remedy IM2 problem in direct conversion receivers, and even though these techniques are far from implementation for mass products, very promising result were demonstrated under laboratory evaluation, which create basis and ideas for further research. First, a downconversion mixer was presented, which exhibits excellent rejection to second-order intermodulation by utilizing so called principle of dynamic matching, illustrated in 〈Fig. 21〉[23].

In 〈Fig. 21〉, the idea is to introduce pre-



〈Fig. 21〉 Principle of dynamic matching.

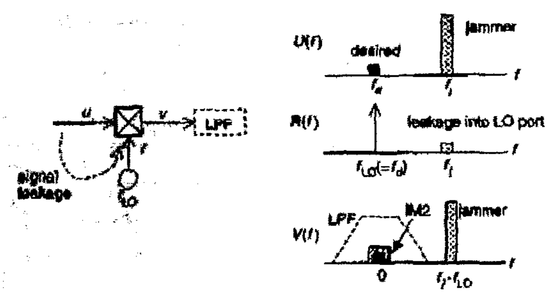


〈**Fig. 22**〉 BiCMOS realization of dynamically matched mixer.

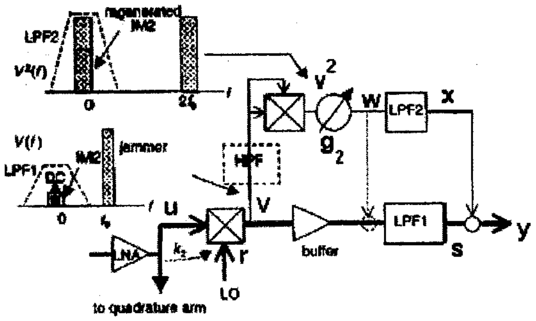
and post-mixing, which allow to get desired signal transferred to baseband and IM2 from core mixer transferred out of passband of following filters by means of postmixing by using periodic signals φ_i and φ_o. Using the pseudorandom signal φ_ii and φ_o is also possible, in this case IM2 from core mixer will be spread over a range of frequencies. Additional benefit is the reduction (up-conversion) of flicker noise. To attain maximum IIP2 performance, synchronization between input and output switches is required. Limited synchronization and on-chip matching constitute the limitations of IM2 rejection performance. BiCMOS and all-CMOS mixers were presented. The schematic of BiCMOS mixer is given in 〈Fig. 22〉.

For 75 MHz frequency of periodic dynamic matching signal authors declare a 12 dB improvement in IIP2 over a best IIP2 ever reported for standard BiCMOS Gilbert-cell mixer, and 11 dB improvements over best IIP2 for standard all-CMOS Gilbert-cell mixer. For all-CMOS mixer 30 dB improvement in noise floor at 1 kHz over standard mixer was observed. In measured performance authors also declare 20 dB DC offset improvement, which is reasonable, since the core mixer is not a direct conversion mixer any more.

Another technique deals only with IM2 originating from interferers' with AM modulation, which were mentioned in current chapter as "second manifestation" of even-order nonlinearity. This kind of IM2 occurs less often but can be more damaging, since because of signal leakage from RF to LO port of a mixer and consequent self-mixing, such interferer will



〈**Fig. 23**〉 Input and output spectra of direct conversion mixer in the presence of signal leakage from RF to LO port.



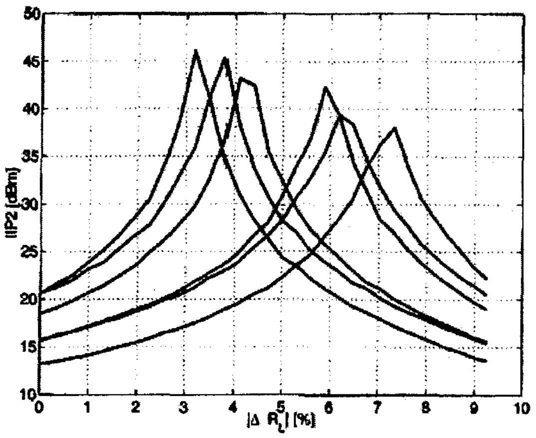
〈**Fig. 24**〉 Scheme of IM2 cancellation.

create a distortion baseband components whose amplitude is proportional to interferer's power envelope. In the presence of circuit imbalance combined with mixer nonlinearity the same effect will occur, like shown in 〈Fig. 23〉.

Proposed technique relies on postdistortion approach. 〈Fig. 24〉 illustrates the main idea. The output spectrum of the mixer still contains the frequency translated interfering signals. These include jammer at $f_0=f_J-f_{LO}$ that cause IM2. The envelope and modulation of these large signals is preserved in the downconversion process. Since IM2 distortion signal is related to the envelop properties, a correction signal w can be generated by passing the pre-filtered signal v through a nonlinear circuit that mimics the dominant distortion characteristic. To generate IM2 distortion, a squaring circuit is used. The output of the squaring circuit is filtered to remove out-of-band components and then fed forward with the appropriate gain scaling (g_2 coefficient) to cancel the unwanted IM2 in the desired signal. The adjustment of coefficient g_2 and summation of main and canceling signals must be done in digital domain. Correlation technique is used for g2 adjustment. Applying modified correlation algorithm, described technique shows promising results of both DC and IM 2 cancellation with single-tone test signals as well as in TDMA GSM-like environment. For the details of used algorithm and measurement result readers are referred to original article[34].

The following technique looks much simpler compare to the previous two, but nevertheless, as authors claim, it could improve IIP2 of a direct conversion receiver by 20 dB or more[33]. It is based on the work reported in[35], which is the first comprehensive investigation of the effect of mismatches in single- and double-balanced active mixers on IM2 performance. The presented technique is based on theoretical result of[35], in which it was found that the effects of different mismatches are not absolutely additive, but interact in a different way, which can be predicted. Therefore, IIP2 of an imbalanced mixer can be improved by changing the balance of some circuit part. Doing this, we do not necessary try to improve the balance in overall, but try to find imbalanced condition, in which IIP2 is nevertheless maximized. Authors have demonstrated, that it always can be done, provided that tuning range and resolution of a controllable "mismatch" devices are selected properly. It can be, like in[33], load resistors.

The realized IMD2 cancellers consist of binary-weighted multiples of equal-sized unit resistors 〈Fig. 18〉. These additional loads are connected to the output through the switching array with 5 bit digital control. The switched resistors are placed in parallel to both mixer loads. I and Q channels must have independent IMD2



〈**Fig. 25**〉 Improved receiver IIP2 of six samples versus tuning range.

cancellers, since different downconversion channels exhibit different IIP2 characteristics and should be calibrated separately. 〈Fig. 25〉 illustrates the measured IIP2 of six receiver samples as a function of the controlled imbalance in the mixer load resistors. The tuning range is $\pm10\%$ from the nominal mixer load resistance values. While applying this technique, the tuning range and resolution must be determined from known process tolerances with the aid of simulations. The same method can be used in double-balanced mixers as well.

4. Flicker-noise

1) Problem description

Since in direct conversion receiver the signal after LNA and mixer usually falls in the range of tens of microvolts, most of the receiver amplification must be performed in baseband. Under this condition, the noise characteristic of baseband circuitry becomes very important. In particular, since the downconverted spectrum is located around zero frequency, the 1/f noise has profound effect, a serious problem in MOS implementations.

2) Existing solutions

In addition to conventional noise reduction techniques, MOS baseband sections must be implemented with large transistors to minimize the magnitude of flicker noise. Bipolar transistors must be used whenever possible because of their absolutely superior flicker-noise characteristic with respect to MOS devices.

Flicker noise imposes additional requirement on front-end gain, which should be high enough to suppress baseband noise contribution, a challenging demand if take into account high linearity requirement of direct conversion front-end.

5. Oscillator leakage and pulling

1) Problem description

In addition to introduction of DC offset, in direct conversion receiver leakage of the LO signal to the antenna and subsequent irradiation creates interference in the band of other receivers. Each wireless standard imposes upper bounds on the amount of in-band LO radiation, typically between -50 and -80 dBm.

Leakage problem in direct conversion receivers has another important aspect, namely, leakage from the RF port to the receiver's voltage controlled oscillator (VCO). Any external signal with $\omega=\omega_{VCO}$ coupling into the oscillator can perturb the phase of the VCO, which can cause serious problems in a phase-modulated system. Additionally, large-signal interferers in the receive may cause strong enough leakage to pull the VCO frequency off, further degrading the receiver performance.

3) Existing solutions

Careful layout and orthogonal tracing of RF and LO paths must be used as initial means of reducing LO leakage. Differential local oscillators and building blocks with high reverse isolation, for example cascode LNA, can also reduce coupling to antenna.

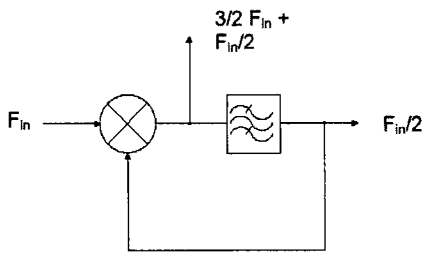
Another idea to desensitize VCO to leakage from antenna and prevent it from radiating to the receive band is to operate VCO on some other frequency and then perform appropriate frequency transformation in order to obtain required LO frequency (non-sub-harmonic mixing is assumed). It makes sense because in this way much less area of effective antenna radiating at is obtained, and problem of LO to RF port leakage is alleviated. Concerning RF to LO leakage, VCO is much less sensitive to incoming signal at $\omega \neq \omega_{VCO}$ (note that sub-harmonic mixing alleviates these issues as well, and at the same time is superior with respect to frequency transformation approach when DC-offset cancellation is concerned).

There are several realizations of this idea. First, we can operate the VCO in the synthesizer at a multiple or fraction of the needed LO frequency, and then perform either a division or multiplication to produce the actual LO. This is practical in some systems, but can be a problem if the desired LO is relatively high and a suitable double-frequency VCO with suitable phase noise is too costly or consumes too much power. It can also be a problem if the process of doubling the VCO frequency consumes too much power.

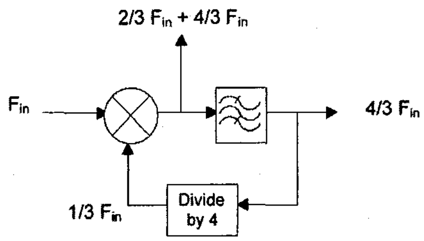
Another approach is to create the tunable LO by means of mixing a tunable VCO with a fixed offset oscillator. Here tradeoffs in power may be more favorable than in the method of using half- or double-frequency oscillator. While this method has the advantage that neither VCO is operated near the RF signal frequency, it requires a second oscillator and closely resembles the heterodyne in terms of component count and complexity.

Another interesting method uses regenerative division to produce the desired LO from an oscillator operating at a different frequency without a second VCO[3][5]. This method, originally published in 1939, uses a part of signal from a mixer's output as the LO input to the same mixer. In the original version, energy at half the input frequency is coupled back to the LO input of a mixer, producing outputs at 1/2 F_{in}in and 3/2 F_{in}, and the desired signal can easily be selected ⟨Fig. 26⟩. Here VCO signal cannot give rise to signal in receive band even after experiencing harmonic distortion.

In a variant of this approach a divide-by-four circuit is used, creating signals at 2/3 and 4/3 the input frequency ⟨Fig. 27⟩. This LO generation scheme was successfully implemented in a multi-band GSM direct-



⟨**Fig. 26**⟩ Basic regenerative divider.



〈**Fig. 27**〉 Regenerative divider for LO at 4/3 VCO frequency.

conversion radio. A carefully chosen tunable VCO frequency (in this case, approximately 1350−1450 MHz) produces outputs in the 900 and 1800/1900 MHz GSM bands that can be used for the direct-conversion local oscillator. Further refinement of this approach delivers the I and Q versions of the LO signal for GSM and DCS/PCS bands.

Ⅲ. Conclusions

Basic introduction to direct conversion architecture was given in comparison with heterodyne one. Principal difficulties in implementation of direct conversion receiver were presented, current state of research in this field and possible solutions were summarized and classified. Increased number of commercial products appearing in the market and recent research advances let us hope that direct conversion architecture will be the basis for wide variety of communication systems in the future. We can assume that in RF part of a receiver, one of the most promising approaches to solution of many specific problems of direct conversion architecture will be subharmonic mixers. Also, a variety of adaptive compensation and calibration techniques utilizing possibilities of Digital Signal Processing will appear, in addition to existed ones, becoming inseparable part of direct conversion receiver.

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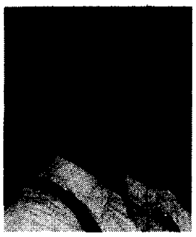
저 자 소 개



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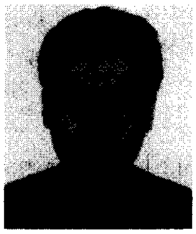

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