Reduction of Plasma Process Induced Damage during HDP IMD Deposition

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The HDP (High Density Plasma) CVD process consists of a simultaneous sputter etch and chemical vapor deposition. As CMOS process continues to scale down to sub- quarter micron technology, HDP process has been widely used for the gap-fill of small geometry metal spacing in inter-metal dielectric process. However, HDP CVD system has some potential problems including plasma-induced damage. Plasma-induced gate oxide damage has been an increasingly important issue for integrated circuit process technology. In this paper, thin gate oxide charge damage caused by HDP deposition of inter-metal dielectric was studied. Multiple step HDP deposition process was demonstrated in this work to prevent plasma-induced damage by introducing an in-situ top SiH_4 unbiased liner deposition before conventional deposition.

Keywords : HDP, CVD, CMOS, inter-metal dielectric, plasma-induced damage

1. INTRODUCTION

As technologies shrink and gate oxides become thinner, IMD (Inter Metal Dielectric) oxide deposition is one of the main charging sources in CMOS processes. Plasma-induced gate oxide damage has been an increasingly important issue for integrated circuit process technology. The damage usually causes the device performance degradation, the yield loss, and/or the unacceptable reliability failure. We investigated the charging phenomenon during HDP (High Density Plasma) CVD process. It could be confirmed that the HDP damage was protected by a pre-deposited liner oxide layer before conventional HDP process in that investigation[1,4]. According to Gyeong S. Hwang's paper[2,5], Monte Carlo simulations of the charging depended on pattern during IMD deposition in HDP revealed that the initial conformality of the IMD film played a crucial role in metal line charging up and the subsequent degradation to the buried gate oxide, to which the metal line is connected. It is generally known that the line charging occurs when the top dielectric is thick enough to prevent the tunneling currents, while the sidewall dielectric thickness still allows the tunneling currents to flow into the metal line, and finally the differential charging of the sidewalls, which induces the latter currents, is caused by electron shading[3,6]. The

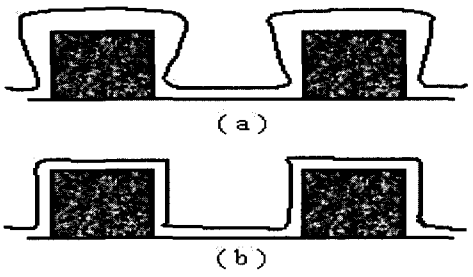


Fig. 1. The profiles of deposited oxide by the two models considered: (a) non-conformal growth, and (b) conformal growth. Most of the charging damage occurs before the oxide grows as it shown.

results suggested that the charging could be reduced by depositing a more conformal IMD film around the metal line and by increasing the surface conductivity of the film. In that work, a multiple steps of HDP process with an in-situ pre-deposited oxide fails to prevent HDP charge damage.

2. EXPERIMENTAL

The experiment was tested on AMAT ultimate HDP CVD centura system, which has two different coils with independent RF generators creating the more uniform plasmas. The HDP was generated by an ICP (Inductively Coupled Plasma) source from SiH_4, Ar, and O_2 chemistries. Bias and source frequencies were respectively 13.56 MHz and 2 MHz. The wafer clamp was done with a unipolar ESC (Electro Static Chuck), and the cooling system obtained the circulation of helium between the ESC and the wafer. All experiments were performed on HDP deposition process 6KÅ with the three different initial liner condition. Split conditions refer to Table 1.

Table 1. Split conditions.

Split	T- SiH_4	Int Temp	Liner dep thk
A	Off	390℃	400Å
B	On	320℃	800Å
C	Off	320℃	800Å
D	On	390℃	400Å

※ Split A is conventional recipe.
T-SiH_4: Top-SiH_4 Flow
Int Temp: Initial liner deposition Temperature.
Liner dep thk: Liner deposition thickness

Wafers were processed through a full 0.18um, 4 level metal CMOS flow. We used the antenna test structures that had the transistor gate size fixed at a width x length of 5 x 0.5um, and the gate oxide thickness could be 3.3 nm. The complete specifications of these structures are summarized in Table 2.

Table 2. Antenna structure.

Device	poly and metal 1 antenna ratio				
NMOS	100:1	300:1	500:1	1K:1	3K:1
PMOS	100:1	300:1	500:1	1K:1	3K:1

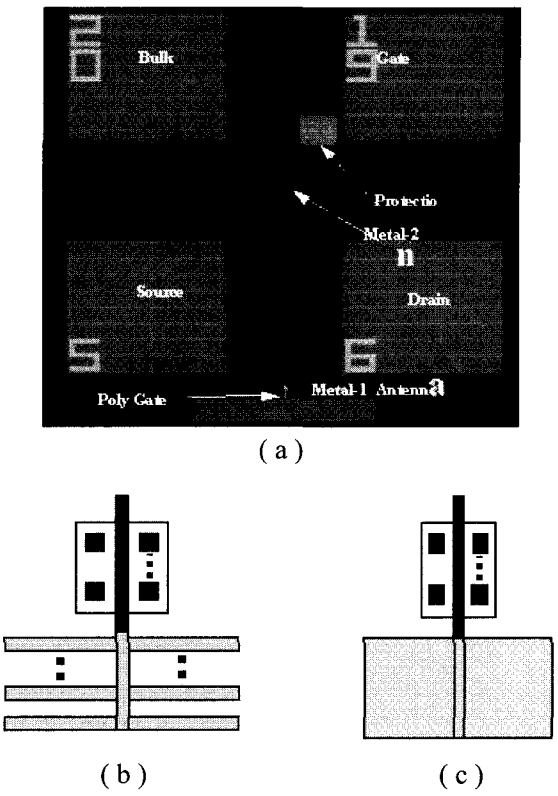
(a) Comb type antenna

※ Metal pitch 1.1 (width/space = 0.25/0.25 um)

Device	poly and metal 1 antenna ratio		
NMOS	100:1	1000:1	3000:1
PMOS	100:1	1000:1	3000:1

(b) Block type antenna

※ Receive transistor : Width/Length 5/0.5um



(a)

(b) (c)

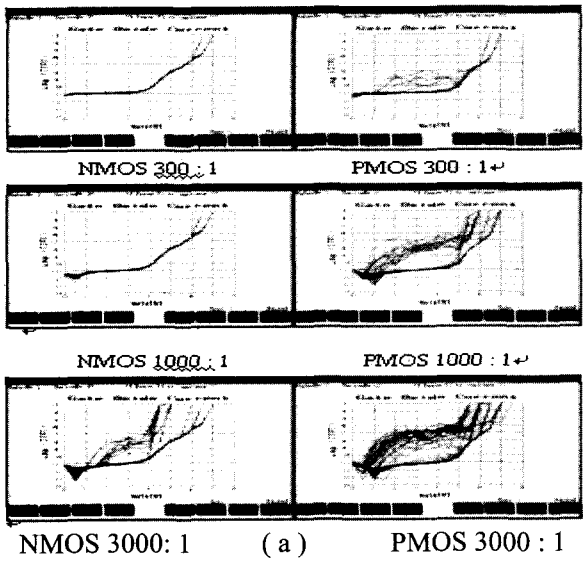
Fig. 2. (a) Antenna test patterns (b) Comb type (c) Block type.

In general, the block type structure is sensitive to charging from dielectric deposition process, also comb type structure is sensitive to charging from metal etch process. We used the characterization techniques adapted to the degradation level. When structures were strongly damaged, we measured the gate leakage current in inversion regime with $V_g = 3V$.

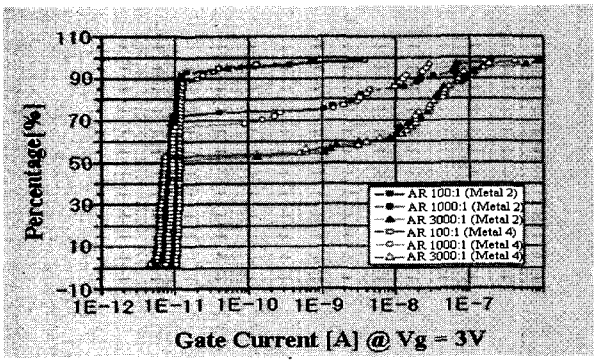
3. RESULTS AND DISCUSSION

Figure 3 shows the results of the antenna structure test with the split A condition. It is indicated that the PMOS degradation is much higher than the NMOS one. Figure 3 (a) comparatively represents the change of gate oxide currents with a block type antenna structure as a various antenna ratios between poly and metal-1 in NMOS and PMOS, respectively.

Figure 3 (b) shows the fail percentages of gate currents at $V_g = 3V$ with a comb type antenna structure as a various antenna ratios. Metal comb antenna structures are more sensitive to cumulative charging of metal etching than HDP IMD deposition process. Block type antenna fail map in NMOS and PMOS are shown with an antenna ratio of 3K:1 in Fig. 3 (c).



(a)



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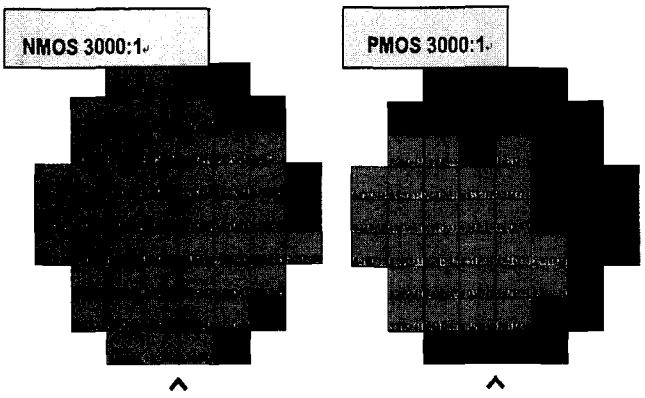
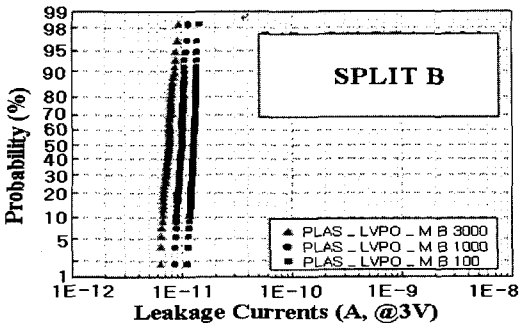
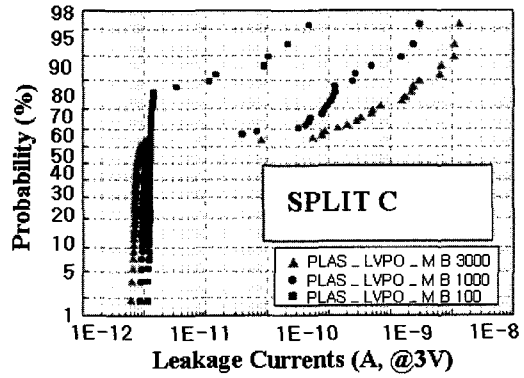


Fig. 3. Split A (Top -SiH_4 off, liner high depo temp) : (a) Metal-1 NMOS vs PMOS block type Antenna fail (b) Metal 2,4 PMOS block type antenna fail, and (c) NMOS vs PMOS block type 3K:1 ant fail map.

Figure 4 represents the changes of leakage currents at fixed gate voltage (V_g = 3V) with block type antenna. And Fig. 5 also shows the variations of leakage currents at fixed gate voltage (V_g = 3V) with comb type antenna. We changed the split conditions of B, C and D in Table 1



(a)



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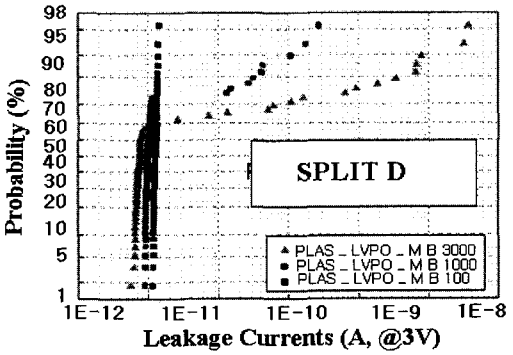
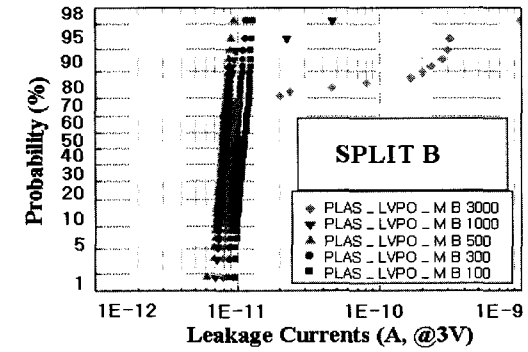


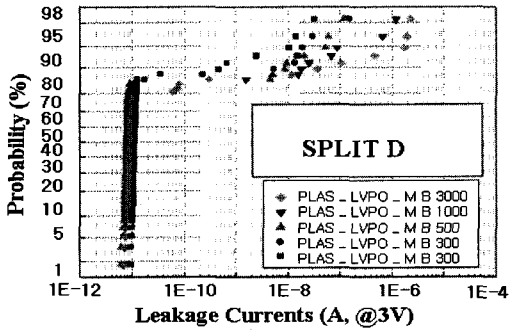
(c)

Fig. 4. PMOS block type antenna gox leakage I.

in order to investigate the influence of the top SiH_4 pre flow and the wafer temperature on plasma-induced damage. It is indicated that the HDP IMD process has much more damaging than the metal etching one in Fig. 4 and Fig. 5. We can point out that plasma damage more strongly depends on top SiH_4 pre flow than the wafer temperature. Meanwhile, Fig.3, Fig. 4, and Fig. 5 show the influence of the deposited liner oxide thickness uniformity and temperature on the HDP CVD charging damage. These show that this charging is correlated with the presence of non-conformal liner on the metal lines and dependent of wafer temperature.



(a)



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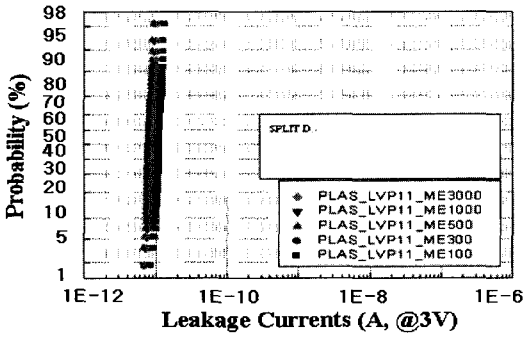

(c)

Fig. 5. PMOS comb type antenna gox leakage I.

Table 3. PMOS block type antenna fail rate.

Split	Ant Fail rate	
	1K : 1	3K : 1
A	16/56 (29%)	28/56 (50%)
B	0/56 (0%)	0/56 (0%)
C	19/56 (34%)	20/56 (36%)
D	9/56 (16%)	14/56 (25%)

Table 3 represents the fail rates with the block type antenna as the respective split conditions. As shown in Table 3, the fail rates were 0% in split B condition with the both antenna ratios of 1K:1 and 3K:1. Split B condition is the top SiH_4 pre flow and low wafer temperature conditions. As a result of these experiments, it is confirmed that the top SiH_4 pre flow and low wafer temperature useful for reduction of plasma-induced damage.

4. CONCLUSION

We have evidenced the existence of initial liner deposition condition dependent charging in High Density Plasma CVD process. Especially, when top SiH_4 pre flow method applied, within wafer thickness uniformity changed from the thin center to the thick outer. This method has conformal coating of liner, before HDP main deposition. Therefore, this technique provides to prevent the electron shading damage effects caused by the topographical dependence. Also, it is very important for keeping the low deposition temperature to prevent plasma charging damage.

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